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Information technology – AT attachment with packet interface-7 –
Part 2: Parallel transport protocols and physical interconnect (ATA/ATAPI-7)

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INFORMATION TECHNOLOGY – AT ATTACHMENT WITH PACKET INTERFACE-7 –

Part 2: Parallel transport protocols and physical interconnect (ATA/ATAPI-7)

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International Standard ISO/IEC 24739-2 was prepared by subcommittee 25: Interconnection of information technology equipment, of ISO/IEC joint technical committee 1: Information technology.

ISO/IEC 24739-2 is to be used in conjunction with ISO/IEC 24739-1 and ISO/IEC 24739-3.

The list of all currently available parts of the ISO/IEC 24739 series, under the general title *Information technology – AT attachment with packet interface-7* , can be found on the IEC web site.

This International Standard has been approved by vote of the member bodies and the voting results may be obtained from the address given on the second title page.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

INTRODUCTION

The ISO/IEC 24739 series specifies the AT attachment interface between host systems and storage devices. It provides a common attachment interface for systems manufacturers, system integrators, software suppliers and suppliers of intelligent storage devices.

Part 1 defines the register delivered commands used by devices implementing the standard. Part 2 defines the connectors and cables for physical interconnection between host and storage device, the electrical and logical characteristics of the interconnecting signals and the protocols for the transporting of commands, data and status over the interface for the parallel interface. Part 3 defines the connectors and cables for physical interconnection between host and storage device, the electrical and logical characteristics of the interconnecting signals and the protocols for the transporting of commands, data and status over the interface for the serial interface. Figure 1 shows the relationship of these documents. For devices implementing the PACKET command feature set, additional command layer standards are listed in Table 1 and described in Clause 2.

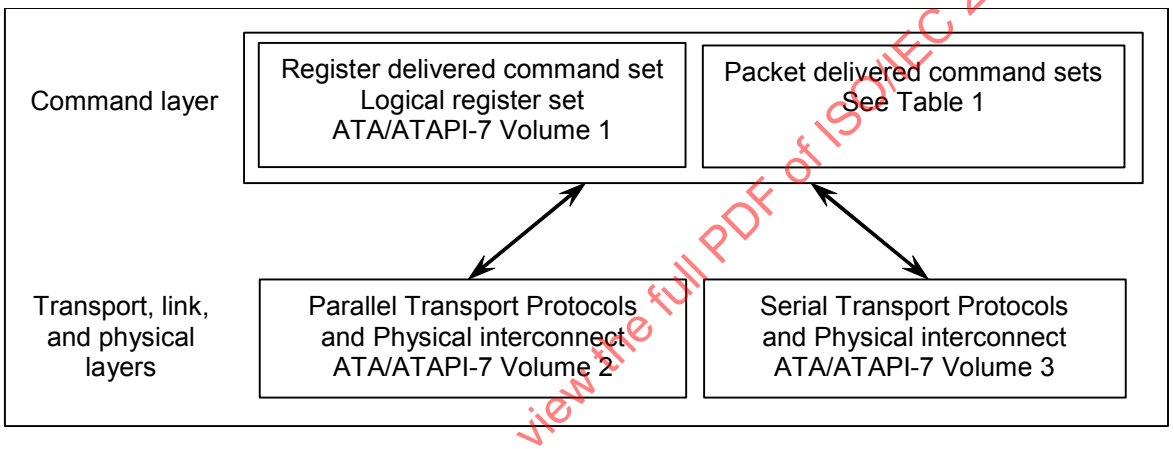

Figure 1 – ATA document relationships

Table 1 – PACKET delivered command sets

Standard
SCSI Primary Commands (SPC)
SCSI Primary Commands-2 (SPC-2)
SCSI Primary Commands-3 (SPC-3)
SCSI Block Commands (SBC-2)
SCSI Stream Commands (SSC)
Multimedia Commands (MMC)
Multimedia Commands-2 (MMC-2)
Multimedia Commands-3 (MMC-3)
Multimedia Commands-4 (MMC-4)
ATAPI for Removable Media (SFF8070I)
ATA Packet Interface (ATAPI) for Streaming Tape QIC-157 revision D

This standard maintains compatibility with the AT Attachment with Packet Interface-6 standard (ATA/ATAPI-6) and while providing additional functions, is not intended to require changes to presently installed devices or existing software.

INFORMATION TECHNOLOGY – AT ATTACHMENT WITH PACKET INTERFACE-7 –

Part 2: Parallel transport protocols and physical interconnect (ATA/ATAPI-7)

1 Scope

This part of ISO/IEC 24739 specifies the AT Attachment Interface between host systems and storage devices. It provides a common attachment interface for systems manufacturers, system integrators, software suppliers and suppliers of intelligent storage devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document, including any amendments, applies.

The provisions of the referenced specifications other than ISO/IEC, IEC, ISO and ITU documents, as identified in this clause, are valid within the context of this International Standard. The reference to such a specification within this International Standard does not give it any further status within ISO/IEC. In particular, it does not give the referenced specification the status of an International Standard.

ISO/IEC 14776-362, *Information technology – Small Computer System Interface (SCSI) – Part 362: Multimedia commands-2 (MMC-2)* [ANSI INCITS 333-2000]

PC Card Standard, February 1995, PCMCIA [1]

CompactFlash™ Association Specification, Revision 1.4[2]

3 Terms, definitions, abbreviations, conventions and keywords

3.1 Terms, definitions and abbreviations

For the purposes of this International Standard, the following definitions as well as the definitions of ISO/IEC 24739-1 and ISO/IEC 24739-3, as soon as they are available, apply.

NOTE ISO/IEC 24739-1 and ISO/IEC 24739-3 are currently in preparation (see also 3.4).

3.1.1
ASCII character
designates a 8-bit value that is encoded using the ASCII character set

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1 For the PC Card Standard published by the Personal Computer Memory Card International Association, contact PCMCIA at 408-433-2273 or http://www.pcmcia.org.

2 For the Compact Flash Association Specification published by the Compact Flash Association, contact the Compact Flash Association at http://www.compactflash.org.

CompactFlash™ is the trademark of the Compact Flash Association. This information is given for the convenience of users of this document and does not constitute an endorsement by IEC or ISO of this trademark. Equivalent descriptons may be used if they can be shown to lead to the same results.

3.1.2
acoustics
measurement of airborne noise emitted by information technology and telecommunications equipment

[ISO 7779:1999]

3.1.3
ATA
AT attachment
ATA defines the physical, electrical, transport and command protocols for the internal attachment of storage devices to host systems

3.1.4
ATA-1 device
device that complied with ANSI X3.221-1994, the AT Attachment Interface for Disk Drives

NOTE ANSI X3.221-1994 has been withdrawn.[3]

3.1.5
ATA-2 device
device that complied with ANSI X3.279-1996, the AT Attachment Interface with Extensions

NOTE ANSI X3.279-1996 has been withdrawn.[3]

3.1.6
ATA-3 device
device that complies with ANSI INCITS 298-1997, the AT Attachment-3 Interface

NOTE ANSI INCITS 298-1997 has been withdrawn.[3]

3.1.7
ATA/ATAPI-4 device
device that complies with ANSI INCITS 317-1998, AT Attachment Interface with Packet Interface Extensions-4

3.1.8
ATA/ATAPI-5 device
device that complies with ANSI INCITS 340-2000, the AT Attachment with Packet Interface-5

3.1.9
ATA/ATAPI-6 device
device that complies with ANSI INCITS 361-2002, the AT Attachment with Packet Interface-6

3.1.10
ATA/ATAPI-7 device
device that complies with this series of International Standards

3.1.11
ATAPI device
AT attachment packet interface device
device implementing the packet command feature set

[3] For further information contact ANSI http://www.ansi.org/.

3.1.12
allocation unit
AU
the minimum number of logically contiguous sectors on the media as used in the streaming feature set

NOTE An Allocation Unit may be accessed with one or more request.

3.1.13
audio-video
AV
audio-video applications use data that is related to video images and/or audio; the distinguishing characteristic of this type of data is that accuracy is of lower priority than timely transfer of the data

3.1.14
backchannel
when transmitting a FIS, the backchannel is the receive channel

3.1.15
bit error rate
BER
statistical probability of a transmitted encoded bit being erroneously received in a communication system

3.1.16
bus release
for devices implementing overlap, the term bus release is the act of clearing both DRQ and BSY to zero before the action requested by the command is completed; this allows the host to select the other device or deliver another queued command

3.1.17
byte count
value placed in the byte count register by the device to indicate the number of bytes to be transferred during this DRQ assertion when executing a PACKET PIO data transfer command

3.1.18
byte count limit
value placed in the byte count register by the host as input to a PACKET PIO data transfer command to specify the maximum byte count that may be transferred during a single DRQ assertion

3.1.19
CompactFlash™ Association
CFA
association which created the specification for compact flash memory that uses the ATA interface

3.1.20
check condition
for devices implementing the PACKET command feature set, this indicates an error or exception condition has occurred

3.1.21
cylinder-head-sector
CHS
obsolete method of addressing the data on the device by cylinder number, head number and sector number

3.1.22
code violation
in a serial interface implementation, a code violation is an error that occurs in the decoding of an encoded character

[see ISO/IEC 24739-3, Clause 15]

3.1.23
command aborted
command completion with ABRT set to one in the error register and ERR set to one in the status register

3.1.24
command acceptance
a command is considered accepted whenever the currently selected device has the BSY bit cleared to zero in the status register and the host writes to the command register

NOTE An exception exists for the DEVICE RESET command (see ISO/IEC 24739-1:2008, Clause 6). In a serial implementation, command acceptance is a positive acknowledgment of a host to device register FIS.

3.1.25
command block registers
interface registers used for delivering commands to the device or posting status from the device

NOTE In a serial implementation, the command block registers are FIS payload fields.

3.1.26
command completion
completion by the device of the action requested by the command or the termination of the command with an error, the placing of the appropriate error bits in the error register, the placing of the appropriate status bits in the status register, the clearing of both BSY and DRQ to zero and Interrupt Pending

3.1.27
command packet
data structure transmitted to the device during the execution of a PACKET command that includes the command and command parameters

3.1.28
command released
when a device supports overlap or queuing, a command is considered released when a bus release occurs before command completion

3.1.29
control block registers
in a parallel implementation, interface registers used for device control and to post alternate status; in a serial interface implementation, the logical field of a FIS corresponding to the device register bits of a parallel implementation

3.1.30
control character
in a serial interface implementation, an encoded character that represents a non-data byte

[see ISO/IEC 24739-3:2008, Clause 15]

3.1.31
cyclical redundancy check
CRC
means used to check the validity of certain data transfers

3.1.32
cylinder high register
name used for the LBA high register in previous ATA/ATAPI standards

3.1.33
cylinder low register
name used for the LBA mid register in previous ATA/ATAPI standards

3.1.34
data character
in a serial interface implementation, an encoded character that represents a data byte (see ISO/IEC 24739-3, Clause 15)

3.1.35
data-in
protocol that moves data from the device to the host

NOTE These transfers are initiated by READ commands.

3.1.36
data-out
protocol that moves data from the host to the device

NOTE These transfers are initiated by WRITE commands.

3.1.37
delayed LBA
any sector for which the performance specified by the streaming performance parameters log is not valid

3.1.38
device
storageperipheral
traditionally, a device on the interface has been a hard disk drive, but any form of storage device may be placed on the interface provided the device adheres to this standard

3.1.39
device selection
in a parallel implementation, a device is selected when the DEV bit of the device register is equal to the device number assigned to the device by means of a device 0/device 1 jumper or switch, or use of the CSEL signal

NOTE In a serial implementation the device ignores the DEV bit, the host adapter may use this bit to emulate device selection.

3.1.40
disparity
difference between the number of ones and the number of zeroes in an encoded character

[see ISO/IEC 24739-3, Clause 15]

3.1.41
DMA data transfer
direct memory access data transfer
means of data transfer between device and host memory without host processor intervention

3.1.42
don't care
term to indicate that a value is irrelevant for the particular function described

3.1.43
driver
active circuit inside a device or host that sources or sinks current to assert or negate a signal on the bus

3.1.44
DRQ data block
unit of data words transferred during a single assertion of DRQ when using PIO data transfer

3.1.45
elasticity buffer
in a serial interface implementation, a portion of the receiver where character slipping and/or character alignment is performed

3.1.46
encoded character
in a serial interface implementation, the output of the 8b/10b encoder

[see ISO/IEC 24739-3, Clause 0]

3.1.47
first party DMA access
method by which a device accesses host memory

NOTE First party DMA differs from DMA in that the device sends a DMA setup FIS to select host memory regions; whereas for DMA the host configures the DMA controller.

3.1.48
frame information structure
FIS
data structure; it is the payload of a frame and does not include the SOF primitive, CRC and EOF primitive

3.1.49
frame
unit of information exchanged between the host adapter and a device

NOTE A frame consists of an SOF primitive, a Frame Information Structure, a CRC calculated over the contents of the FIS and an EOF primitive.

3.1.50
forced unit access
FUA
requires that user data be transferred to or from the device media before command completion even if caching is enabled

3.1.51
Gen1 DWORD time
the time it takes to transmit a 40 bit encoded value at 1.5 Gbit/s

3.1.52
host
computer system executing the software BIOS and/or operating system device driver controlling the device and the adapter hardware for the ATA interface to the device

3.1.53
host adapter
implementation of the host transport, link and physical layers

3.1.54
interrupt pending
in a parallel implementation, an internal state of a device;
in this state, the device asserts INTRQ if nIEN is cleared to zero and the device is selected [see Clause 8];
in a serial implementation, the Interrupt Pending state is an internal state of the host adapter; this state is entered by reception of a FIS with the I field set to one

[see ISO/IEC 24739-3, Clause 16]

3.1.55
logical block address
LBA
addressing of data on the device by the linear mapping of sectors

3.1.56
linear feedback shift register
LFSR
[see ISO/IEC 24739-3, Clause 0]

3.1.57
link
the link layer manages the phy layer to achieve the delivery and reception of frames (see ISO/IEC 24739-3, Clause 15)

3.1.58
logical sector
a uniquely addressable set of 256 words (512 bytes)

3.1.59
native max address
the highest address a device accepts in the factory default condition, that is, the highest address that is accepted by the SET MAX ADDRESS command

3.1.60
overlap
a protocol that allows devices that require extended command time to perform a bus release so that commands may be executed by the other device (if present) on the bus

3.1.61
packet delivered command
command that is delivered to the device using the PACKET command via a command packet that contains the command and the command parameters. See also register delivered command

3.1.62
PHY
physical layer electronics

[see ISO/IEC 24739-3, Clause 14]

3.1.63
physical sector
group of contiguous logical sectors that are read from or written to the device media in a single operation

3.1.64
programmed input/output data transfer
PIO data transfer
PIO data transfers are performed by the host processor utilizing accesses to the data register

3.1.65
primitive
in a serial interface implementation, a single DWORD of information that consists of a control character in byte 0 followed by three additional data characters in byte 1 through 3

3.1.66
queued
command queuing allows the host to issue concurrent commands to the same device

NOTE Only commands included in the Overlapped feature set may be queued. In this standard, the queue contains all commands for which command acceptance has occurred, but command completion has not occurred.

3.1.67
read command
command that causes the device to transfer data from the device to the host (e.g., READ SECTOR(S), READ DMA, etc.)

3.1.68
register
register may be a physical hardware register or a logical field

3.1.69
register delivered command
command that is delivered to the device by placing the command and all of the parameters for the command in the device command block registers

NOTE See also packet delivered command.

3.1.70
register transfers
host reading and writing any device register except the data register; register transfers are 8 bits wide

3.1.71
released
in a parallel interface implementation, indicates that a signal is not being driven

NOTE For drivers capable of assuming a high-impedance state, this means that the driver is in the high-impedance state. For open-collector drivers, the driver is not asserted.

3.1.72
sector
uniquely addressable set of 256 words (512 bytes)

3.1.73
sector number register
LBA low register in previous ATA/ATAPI standards

3.1.74
shadow command block
in a serial interface implementation, a set of virtual fields in the host adapter that map the command block registers defined at the command layer to the fields within the FIS content

3.1.75
shadow control block
in a serial interface implementation, a set of virtual fields in the host adapter that map the control block registers defined at the command layer to the fields within the FIS content

3.1.76
signature
unique set of values placed in the command block registers by the device to allow the host to distinguish devices implementing the PACKET command feature set from those devices not implementing the PACKET command feature set

3.1.77
self-monitoring, analysis and reporting technology
SMART
for prediction of device degradation and/or faults

3.1.78
transport
transport layer manages the lower layers (link and phy) as well as constructing and parsing FISs

[see ISO/IEC 24739-3, Clause 16]

3.1.79
ultra DMA burst
the period from an assertion of DMACK− to the subsequent negation of DMACK− when an ultra DMA transfer mode has been enabled by the host

3.1.80
unaligned write
write command that does not start at the first logical sector of a physical sector or does not end at the last logical sector of a physical sector

3.1.81
unit attention condition
state that a device implementing the PACKET command feature set maintains while the device has asynchronous status information to report to the host

3.1.82
unrecoverable error
when the device sets either the ERR bit or the DF bit to one in the status register at command completion

3.1.83
vendor specific
VS
bits, bytes, fields and code values that are reserved for vendor specific purposes

NOTE 1 These bits, bytes, fields and code values are not described in this standard and they may vary among vendors. This term is also applied to levels of functionality whose definition is left to the vendor.

NOTE 2 Industry practice could result in conversion of a Vendor Specific bit, byte, field or code value into a defined standard value in a future standard.

3.1.84
write command
command that causes the device to transfer data from the host to the device (e.g., WRITE SECTOR(S), WRITE DMA, etc.)

3.1.85
world wide name
WWN
64-bit worldwide unique name based upon a company's IEEE identifier

[see IDENTIFY DEVICE Words (111:108) in ISO/IEC 24739-1, Clause 6.]

3.2 Abbreviations

ATA	AT Attachment
ATAPI	AT Attachment Packet Interface
AU	Allocation Unit
AV	Audio-Video
AWG	American Wire Gauge
BER	Bit Error Rate
CD	Card Detect
CFA	CompactFlash™ Association
CHS	Cylinder-Head-Sector
CRC	Cyclical Redundancy Check
CS	Device Chips Select
CSEL	Cable Select
DC	Direct Current
DD	Device Data
DDIAG	Device Diagnostic
DIOW	Device Input Output Write
DMA	Direct Memory Access
DMACK	DMA Knowledge
DMARQ	DMA Request
EVN	Even
FIS	Frame Information Structure
FUA	Forced Unit Access
IOWR	Input Output Read Write
LBA	Logical Block Address
LFSR	Linear Feedback Shift Register
OC	Open Collector
ODD	Odd
PC	Personal Computer
PCB	Printed Circuit Board
PD	Pull-down
PHY	Physical Layer Electronics
PIO	Programmed Input/Output data transfer
PU	Pull-Up

SMART	Self-Monitoring, Analysis And Reporting Technology
TP	Totem-Pole
TS	Tri-State
WWN	World Wide Name
VS	Vendor Specific

3.3 Conventions

3.3.1 General

Lowercase is used for words having the normal English meaning. Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in Clause 3 or in the text where they first appear.

The names of abbreviations, commands, fields and acronyms used as signal names are in all uppercase (e.g., IDENTIFY DEVICE). Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field. (See 3.3.7 for the naming convention used for naming bits.)

Names of device registers begin with a capital letter (e.g., LBA Mid register).

The expression “word n” or “bit n” shall be interpreted as indicating the content of word n or bit n.

3.3.2 Precedence

If there is a conflict between text, figures and tables, the precedence shall be tables, figures, then text.

3.3.3 Lists

Ordered lists, those lists describing a sequence, are of the form:

a)
b)
c)

Unordered list are of the form:

1)
2)
3)

3.3.4 Keywords

Several keywords are used to differentiate between different levels of requirements and optionality.

3.3.4.1 expected

Keyword used to describe the behavior of the hardware or software in the design models assumed by this standard. Other hardware and software design models may also be implemented.

3.3.4.2 mandatory

Keyword indicating items to be implemented as defined by this standard.

3.3.4.3 may

Keyword that indicates flexibility of choice with no implied preference.

3.3.4.4 obsolete

Keyword indicating that the designated bits, bytes, words, fields and code values that may have been defined in previous standards are not defined in this standard and shall not be reclaimed for other uses in future standards. However, some degree of functionality may be required for items designated as “obsolete” to provide for backward compatibility.

Obsolete commands should not be used by the host. Commands defined as obsolete may be command aborted by devices conforming to this standard. However, if a device does not command abort an obsolete command, the minimum that is required by the device in response to the command is command completion.

3.3.4.5 optional

Keyword that describes features that are not required by this standard. However, if any optional feature defined by the standard is implemented, the feature shall be implemented in the way defined by the standard.

3.3.4.6 prohibited

Keyword ind icating that an item shall not be implemented by an implementation.

3.3.4.7 reserved

Keyword indicating reserved bits, bytes, words, fields and code values that are set aside for future standardization. Their use and interpretation may be specified by future extensions to this or other standards. A reserved bit, byte, word or field shall be cleared to zero, or in accordance with a future extension to this standard. The recipient shall not check reserved bits, bytes, words or fields. Receipt of reserved code values in defined fields shall be treated as a command parameter error and reported by returning command aborted.

3.3.4.8 retired

Keyword indicating that the designated bits, bytes, words, fields and code values that had been defined in previous standards are not defined in this standard and may be reclaimed for other uses in future standards. If retired bits, bytes, words, fields or code values are used before they are reclaimed, they shall have the meaning or functionality as described in previous standards.

3.3.4.9 shall

Keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this standard.

3.3.4.10 should

Keyword indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase “it is recommended”.

3.3.5 Numbering

Numbers that are not immediately followed by a lowercase "b" or "h" are decimal values. Numbers that are immediately followed by a lowercase "b" (e.g., 01b) are binary values. Numbers that are immediately followed by a lowercase "h" (e.g., 3Ah) are hexadecimal values.

3.3.6 Signal conventions

Signal names are shown in all uppercase letters.

All signals are either high active or low active signals. A dash character (-) at the end of a signal name indicates the signal is a low active signal. A low active signal is true when the signal is below V_{iL} and is false when the signal is above V_{iH}. No dash at the end of a signal name indicates the signal is a high active signal. A high active signal is true when the signal is above V_{iH} and is false when the signal is below V_{iL}.

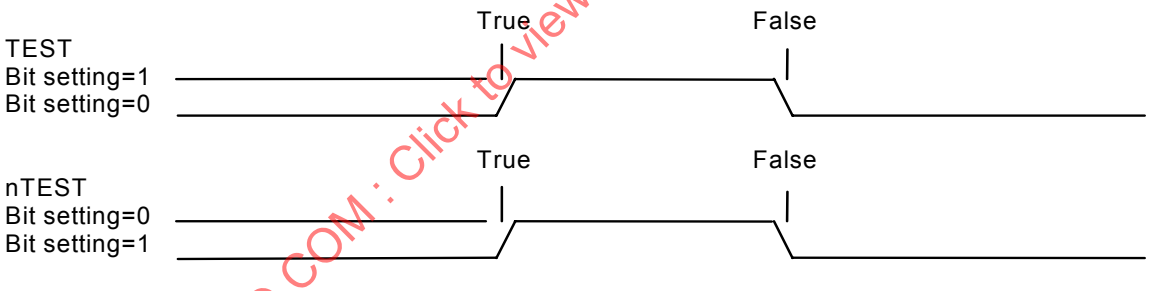
“Asserted” means that the signal is driven by an active circuit to the true state. “Negated” means that the signal is driven by an active circuit to the false state. “Released” means that the signal is not actively driven to any state (see Clause 7). Some signals have bias circuitry that pull the signal to either a true state or false state when no signal driver is actively asserting or negating the signal.

Control signals that may be used for more than one mutually exclusive function are identified with their function names separated by a colon (e.g., DIOW-:STOP).

SIGNAL(n:m) denotes a set of signals, for example, DD(15:0).

3.3.7 Bit conventions

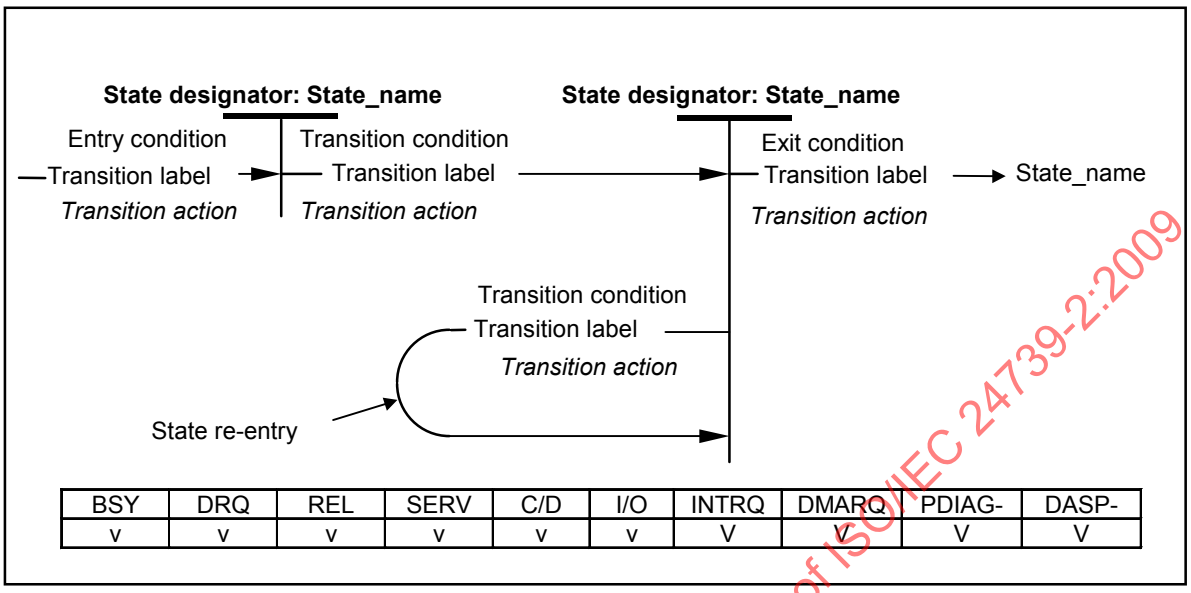
Bit names are shown in all uppercase letters except where a lowercase n precedes a bit name. If there is no preceding n, then when BIT is set to one the meaning of the bit is true and when BIT is cleared to zero the meaning of the bit is false. If there is a preceding n, then when nBIT is cleared to zero, the meaning of the bit is true and when nBIT is set to one, the meaning of the bit is false.



Bit (n:m) denotes a set of bits, for example, bits (7:0).

3.3.8 State diagram conventions

State diagrams shall be as shown in Figure 2.



BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
v	v	v	v	v	v	V	V	V	V

Figure 2 – State diagram convention

Each state is identified by a state designator and a state name. The state designator is unique among all states in all state diagrams in this document. The state designator consists of a set of letters that are capitalized in the title of the figure containing the state diagram followed by a unique number. The state name is a brief description of the primary action taken during the state and the same state name may appear in other state diagrams. If the same primary function occurs in other states in the same state diagram, they are designated with a unique letter at the end of the name. Additional actions may be taken while in a state and these actions are described in the state description text.

In device command protocol state diagrams, the state of bits and signals that change state during the execution of this state diagram are shown under the state designator:state_name and a table is included that shows the state of all bits and signals throughout the state diagram as follows:

v = bit value changes.
1 = bit set to one.
0 = bit cleared to zero.
x = bit is don't care.
V = signal changes.
A = signal is asserted.
N = signal is negated.
R = signal is released.
X = signal is don't care.

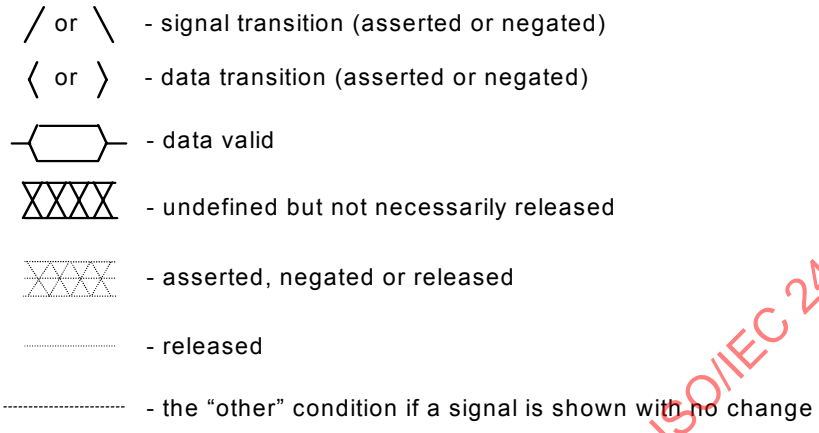
Each transition is identified by a transition label and a transition condition. The transition label consists of the state designator of the state from which the transition is being made, followed by the state designator of the state to which the transition is being made. In some cases, the transition to enter or exit a state diagram may come from or go to a number of state diagrams, depending on the command being executed. In this case, the state designator is labeled xx. The transition condition is a brief description of the event or condition that causes the transition to occur and may include a transition action, indicated in italics, that is taken when the transition occurs. This action is described fully in the transition description text.

Upon entry to a state, all actions to be executed in that state are executed. If a state is re-entered from itself, all actions to be executed in the state are executed again.

Transitions from state to state shall be instantaneous.

3.3.9 Timing conventions

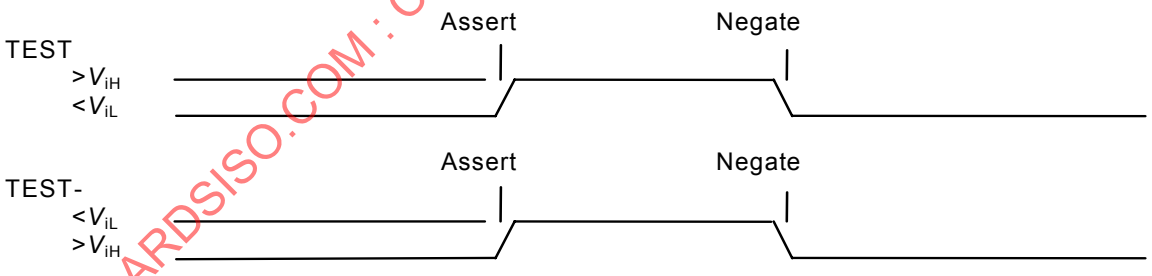
Certain symbols are used in the timing diagrams. These symbols and their respective definitions are listed below.



All signals are shown with the asserted condition facing to the top of the page. The negated condition is shown towards the bottom of the page relative to the asserted condition.

The interface uses a mixture of negative and positive signals for control and data. The terms asserted and negated are used for consistency and are independent of electrical characteristics.

In all timing diagrams, the lower line indicates negated and the upper line indicates asserted. The following illustrates the representation of a signal named TEST going from negated to asserted and back to negated, based on the polarity of the signal.



3.3.10 Byte ordering for data transfers

Data is transferred in blocks using either PIO or DMA protocols. PIO data transfers occur when the BSY bit is cleared to zero and the DRQ bit is set to one. These transfers are usually 16-bit but CFA devices may implement 8-bit PIO transfers. Data is transferred in blocks of one or more bytes known as a DRQ block. DMA data transfers occur when the host asserts DMACK− in response to the device asserting DMARQ. DMA transfers are always 16-bit. Each assertion of DMACK− by the host defines a DMA data burst. A DMA data burst is two or more bytes.

Assuming a DRQ block or a DMA burst of data contains "n" bytes of information, the bytes are labeled Byte(0) through Byte(n-1), where Byte(0) is first byte of the block and Byte(n-1) is the last byte of the block. Table 2 shows the order the bytes shall be presented in when such a block of data is transferred on the interface using 16-bit PIO and DMA transfers. Table 3 shows the order the bytes shall be presented in when such a block or burst of data is transferred on the interface using 8-bit PIO.

Table 2 – Byte order

	DD 15	DD 14	DD 13	DD 12	DD 11	DD 10	DD 9	DD 8	DD 7	DD 6	DD 5	DD 4	DD 3	DD 2	DD 1	DD 0
First transfer	Byte (1)								Byte (0)							
Second transfer	Byte (3)								Byte (2)							
.....																
Last transfer	Byte (n-1)								Byte (n-2)							

Table 3 – Byte order

	DD 7	DD 6	DD 5	DD 4	DD 3	DD 2	DD 1	DD 0
First transfer	Byte (0)							
Second transfer	Byte (1)							
.....								
Last transfer	Byte (n-1)							

NOTE The above description is for data on the interface. Host systems and/or host adapters may cause the order of data as seen in the memory of the host to be different.

Some parameters are defined as a string of ASCII characters. ASCII data fields shall contain only code values 20h through 7Eh. For the string “Copyright”, the character “C” is the first byte, the character “o” is the second byte, etc. When these fields are transferred, the order of transmission is:

the 1st character (“C”) is on DD(15:8) of the first word,
the 2nd character (“o”) is on DD(7:0) of the first word,
the 3rd character (“p”) is on DD(15:8) of the second word,
the 4th character (“y”) is on DD(7:0) of the second word,
the 5th character (“r”) is on DD(15:8) of the third word,
the 6th character (“i”) is on DD(7:0) of the third word,
the 7th character (“g”) is on DD(15:8) of the fourth word,
the 8th character (“h”) is on DD(7:0) of the fourth word,
the 9th character (“t”) is on DD(15:8) of the fifth word,
the 10th character (“space”) is on DD(7:0) of the fifth word,
etc.

Word (n:m) denotes a set of words, for example, words (103:100).

3.3.11 Byte, word and DWORD relationships

Figure 3 illustrates the relationship between bytes, words and DWORDs for serial interface implementations.

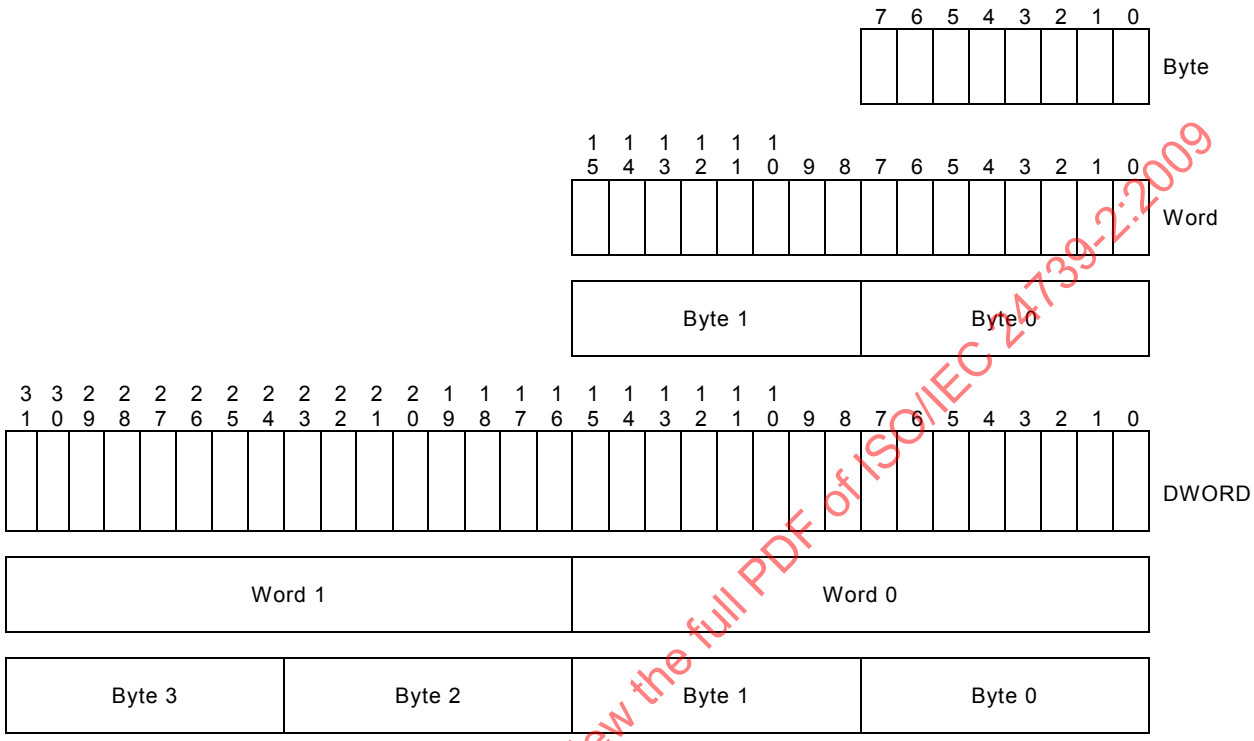


Figure 3 – Byte, word and DWORD relationships

3.4 Relationship of this part of ISO/IEC 24739 to ISO/IEC 24739-1 and ISO/IEC 24739-3

Originally, the three parts formed a single specification. For the convenience of the user, it was decided that this large specification will be published in three parts. However, to comply with other existing publications and to show the close interdependece between the three parts, the original overall structure was kept as far as practicable. Therefore, entire Clauses and Annexes have been left empty with a reference to where they can be found in either Part 1 or Part 3.

4 General operational requirements

Refer to ISO/IEC 24739-1, Clause 4 for operational requirements (see 3.4).

5 I/O register descriptions

Refer to ISO/IEC 24739-1, Clause 5 for I/O register descriptions and see also Clause 10 for parallel interface register addressing (see 3.4).

6 Command descriptions

Refer to ISO/IEC 24739-1, Clause 6 for command descriptions (see 3.4).

7 Parallel interface physical and electrical requirements

7.1 Cable configuration

This standard defines an interface containing a single host or host adapter and one or two devices. One device is configured as Device 0 and the other device as Device 1.

The designation of a device as Device 0 or Device 1 may be made in a number of ways including but not limited to

- a switch or a jumper on the device,
- use of the Cable Select (CSEL) pin.

The host shall be placed at one end of the cable. It is recommended that, for a single device configuration, the device be placed at the opposite end of the cable from the host. If a single device configuration is implemented with the device not at the end of the cable, a cable stub results that may cause degradation of signals. Single device configurations with the device not at the end of the cable shall not be used with Ultra DMA modes.

7.2 Electrical characteristics

7.2.1 General

Table 4 defines the DC characteristics of the interface signals. Table 5 defines the AC characteristics. These characteristics apply to both host and device, unless otherwise specified.

Table 4 – DC characteristics

Description		Minimum	Maximum
I_{oL}	Driver sink current [a]	4 mA	
I_{oLDASP}	Driver sink current for DASP [a]	12 mA	
I_{oH}	Driver source current [b]	400 µA	
$I_{oHDMARQ}$	Driver source current for DMARQ [b]	500 µA	
I_Z	Device pull-up current on DD(15:8), DD(6:0) and STROBE when released	−100 µA	200 µA
I_{ZDD7}	Device pull-up current on DD7 when released	−100 µA	10 µA
V_{iH}	Voltage input high	2.0 VDC	5.5 VDC
V_{iL}	Voltage input low		0.8 VDC
V_{oH}	Voltage output high at I_{oH} min [c]	2.4 VDC	
V_{oL}	Voltage output low at I_{oL} min [c]		0.5 VDC
Additional DC characteristics for Ultra DMA modes greater than 4			
VDD3	DC supply voltage to drivers and receivers	3.3 V – 8 %	3.3 V + 8 %
V+	Low to high input threshold	1.5 V	2.0 V
V–	High to low input threshold	1.0 V	1.5 V
VHYS	Difference between input thresholds: ((V+current value) – (V–current value))	320 mV	
VTHRAVG	Average of thresholds: ((V+current value) + (V–current value))/2	1.3 V	1.7 V
VoH2	Voltage output high at -6 mA to +3 mA (at VoH2 the output shall be able to supply and sink current to VDD3) [c]	VDD3 - 0.51 VDC	VDD3 + 0.3 VDC
VoL2	Voltage output low at 6 mA [c]		0.51 VDC
A device shall have less than 64 µA of leakage current into a 6.2 kΩ pull-down resistor while the INTRQ signal is in the			

released state.
a I_{oLDASP} shall be 12 mA minimum to meet legacy timing and signal integrity.
b I_{oH} value at 400 µA is insufficient in the case of DMARQ that is pulled low by a 5.6 kΩ resistor.
c Voltage output high and low values shall be met at the source connector to include the effect of series termination.

Table 5 – AC characteristics

Description		Minimum	Maximum
S_{RISE}	Rising edge slew rate for any signal [a]		1.25 V/ns
S_{FALL}	Falling edge slew rate for any signal [a]		1.25 V/ns
C_{host}	Host interface signal capacitance at the host connector [b]		25 pF
C_{device}	Device interface signal capacitance at the device connector [b]		20 pF
Additional AC characteristics for Ultra DMA modes greater than mode 4			
S_{RISE2}	Rising edge slew rate for DD(15:0) and STROBE [a]	0.40 V/ns	1.0 V/ns
S_{FALL2}	Falling edge slew rate for DD(15:0) and STROBE [a]	0.40 V/ns	1.0 V/ns
VDSSOH	Induced signal to conductor side of device connector for any non-switching data signal at VoH due to simultaneous switching of all other data lines high and low by the device [c]	VDD3 - 500 mV	
VDSSOL	Same as VDSSOH except non-switching data signal at VoL [c]		500 mV
VHSSOH	Induced signal to conductor side of host connector for any non-switching data signal at VoH due to simultaneous switching of all other data lines high and low by the host [c]	VDD3 – 600 mV	
VHSSOL	Same as VHSSOH except non-switching data signal at VoL [c]		600 mV
V_{RING}	AC voltage at recipient connector [d]	-1.0 V	6.0 V
$C_{device2}$	Device capacitance measured at the connector pin [b]		17 pF
C_{ratio}	Ratio of the highest DD(15:0) or STROBE signal capacitance as measured at the connector to the lowest DD(15:0) or STROBE signal capacitance.		1.5
Vih_{PEAK}	The highest voltage reached on a rising transition at the recipient connector within 3 ns of crossing 1.5 V [e]	2.2 V	
V_{ihRING}	The lowest voltage on a high signal at the recipient connector at any time after the rising edge crosses Vih_{PEAK} until activity driven low by a subsequent falling transition [e]	1.7 V	
V_{ilPEAK}	The lowest voltage reached on a falling transition at the recipient connector within 3 ns of crossing 1.5 V [e]		0.8 V
V_{ilRING}	The highest voltage on a low signal at the recipient connector at any time after the falling edge crosses Vil_{PEAK} until activity driven high by a subsequent rising transition [e]		1.3 V

a Signal integrity may be improved by using slower slew rates at slower transfer rates.

b Capacitance measured at 1 MHz .

c See 7.2.2.2 for measurement details.

d The sender shall not generate voltage peaks higher then these absolute limits on DD(15:0) with all data lines switching simultaneously and a single recipient at end of cable. The test load shall be an 18" long, 40-conductor cable in Ultra DMA mode 2, as well as, an 18", long 80-conductor cable operated in the highest Ultra DMA mode supported.

e V_{ihPEAK} , V_{ihRING} , V_{ilPEAK} and V_{ilRING} shall be met in a functioning system across all patterns and shall be met when measured at any connector.

7.2.2 AC characteristics measurement techniques

7.2.2.1 Slew rate

The sender's signals shall be tested while driving an 45.7 cm (18 in) long, 80-conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has no trace, cable, or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and 12.7 mm (0.5 in) or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within 12.7 mm (0.5 in) of the connector. The test load and test points should then be soldered directly to the exposed source side connectors. The test load shall consist of a 15 pF or 40 pF, 5 %, 2.03 mm (0.08 in) by 1.27 mm (0.05 in), surface mount (or smaller size) capacitor from the test point to ground. Slew rates shall be met for both capacitor values. Measurements shall be taken at the test point using a 1 GHz or faster test probe with less than 1 pF capacitance and greater than 100 kΩ impedance connected to a 500 MHz or faster oscilloscope. The average rate shall be measured from 20 % to 80 % of the settled V_{oH} level with data transitions at least 120 ns apart. The settled V_{oH} level shall be measured as the average output high level under the defined testing conditions from 100 ns after 80 % of a rising edge until 20 % of the subsequent falling edge.

7.2.2.2 V_{SSO}

V_{sso} shall be tested with the same test cable configuration as described for slew rate testing except with the test load described here and the cut-cable conductor configuration. For both V_{oL} and V_{oH} measurements, the test load shall consist of a 90.9 Ω 1 % resistor (this also may be accomplished by using 1 kΩ 1 % and 100 Ω 1 % resistors in parallel) and a 0.1 µF 20 % capacitor in series to ground. Both resistor and capacitor shall be 2.03 mm (0.08 in) by 1.27 mm (0.05 in) or smaller surface mount. The order of components should be signal-resistor-capacitor-ground. Refer to 7.2.4.4 for PCB layout requirements related to V_{SSO}.

To generate a test pattern for V_{SSOH} a 32-sector or longer data transfer shall be sent to the recipient. The first 30 sectors shall contain Fh in order to generate an "all 1s" pattern to pre-charge the capacitor to V_{oH}. The final sectors of the command shall contain the required pattern for V_{SSOH} for at least 2 sectors (i.e., a pattern that holds the data line under test at V_{oH} while driving a "1010…" pattern on all other data lines. V_{SSOH} shall be measured within the first 32 words after the pre-charge pattern is complete and the V_{SSOH} pattern begins.

To generate a test pattern for V_{SSOL} a 32-sector or longer data transfer shall be sent to the recipient. The first 30 sectors shall contain 0h in order to generate an "all 0's" pattern to pre-charge the capacitor to V_{oL}. The final sectors of the command shall contain the required pattern for V_{SSOL} for at least 2 sectors (i.e., a pattern that holds the data line under test at V_{oL} while driving a "1010…" pattern on all other data lines. V_{SSOL} shall be measured within the first 32 words after the pre-charge pattern is complete and the V_{SSOL} pattern begins.

7.2.3 Driver types and required termination

Table 6 – Driver types and required termination

Signal	Source	Driver type [a]	Host [b]	Device [b]	Footnotes to table
RESET−	Host	TP			
DD(15:0)	Bidir	TS			c
DMARQ	Device	TS	5.6 kΩ PD		
DIOR-:HDMARDY-:HSTROBE	Host	TS			
DIOW-:STOP	Host	TS			
IORDY:DDMARDY-:DSTROBE	Device	TS	4.7 kΩ PU		f, k
CSEL	Host		Ground	10 kΩ PU	d, f
DMACK-	Host	TP			
INTRQ	Device	TS	10 kΩ		e
DA(2:0)	Host	TP			
PDIAG-:CBLID-	Device	TS		10 kΩ PU	b, f, g, h
CS0- CS1-	Host	TP			
DASP-	Device	OC		1 kΩ PU	f, i

a TS = Tri-state; OC = Open collector; TP = Totem-pole; PU = Pull-up; PD = Pull-down.

b All resistor values are the minimum (lowest allowed) except for the 10 kΩ PU on PDIAG-:CBLID- which shall have a tolerance of ±5 % or less.

c Devices shall not have a pull-up resistor on DD7. The host shall have a 10 kΩ pull-down resistor and not a pull-up resistor on DD7 to allow a host to recognize the absence of a device at power-up so that a host shall detect BSY as being cleared when attempting to read the Status register of a device that is not present.

d When used as CSEL, this line is grounded at the host and a 10 kΩ pull-up is required at both devices.

e A 10 kΩ pull-up or 6.2 kΩ pull-down, depending upon the level sensed, should be implemented at the host.

f Pull-up values are based on +5 V_{CC}. Except for the pull-up on PDIAG-:CBLID- which shall be to +5 V_{CC} for backward compatibility, pull-ups may be to V_{DD3}. For systems supporting Ultra DMA modes greater than 4, the host pull-up on IORDY:DDMARDY-:DSTROBE should be to V_{DD3}.

g Hosts that do not support Ultra DMA modes greater than mode 2 shall not connect to the PDIAG-:CBLID- signal.

h The 80-conductor cable assembly shall meet the following requirements: the PDIAG-:CBLID- signal shall be connected to ground in the host connector of the cable assembly; the PDIAG-:CBLID- signal shall not be connected between the host and the devices; and the PDIAG-:CBLID- signal shall be connected between the devices.

i The host shall not drive DASP-. If the host connects to DASP- for any purpose, the host shall ensure that the signal level detected on the interface for DASP- shall maintain V_{OH} and V_{OL} compatibility, given the I_{OH} and I_{OL} requirements of the DASP- device drivers.

k For host systems not supporting modes greater than Ultra DMA mode 4, a pull-up of 1 kΩ may be used.

7.2.4 Electrical characteristics for Ultra DMA

7.2.4.1 General

Hosts that support Ultra DMA transfer modes greater than mode 2 shall not share signals between primary and secondary I/O ports. They shall provide separate drivers and separate receivers for each cable.

7.2.4.2 Cable configuration

Table 7 defines the host transceiver configurations for a dual cable system configuration for all transfer modes.

Table 7 – Host transceiver configurations

Transfer mode	Optional host transceiver configuration	Recommended host transceiver configuration	Mandatory host transceiver configuration
All PIO and Multiword DMA	One transceiver may be used for signals to both ports.	DIOR-, DIOW- and IORDY should have a separate transceiver for each port.	Either DIOR-, DIOW- and IORDY or CS0- and CS1- shall have a separate transceiver for each port.
Ultra DMA 0, 1, 2	One transceiver may be used for signals to both ports except DMACK-.	DIOR-, DIOW- and IORDY should have a separate transceiver for each port.	Either DIOR-, DIOW- and IORDY or CS0- and CS1- shall have a separate transceiver for each port. DMACK- shall have a separate transceiver for each port.
Ultra DMA modes >2	One transceiver may be used for signals to both ports for RESET-, INTRQ, DA(2:0), CS0-, CS1- and DASP-.	RESET-, INTRQ, DA(2:0), CS0-, CS1- and DASP- should have a separate transceiver for each port.	All signals shall have a separate transceiver for each port except for RESET-, INTRQ, DA(2:0), CS0-, CS1- and DASP-.

Table 8 defines the system configuration for connection between devices and systems for all transfer modes. For Ultra DMA modes requiring an 80-conductor cable, that cable shall meet the requirements for 80-conductor cables (see 7.3.2.3).

Table 8 – System configuration for connection between devices and systems for all transfer modes

Transfer mode	Single device direct connection configuration [a]	40-conductor cable connection configuration [b]	80-conductor cable connection configuration [b]
All PIO and Multiword DMA	May be used.	May be used.	May be used [c]
Ultra DMA 0, 1, 2	May be used.	May be used.	May be used [c]
Ultra DMA modes >2	May be used (See NOTE 4).	Shall not be used.	May be used [d]

[a] Direct connection is a direct point-to-point connection between the host connector and the device connector.

[b] The 40-conductor cable assembly and the 80-conductor cable assembly are defined in 7.3.

[c] 80-conductor cable assemblies may be used in place of 40-conductor cable assemblies to improve signal quality for data transfer modes that do not require an 80-conductor cable assembly.

[d] Either a single device direct connection configuration or an 80-conductor cable connection configuration shall be used for systems operating with Ultra DMA modes greater than 2.

7.2.4.3 Series termination required for Ultra DMA

Series termination resistors are required at both the host and the device for operation in any of the Ultra DMA modes. Table 9 describes typical values for series termination at the host and the device.

For host systems and devices supporting Ultra DMA modes greater than 4, the output and bi-directional series termination values for DD(15:0) and STROBE signals shall be chosen so that the sum of the driver output resistance at V_{oL2} or V_{oH2} and the series termination resistance is

between 50 Ω and 85 Ω. For these systems, the STROBE input shall use the same series termination resistance value as the data lines.

Host systems supporting Ultra DMA modes greater than 5 and having PCB traces longer than 4" shall use series termination resistors of no less than 22 Ω on DD(15:0) and STROBE signals. The termination resistors shall be placed within 12.7 mm (0.5 in) of the host connector.

Table 9 – Typical series termination for Ultra DMA

Signal	Host termination Ω	Device termination Ω
DIOR-:HDMARDY-:HSTROBE	22	82
DIOW-:STOP	22	82
CS0-, CS1-	33	82
DA0, DA1, DA2	33	82
DMACK-	22	82
DD15 through DD0	33	33
DMARQ	82	22
INTRQ	82	22
IORDY:DDMARDY-:DSTROBE	82	22
RESET-	33	82

Only those signals that require termination are listed in this table. If a signal is not listed, series termination is not required for operation in an Ultra DMA mode. Figure 4 shows signals also requiring a pull-up or pull-down resistor at the host. The actual termination values should be selected to compensate for transceiver and trace impedance to match the characteristic cable impedance.

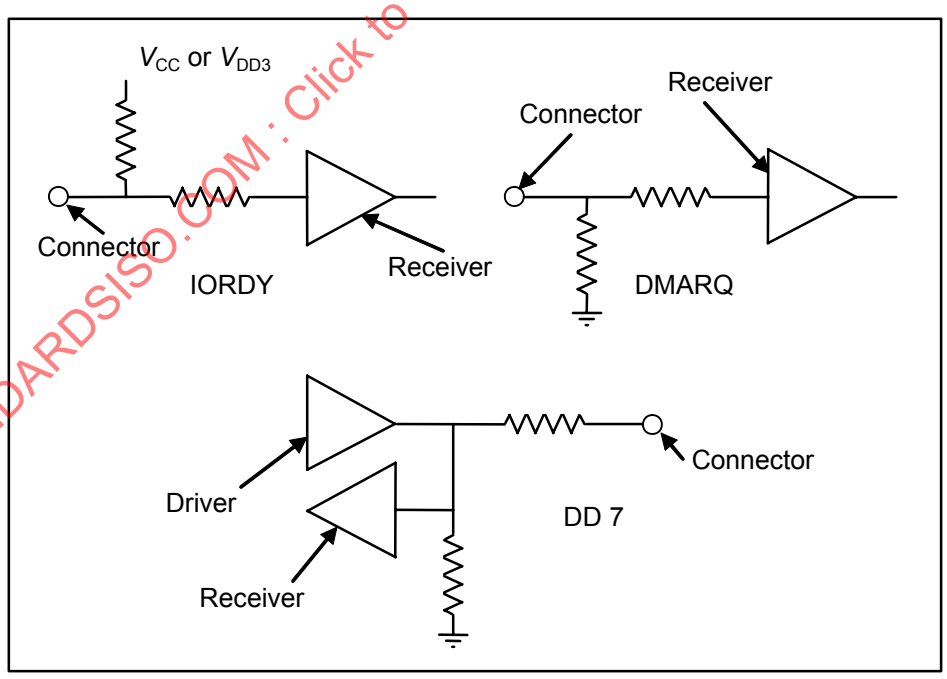


Figure 4 – Ultra DMA termination with pull-up or pull-down

7.2.4.4 PCB trace requirements for Ultra DMA

PCB trace layout is a factor in meeting the V_{sso} values in Table 4.

The longest DD(15:0) or STROBE trace for any device supporting Ultra DMA modes greater than 5 shall be 101.6 mm (4 in).

On any PCB for a host or device supporting Ultra DMA: The longest DD(15:0) trace shall be no more than 12.7 mm (0.5 in) longer than either STROBE trace as measured from the IC pin to the connector. The shortest DD(15:0) trace shall be no more than 12.7 mm (0.5 in) shorter than either STROBE trace as measured from the IC pin to the connector.

Any DD(15:0) or STROBE trace on a PCB for a host or device supporting Ultra DMA modes greater than 5 shall meet the following:

$$L / (1 + (D / H)^2) < 0.8 \quad (1)$$

where

L is the trace length in mm/25.4 (inches);

D is the center-to-center trace spacing of adjacent traces. If both traces are the same width, this is equivalent to one trace width plus the trace separation.

H is the height of the trace above a continuous, unbroken supply plane. The plane may be power or ground but if a power plane is used, it must be bypassed to the ground plane on both sides of the DD(15:0) bus near the connector ground pins and at the IC.

The units used for *D* and *H* shall be the same.

7.3 Connectors and cable asemblies

7.3.1 General

The device shall implement one of the connector options described in this subclause.

7.3.2 40-pin connector

7.3.2.1 General

The I/O connector is a 40-pin connector. The header mounted to a host or device is shown in Figure 5 and the dimensions are shown in Table 10. The connector mounted to the end of the cable is shown in

Figure 6 and the dimensions are shown in Table 11. Signal assignments on these connectors are shown in Table 12.

The pin locations are governed by the cable plug, not the receptacle. The way in which the receptacle is mounted on the printed circuit board affects the pin positions and pin 1 shall remain in the same relative position. This means the pin numbers of the receptacle may not reflect the conductor number of the plug. The header receptacle may or may not be polarized and all the signals are relative to pin 20, which is keyed.

By using the plug positions as primary, a straight cable can connect devices. As shown in Figure 7, conductor 1 on pin 1 of the plug shall be in the same relative position no matter what the receptacle numbering looks like. If receptacle numbering was followed, the cable would have to twist 180° between a device with top-mounted receptacles and a device with bottom-mounted receptacles.

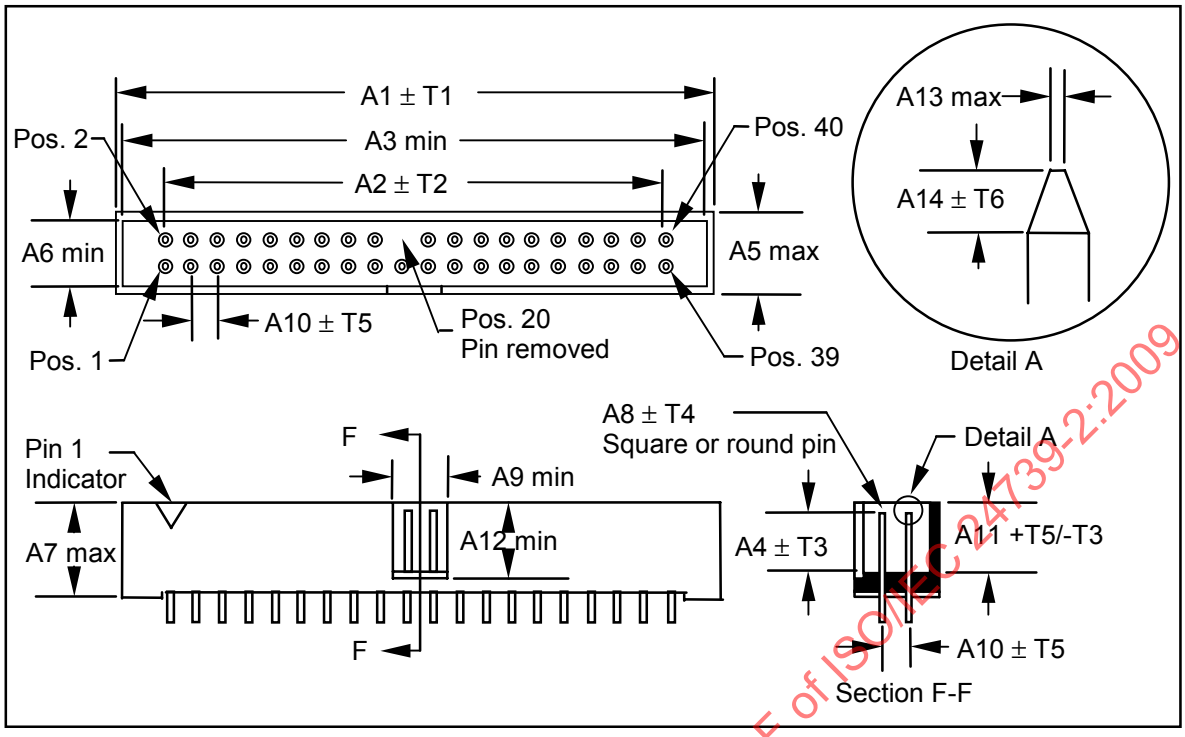


Figure 5 – Host or device 40-pin I/O header

Table 10 – Host or device 40-pin I/O header

Dimension	mm	in
A1	58.17	2.290
A2	48.26	1.900
A3	56.01	2.205
A4	5.84	0.230
A5	9.55	0.376
A6	6.22	0.245
A7	10.16	0.400
A8	0.64	0.025
A9	4.06	0.160
A10	2.54	0.100
A11	6.35	0.250
A12	6.48	0.255
A13	0.33	0.013
A14	0.58	0.023
T1	0.51	0.020
T2	0.13	0.005
T3	0.25	0.010
T4	0.03	0.001
T5	0.08	0.003
T6	0.18	0.007

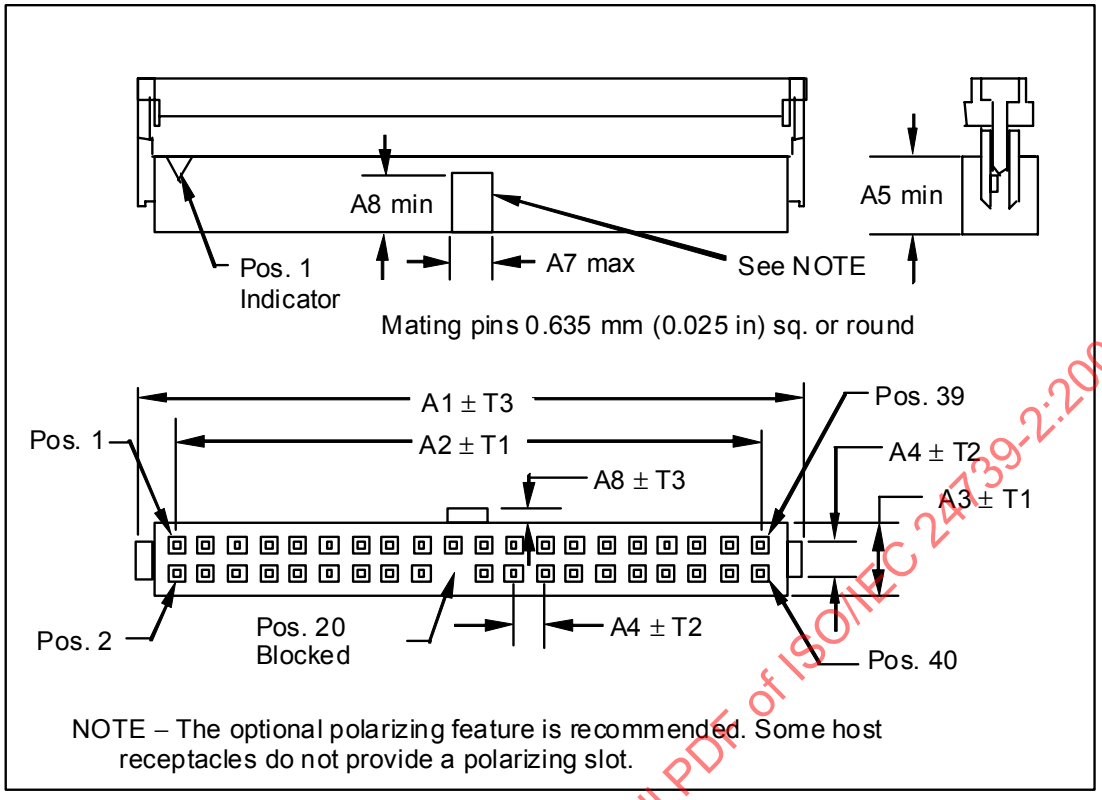


Figure 6 – 40-pin I/O cable connector

Table 11 – 40-pin I/O cable connector

Dimension	mm	in
A1	55.37	2.180
A2	48.26	1.900
A3	6.10	0.240
A4	2.54	0.100
A5	6.48	0.255
A6	4.57	0.180
A7	3.81	0.150
A8	1.27	0.050
T1	0.13	0.005
T2	0.08	0.003
T3	0.25	0.010

Table 12 – 40-pin I/O connector interface signals

Signal name	Connector contact	Conductor		Connector contact	Signal name
RESET-	1	1	2	2	Ground
DD7	3	3	4	4	DD8
DD6	5	5	6	6	DD9
DD5	7	7	8	8	DD10
DD4	9	9	10	10	DD11
DD3	11	11	12	12	DD12
DD2	13	13	14	14	DD13
DD1	15	15	16	16	DD14
DD0	17	17	18	18	DD15
Ground	19	19	20	20	(keypin)
DMARQ	21	21	22	22	Ground
DIOW-:STOP	23	23	24	24	Ground
DIOR-:HDMARDY-:HSTROBE	25	25	26	26	Ground
IORDY:DDMARDY-:DSTROBE	27	27	28	28	CSEL
DMACK-	29	29	30	30	Ground
INTRQ	31	31	32	32	Obsolete [a]
DA1	33	33	34	34	PDIAG-:CBLID-
DA0	35	35	36	36	DA2
CS0-	37	37	38	38	CS1-
DASP-	39	39	40	40	Ground

[a] Pin 32 was defined as IOCS16 in ATA-2, ANSI X3.279-1996.

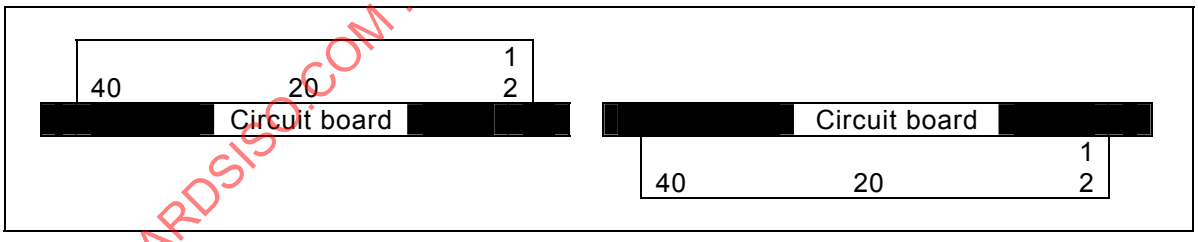


Figure 7 – 40-pin I/O header mounting

7.3.2.2 40-conductor cable

The 40-conductor cable assemby is shown in Figure 8 with dimensions in Table 13. Cable capacitance shall not exceed 35 pF.

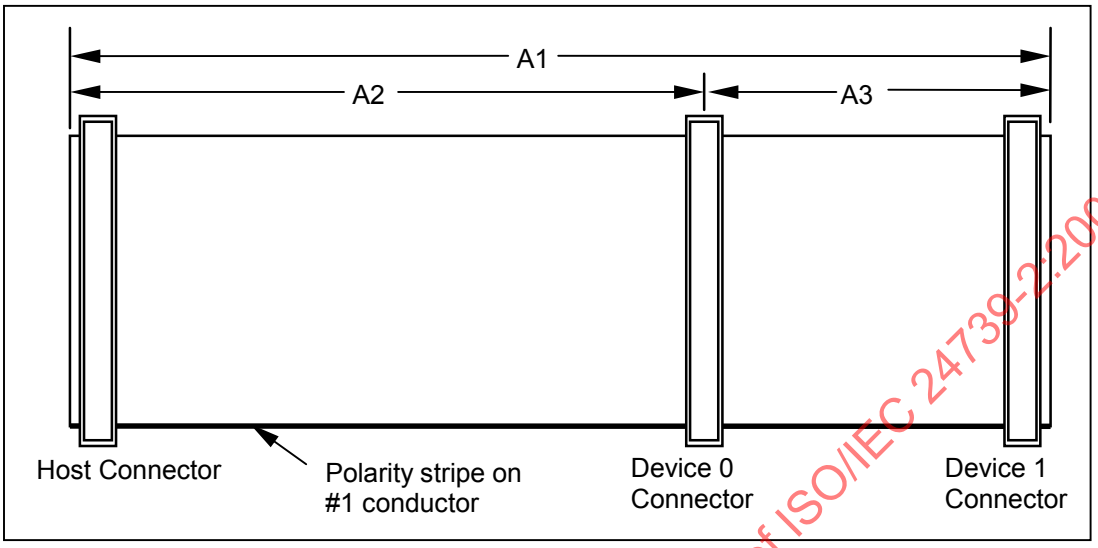


Figure 8 – 40-conductor cable configuration

Table 13 – 40-conductor cable configuration

Dimension	mm	in
1	254.00 min. 457.20 max.	10.00 min. 18.00 max.
A2	127.00 min. 304.80 max.	5.00 min. 12.00 max.
A3	127.00 min. 152.40 max.	5.00 min. 6.00 max.

7.3.2.3 80-conductor cable assembly using the 40-pin connector

To provide better signal integrity, the optional 80-conductor cable assembly is specified for use with 40-pin connectors. Use of this assembly is mandatory for systems operating at Ultra DMA modes greater than 2. The mating half of the connector is as described in 7.3.2. Every other conductor in the 80-conductor cable is connected to the ground pins in each connector.

The electrical requirements of the 80-conductor ribbon cable are shown in Table 14 and the physical requirements are described in Figure 9 and Table 15.

Figure 10 and Table 16 describe the physical dimensions of the cable assembly. The connector in the center of the cable assembly labelled Device 1 Connector is optional. The System Board connector shall have a blue base and a black or blue retainer. The Device 0 Connector shall have a black base and a black retainer. The Device 1 Connector shall have a gray base and a black or gray retainer. The cable assembly may be printed with connector identifiers.

There are alternative cable conductor to connector pin assignments depending on whether the connector attaches all even or odd conductors to ground. Table 17 shows the signal assignments for connectors that ground the even numbered conductors. Table 18 shows the signal assignments for connectors that ground the odd numbered conductors. Only one connector type, even or odd, shall be used in a given cable assembly. Connectors shall be labelled as grounding the even or odd conductors, as shown in Figure 11. Cable assemblies conforming to Table 17 are interchangable with cable assemblies conforming to Table 18.

All connectors shall have position 20 blocked to provide keying. Pin 28 in Device 1 Connector shall not be attached to any cable conductor, the connector contact may be removed to meet this requirement (see 8.2.13.3). Pin 34 in the Host Connector shall not be attached to any cable conductor and shall be attached to Ground within the connector (see 9.4).

Table 14 – 80-conductor cable electrical requirements

Conductor		0.050 92 mm^2 (30 AWG)
Ground-signal-ground		
Single ended impedance	(Ω)	70 to 90
Capacitance	(pF/ft)	13 to 22
	(pF/m)	42 to 72
Inductance	(μH)	0.08 to 0.16
Propagation delay	(ns/ft)	1.35 to 1.65
	(ns/m)	4.43 to 5.41

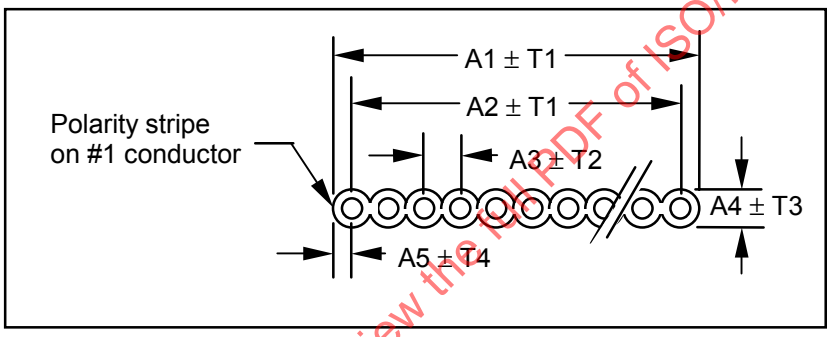


Figure 9 – 80-conductor ribbon cable

Table 15 – 80-conductor ribbon cable

Dimension	mm	in
A1	50.800	2.000
A2	50.165	1.975
A3	0.635	0.025
A4	0.685 8	0.027
A5	0.317 5	0.012 5
T1	0.127	0.005
T2	0.0406	0.001 6
T3	0.050 8	0.002
T4	0.102	0.004

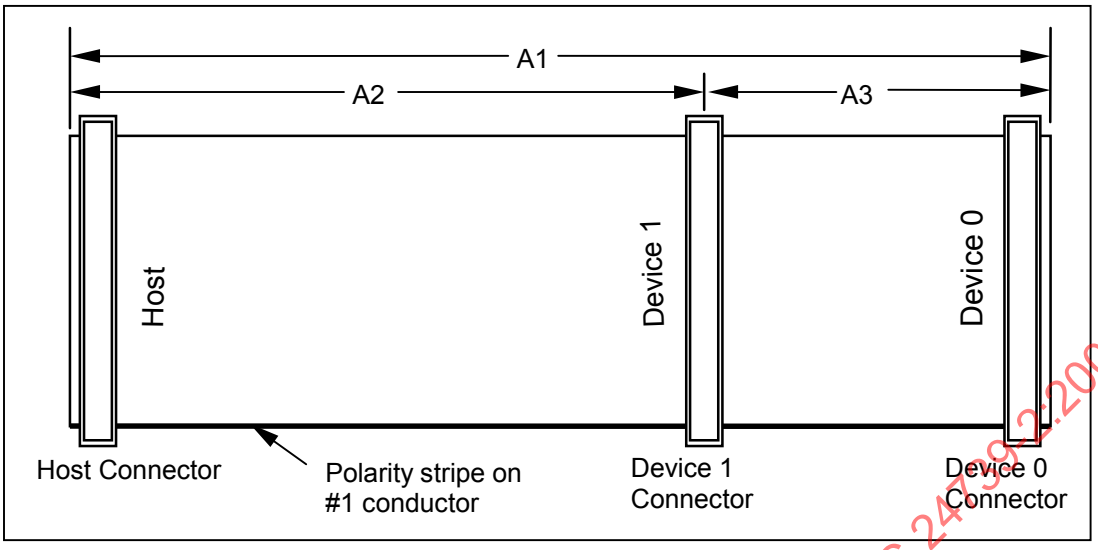


Figure 10 – 80-conductor cable configuration

Table 16 – 80-conductor cable configuration

Dimension	mm	in
A1	457.20 max.	18.00 max.
A2	127.00 min.	5.00 min.
A3	152.40 max.	6.00 max.
A2 min. shall be greater than or equal to A3.		

Table 17 – Signal assignments for connectors grounding even conductors

Signal name	Connector contact	Conductor		Signal name
RESET-	1	1	2	Ground
Ground	2	3	4	Ground
DD7	3	5	6	Ground
DD8	4	7	8	Ground
DD6	5	9	10	Ground
DD9	6	11	12	Ground
DD5	7	13	14	Ground
DD10	8	15	16	Ground
DD4	9	17	18	Ground
DD11	10	19	20	Ground
DD3	11	21	22	Ground
DD12	12	23	24	Ground
DD2	13	25	26	Ground
DD13	14	27	28	Ground
DD1	15	29	30	Ground
DD14	16	31	32	Ground
DD0	17	33	34	Ground
DD15	18	35	36	Ground
Ground	19	37	38	Ground
(keypin)	20	39	40	Ground
DMARQ	21	41	42	Ground
Ground	22	43	44	Ground
DIOW-	23	45	46	Ground
Ground	24	47	48	Ground
DIOR-	25	49	50	Ground
Ground	26	51	52	Ground
IORDY	27	53	54	Ground
CSEL	28	55	56	Ground
DMACK-	29	57	58	Ground
Ground	30	59	60	Ground
INTRQ	31	61	62	Ground
Reserved	32	63	64	Ground
DA1	33	65	66	Ground
PDIAG-	34 [a]	67	68	Ground
DA0	35	69	70	Ground
DA2	36	71	72	Ground
CS0-	37	73	74	Ground
CS1-	38	75	76	Ground
DASP-	39	77	78	Ground
Ground	40	79	80	Ground

[a] Pin 34 in the Host Connector shall not be attached to any cable conductor and shall be attached to Ground within the connector (see 9.4).

Table 18 – Signal assignments for connectors grounding odd conductors

Signal name	Conductor		Connector contact	Signal name
Ground	1	2	1	RESET-
Ground	3	4	2	Ground
Ground	5	6	3	DD7
Ground	7	8	4	DD8
Ground	9	10	5	DD6
Ground	11	12	6	DD9
Ground	13	14	7	DD5
Ground	15	16	8	DD10
Ground	17	18	9	DD4
Ground	19	20	10	DD11
Ground	21	22	11	DD3
Ground	23	24	12	DD12
Ground	25	26	13	DD2
Ground	27	28	14	DD13
Ground	29	30	15	DD1
Ground	31	32	16	DD14
Ground	33	34	17	DD0
Ground	35	36	18	DD15
Ground	37	38	19	Ground
Ground	39	40	20	(keypin)
Ground	41	42	21	DMARQ
Ground	43	44	22	Ground
Ground	45	46	23	DIOW-
Ground	47	48	24	Ground
Ground	49	50	25	DIOR-
Ground	51	52	26	Ground
Ground	53	54	27	IORDY
Ground	55	56	28	CSEL
Ground	57	58	29	DMACK-
Ground	59	60	30	Ground
Ground	61	62	31	INTRQ
Ground	63	64	32	Reserved
Ground	65	66	33	DA1
Ground	67	68	34 [a]	PDIAG-
Ground	69	70	35	DA0
Ground	71	72	36	DA2
Ground	73	74	37	CS0-
Ground	75	76	38	CS1-
Ground	77	78	39	DASP-
Ground	79	80	40	Ground

[a] Pin 34 in the Host Connector shall not be attached to any cable conductor and shall be attached to Ground within the connector (see 9.4).

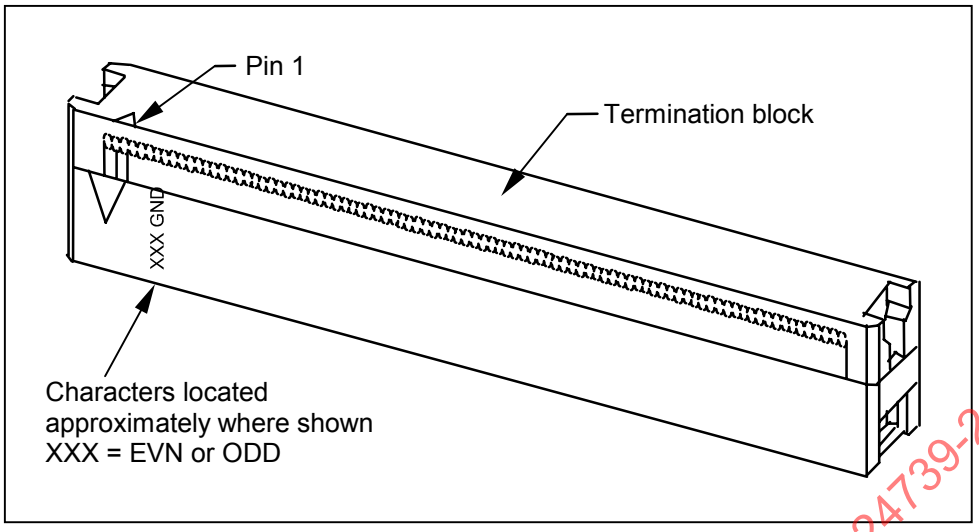


Figure 11 – Connector labeling for even or odd conductor grounding

7.3.3 4-pin power connector

7.3.3.1 General

The power connector is a 4-pin connector. The header mounted to a device is shown in Figure 12 and the dimensions are shown in Table 19. The connector mounted to the end of the cable is shown in Figure 13 and the dimensions are shown in Table 20. Pin assignments for these connectors are shown in Table 21.

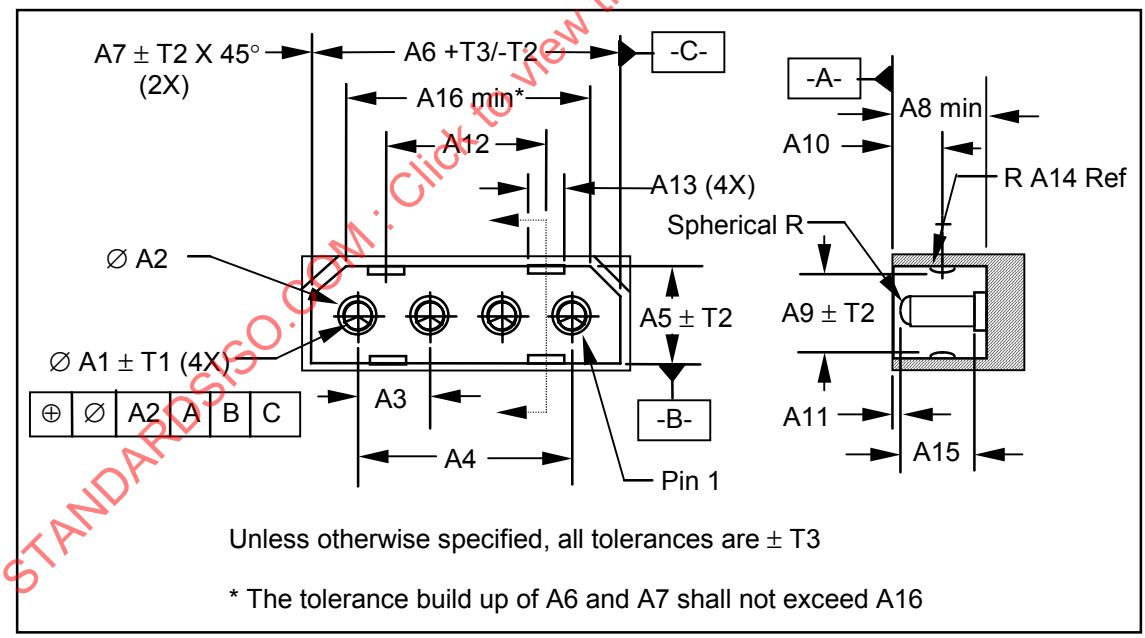


Figure 12 – Device 4-pin power header

Table 19 – Device 4-pin power header

Dimension	mm	in
A1	2.10	0.083
A2	3.50	0.138
A3	5.08	0.200
A4	15.24	0.600
A5	6.60	0.260
A6	21.32	0.839
A7	1.65	0.065
A8	7.50	0.295
A9	6.00	0.236
A10	4.95	0.195
A11	1.00	0.039
A12	11.18	0.440
A13	3.80	0.150
A14	3.00	0.118
A15	5.10	0.201
A16	17.80	0.701
T1	0.04	0.0016
T2	0.15	0.006
T3	0.25	0.010

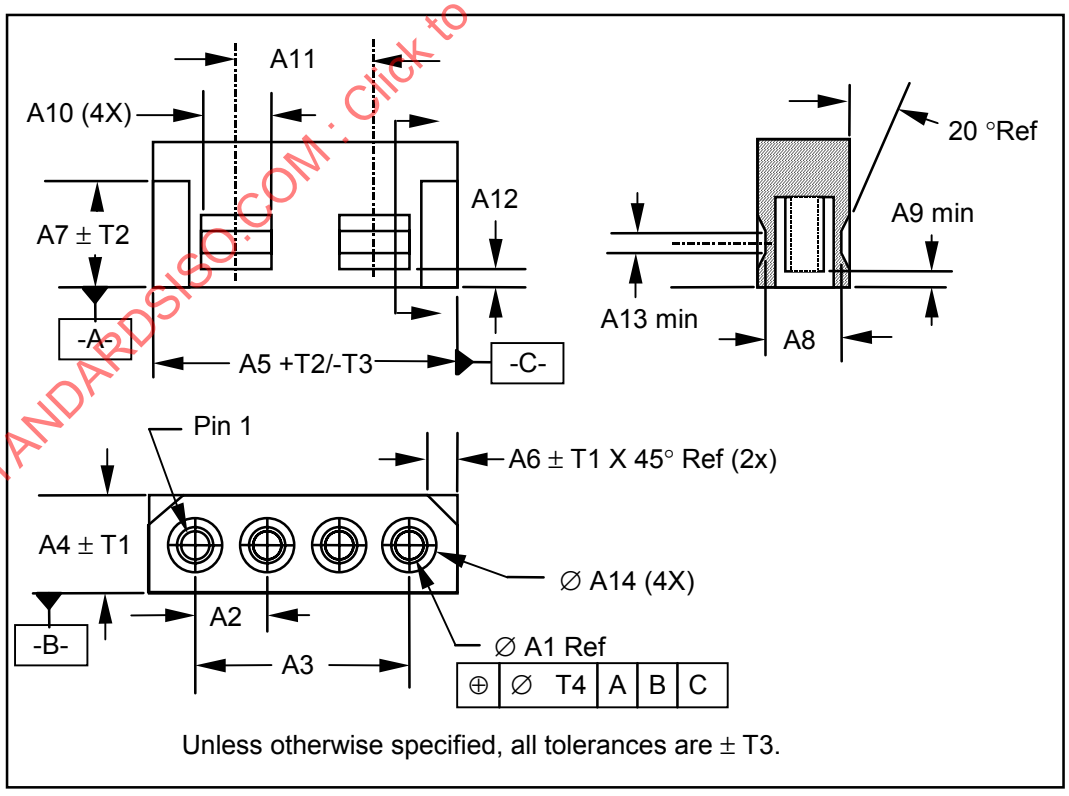


Figure 13 – 4-pin power cable connector

Table 20 – 4-pin power cable connector

Dimension	mm	in
A1	2.03	0.080
A2	5.08	0.200
A3	15.24	0.600
A4	6.35	0.250
A5	21.00	0.827
A6	1.78	0.070
A7	7.87	0.310
A8	5.51	0.217
A9	1.19	0.047
A10	5.08	0.200
A11	11.18	0.440
A12	1.19	0.047
A13	2.00	0.079
A14	4.06	0.160
T1	0.10	0.004
T2	0.15	0.006
T3	0.25	0.010
T4	0.60	0.024

Table 21 – 4-pin power connector pin assignments

Power line	Pin
+12 V	1
+12 V return	2
+5 V return	3
+5 V	4

7.3.3.2 Mating performance

Mating force should be 1.75 kg (3.85 lbs) maximum per contact.

Unmating force should be 113.5 g (0.25 lbs) minimum per contact.

7.3.4 Unitized connectors

The 40-pin I/O signal header and the 4-pin power connector may be implemented in one of two unitized connectors that provide additional pins for configuration jumpers. The dimensioning of the 40-pin I/O signal area shall be as defined in Figure 5 and the dimensioning of the 4-pin power connector area shall be as defined in Figure 12 for both unitized connectors.

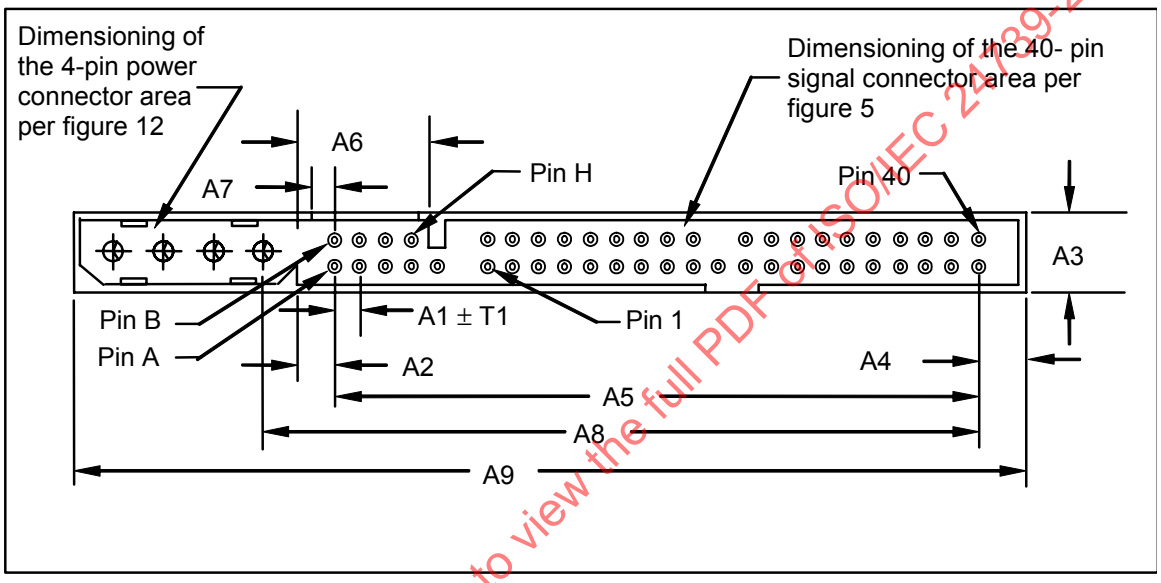
The first of the unitized connectors is shown in Figure 14 with dimensions as shown in Table 22. The jumper pins, A through I, have been assigned as follows:

- E-F - CSEL
- G-H - Master
- G-H and E-F - Master with slave present

- No jumper - Slave
- A through D - Vendor specific
- I - Reserved

The second of the unitized connectors is shown in Figure 15 with dimensions as shown in Table 23. The jumper pins, A through J, have been assigned as follows:

- A-B - CSEL
- C-D - Slave
- E-F - Master
- G through J - Vendor specific



Tolerances ±0.254 mm (0.010 in) unless otherwise specified.

Figure 14 – Unitized connector

Table 22 – Unitized connector

Dimension	mm	in
A1	2.54	0.100
A2	4.06	0.160
A3	8.40	0.331
A4	5.26	0.207
A5	63.50	2.500
A6	13.54	0.533
A7	2.54	0.100
A8	70.825	2.788
A9	95.50	3.760
T1	0.15	0.006

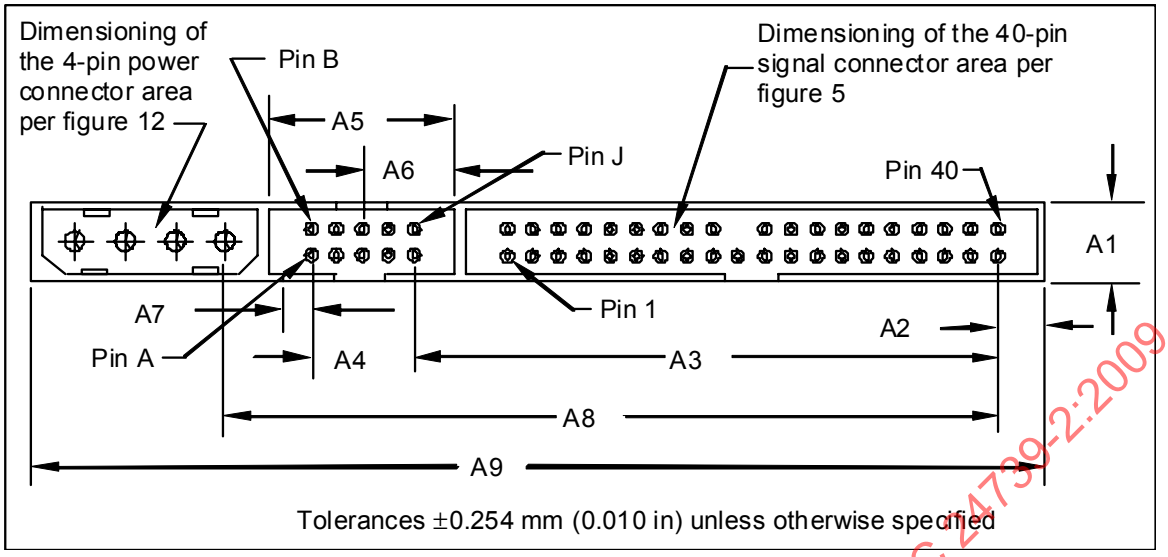


Figure 15 – Unitized connector

Table 23 – Unitized connector

Dimension	mm	in
A1	8.51	0.335
A2	5.51	0.217
A3	57.15	2.250
A4	10.16	0.400
A5	17.88	0.704
A6	8.94	0.352
A7	2.54	0.100
A8	75.29	2.964
A9	100.33	3.950

7.3.5 50-pin 65 mm (2.5 in) form factor style connector

An alternative connector is often used for 65 mm (2.5 in) or smaller devices. This connector is shown in Figure 16 with dimensions shown in Table 24. Signal assignments are shown in Table 25. Although there are 50 pins in the plug, a 44-pin mating receptacle may be used.

Pins E, F and 20 are keys and are removed.

Some devices may use pins A, B, C and D for option selection via physical jumpers. If a device uses pins A, B, C and D for device selection, when no jumper is present the device should be designated as Device 0. When a jumper is present between pins B and D, the device should respond to the CSEL signal to determine the device number.

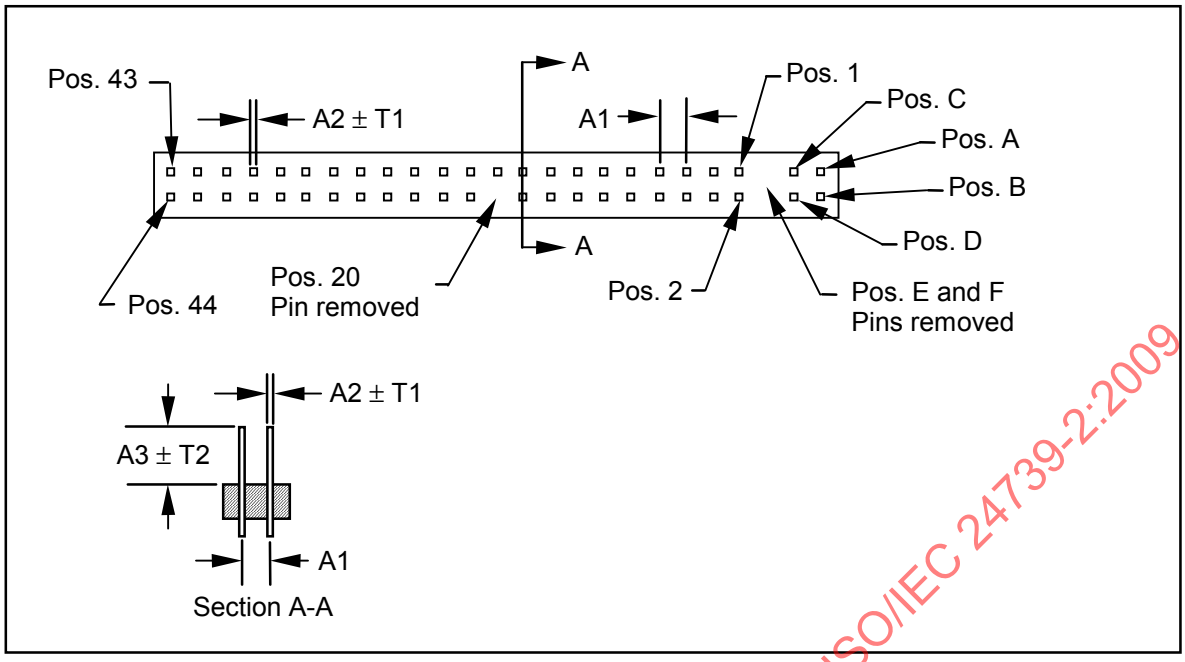


Figure 16 – 50-pin 65 mm (2.5 in) form factor style connector

Table 24 – 50-pin connector

Dimension	mm	in
A1	2.00	0.079
A2	0.50	0.020
A3	3.86	0.152
T1	0.05	0.002
T2	0.20	0.008

Table 25 – Signal assignments for 50-pin 65 mm (2.5 in) form factor style connector

Signal name	Connector contact	Conductor		Connector contact	Signal name
Option selection pins	A			B	Option selection pins
Option selection pins	C			D	Option selection pins
(keypin)	E			F	(keypin)
RESET-	1	1	2	2	Ground
DD7	3	3	4	4	DD8
DD6	5	5	6	6	DD9
DD5	7	7	8	8	DD10
DD4	9	9	10	10	DD11
DD3	11	11	12	12	DD12
DD2	13	13	14	14	DD13
DD1	15	15	16	16	DD14
DD0	17	17	18	18	DD15
Ground	19	19	20	20	(keypin)
DMARQ	21	21	22	22	Ground
DIOW-:STOP	23	23	24	24	Ground
DIOR-:HDMARDY-:HSTROBE	25	25	26	26	Ground
IORDY:DDMARDY-:DSTROBE	27	27	28	28	CSEL
DMACK-	29	29	30	30	Ground
INTRQ	31	31	32	32	Obsolete (see [a])
DA1	33	33	34	34	PDIAG-
DA0	35	35	36	36	DA2
CS0-	37	37	38	38	CS1-
DASP-	39	39	40	40	Ground
+5 V (logic)	41	41	42	42	+5 V (motor)
Ground(return)	43	43	44	44	Reserved - no connection

[a] Pin 32 was defined as IOCS16 in ATA-2, ANSI X3.279-1996.

7.3.6 68-pin PCMCIA connector

7.3.6.1 General

This subclause defines the pinouts used for the 68-pin alternative connector for the AT attachment interface. This connector is defined in the PCMCIA PC Card Standard. This subclause defines a pinout alternative that allows a device to function as an AT attachment interface compliant device, while also allowing the device to be compliant with PC Card ATA mode defined by PCMCIA. The signal protocol allows the device to identify the host interface as being 68-pin as defined in this standard or PC Card ATA.

To simplify the implementation of dual-interface devices, the 68-pin AT attachment interface maintains commonality with as many PC Card ATA signals as possible, while supporting full command and signal compliance with this standard.

The 68-pin pinout shall not cause damage or loss of data if a PCMCIA card is accidentally plugged into a host slot supporting this interface. The inversion of the RESET signal between this standard and PCMCIA interfaces prevents loss of data if the device is unable to reconfigure itself to the appropriate host interface.

7.3.6.2 Signals

This standard relies upon the electrical and mechanical characteristics of PCMCIA and unless otherwise noted, all signals and registers with the same names as PCMCIA signals and registers have the same meaning as defined in PCMCIA.

The PC Card ATA specification is used as a reference to identify the signal protocol used to identify the host interface protocol.

7.3.6.3 Signal descriptions

7.3.6.3.1 General

Any signals not defined below shall be as described in this standard, PCMCIA, or the PC Card ATA documents.

Table 26 shows the signals and relationships such as direction, as well as providing the signal name of the PCMCIA equivalent.

Table 26 – Signal assignments for 68-pin connector

Pin	Signal	Hst	Dir	Dev	PCMCIA	Pin	Signal	Hst	Dir	Dev	PCMCIA
1	Ground	x	→	x	Ground	35	Ground	x	→	x	Ground
2	DD3	x	↔	x	D3	36	CD1-	x	←	x	CD1-
3	DD4	x	↔	x	D4	37	DD11	x	↔	x	D11
4	DD5	x	↔	x	D5	38	DD12	x	↔	x	D12
5	DD6	x	↔	x	D6	39	DD13	x	↔	x	D13
6	DD7	x	↔	x	D7	40	DD14	x	↔	x	D14
7	CS0-	x	→	x	CE1-	41	DD15	x	↔	x	D15
8			→	i	A10	42	CS1-	x	→	x(1)	CE2-
9	SELATA-	x	→	x	OE-	43			←	i	VS1-
10						44	DIOR-	x	→	x	IORD-
11	CS1-	x	→	x(1)	A9	45	DIOW-	x	→	x	IOWR-
12			→	i	A8	46					

Pin	Signal	Hst	Dir	Dev	PCMCIA	Pin	Signal	Hst	Dir	Dev	PCMCIA
13						47					
14						48					
15			→	i	WE-	49					
16	INTRQ	x	←	x	READY/ IREQ-	50					
17	Vcc	x	→	x	Vcc	51	Vcc	x	→	x	Vcc
18						52					
19						53					
20						54					
21						55	M/S-	x	→	x(2)	
22			→	i	A7	56	CSEL	x	→	x(2)	
23			→	i	A6	57			←	i	VS2-
24			→	i	A5	58	RESET-	x	→	x	RESET
25			→	i	A4	59	IORDY	o	←	x(3)	WAIT-
26			→	i	A3	60	DMARQ	o	←	x(3)	INPACK-
27	DA2	x	→	x	A2	61	DMACK-	o	→	o	REG-
28	DA1	x	→	x	A1	62	DASP-	x	↔	x	BVD2/ SPKR-
29	DA0	x	→	x	A0	63	PDIAG-	x	↔	x	BVD1/ STSCHG
30	DD0	x	↔	x	D0	64	DD8	x	↔	x	D8
31	DD1	x	↔	x	D1	65	DD9	x	↔	x	D9
32	DD2	x	↔	x	D2	66	DD10	x	↔	x	D10
33		x	←	x	WP/ IOIS16	67	CD2-	x	←	x	CD2-
34	Ground	x	→	x	Ground	68	Ground	x	→	x	Ground

The following applies to the device.

a) The device shall support only one CS1- signal pin.

b) The device shall support either M/S- or CSEL but not both.

c) The device shall hold this signal negated if it does not support the function.

Key

Dir = the direction of the signal between host and device.

x in the Hst (host) column = this signal shall be supported by the Host.

x in the Dev (device) column = this signal shall be supported by the device.

i in the Dev (device) column = this signal shall be ignored by the device while in 68-pin mode.

o = this signal is optional.

Nothing in Dev column = no connection should be made to that pin.

7.3.6.3.2 CD1- (Card Detect 1)

This signal shall be grounded by the device. CD1- and CD2- are used by the host to detect the presence of the device.

7.3.6.3.3 CD2- (Card Detect 2)

This signal shall be grounded by the device. CD1- and CD2- are used by the host to detect the presence of the device.

7.3.6.3.4 CS1- (Device chip select 1)

Hosts shall provide CS1- on both the pins identified in Table 26.

Devices shall recognize only one of the two pins as CS1-.

7.3.6.3.5 DMACK- (DMA acknowledge)

This signal is optional for hosts and devices.

If this signal is supported by the host or the device, the function of DMARQ shall also be supported.

7.3.6.3.6 DMARQ (DMA request)

This signal is optional for hosts.

If this signal is supported by the host or the device, the function of DMACK- shall also be supported.

7.3.6.3.7 IORDY (I/O channel ready)

This signal is optional for hosts.

7.3.6.3.8 M/S- (Master/slave)

This signal is the inverted form of CSEL. Hosts shall support both M/S- and CSEL though devices need only support one or the other.

Hosts shall assert CSEL and M/S- prior to applying V_{CC} to the connector.

7.3.6.3.9 SELATA- (select 68-pin ATA)

This pin is used by the host to select which mode to use, PC Card ATA mode or the 68-pin mode defined in this standard. To select 68-pin ATA mode, the host shall assert SELATA- prior to applying power to the connector and shall hold SELATA- asserted.

The device shall not re-sample SELATA- as a result of either a hardware or software reset. The device shall ignore all interface signals for 19 ms after the host supplies V_{cc} within the device's voltage tolerance. If SELATA- is negated following this time, the device shall either configure itself for PC Card ATA mode or not respond to further inputs from the host.

7.3.6.4 Removability considerations

7.3.6.4.1 General

This standard supports the removability of devices that use the protocol. As removability is a new consideration for devices, several issues need to be considered with regard to the insertion or removal of devices.

NOTE If a device is compliant with the Compact Flash Association Specification, use the connector defined in the Compact Flash specification.

7.3.6.4.2 Device recommendations

The following are recommendations to device implementors:

- CS0-, CS1-, RESET- and SELATA- signals be negated on the device to prevent false selection during hot insertion.
- Ignore all interface signals except SELATA- until 19 ms after the host supplies V_{CC} within the device's voltage tolerance. This time is necessary to de-bounce the device's power-on reset sequence. Once in the 68-pin mode as defined in this standard, if SELATA- is ever negated following the 19 ms de-bounce delay time, the device disables itself until V_{CC} is removed.
- Provide a method to prevent unexpected removal of the device or media.

7.3.6.4.3 Host recommendations

The following are recommendations to host implementors:

- Connector pin sequencing to protect the device by making contact to ground before any other signal in the system.
- SELATA- to be asserted at all times.
- All devices reset and reconfigured to the same base address each time a device at that address is inserted or removed.
- The removal or insertion of a device at the same address is to be detected so as to prevent the corruption of a command.
- Provide a method to prevent unexpected removal of the device or media.

7.3.7 48 mm (1.8 in) 3.3 V parallel connector

The connector for the 48 mm (1.8 in) 3.3 V parallel form factor device is defined in Figure 17 with dimensions as defined in Table 27. Pin assignments are defined in Table 29. The host connector for the 48 mm (1.8 in) 3.3 V parallel form factor device is defined in Figure 18 with dimensions as defined in Table 28. Pin assignments are defined in Table 29.

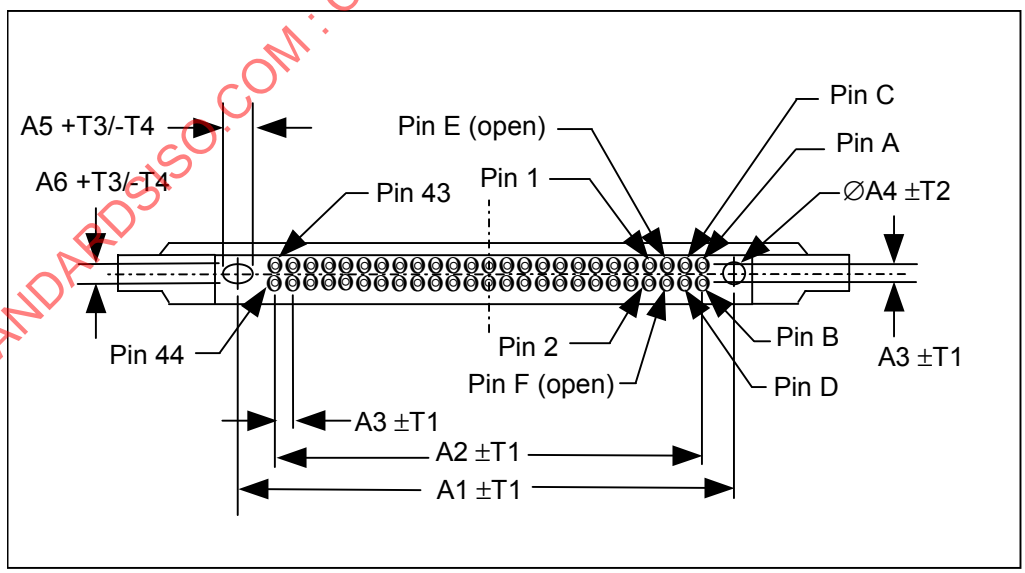


Figure 17 – 48 mm (1.8 in) 3.3 V parallel connector

Table 27 – 48 mm (1.8 in) 3.3 V parallel connector

Dimensions	Value mm	Value in
A1	36.70	1.445
A2	30.48	1.200
A3	1.27	0.050
A4	2.10	0.083
A5	2.50	0.098
A6	1.50	0.059
T1	0.15	0.006
T2	0.05	0.002
T3	0.10	0.004
T4	0.00	0.000

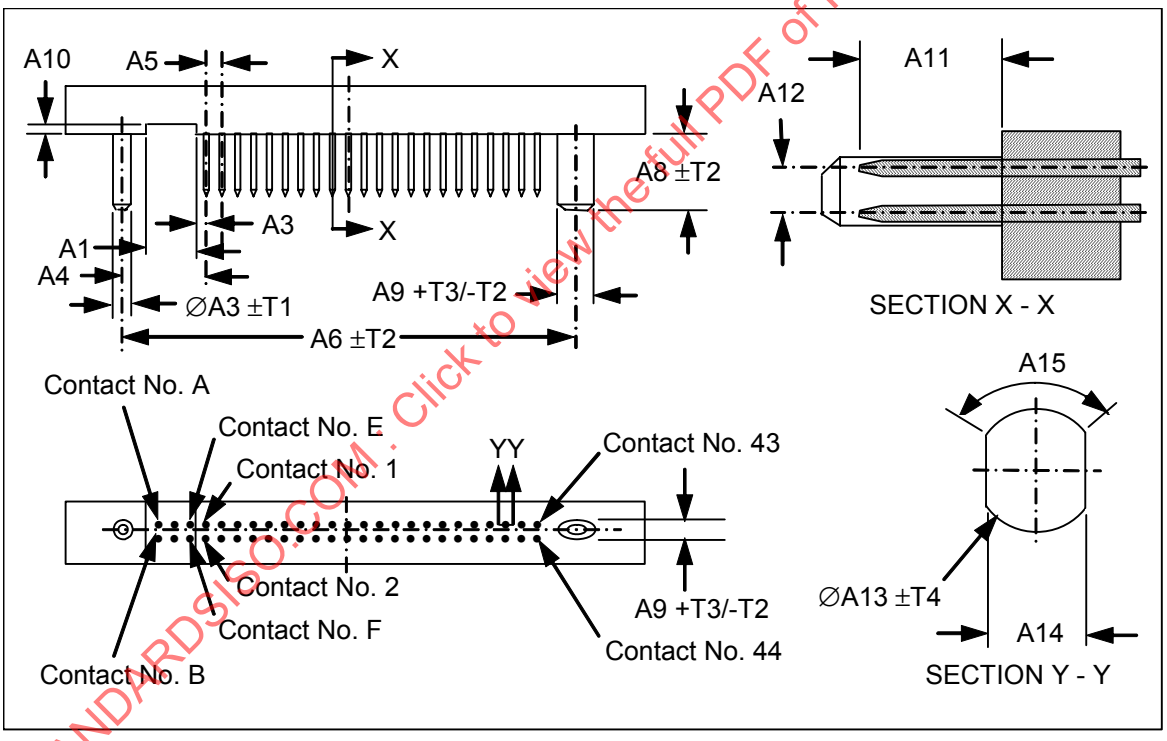


Figure 18 – 48 mm (1.8 in) 3.3 V parallel host connector

Table 28 – 48 mm (1.8 in) 3.3 V parallel host connector

Dimension	Value mm	Value in
A1	4.31	0.170
A2	1.90	0.075
A3	0.635	0.025
A4	6.92	0.272
A5	1.27	0.050
A6	36.70	1.445
A7	2.30	0.091
A8	4.50	0.177
A9	1.40	0.055
A10	0.60	0.024
A11	3.50	0.138
A12	1.27	0.050
A13	0.44	0.017
A14	0.44 max.	0.017 max.
A15	110° min.	110° min.
T1	0.05	0.002
T2	0.10	0.004
T3	0.00	0.000
T4	0.02	0.000 8

Table 29 – Pin assignments for the 48 mm (1.8 in) 3.3 V parallel connector

Pin	Signal	Pin	Signal
1	RESET-	2	Ground
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD11
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	Ground	20	No connection
21	DMARQ	22	Ground
23	DIOW-:STOP	24	Ground
25	DIOR-:HDMARDY-:HSTROBE	26	Ground
27	IORDY:DDMARDY-:DSTROBE	28	CSEL
29	DMACK-	30	Ground
31	INTRQ	32	IOCS16-
33	DA1	34	PDIAG-:CBLID-
35	DA0	36	DA2
37	CS0-	38	CS1-
39	DASP-	40	Ground
41	+3.3 V	42	−3.3 V (motor)
43	Ground	44	Reserved

7.4 Physical form factors

7.4.1 95 mm (3.5 in) form factor

7.4.1.1 General

The 95 mm (3.5 in) form factor is shown in Figure 19 with dimensions as shown in Table 30. Physical dimensions shall be measured at 20 °C ± 2 °C. The device shall not be exposed to any conditions (transit temperatures, shock, etc.) beyond the manufacturer's specified limits before measurement.

The position of four mounting holes on the bottom of the device and two mounting holes on each side of the device are specitfied.

The Device PCB may extend beyond the HDA. If it does, there is a space at the end of the HDA underneath or above the PCB overhang. This dead space shall not be encroached upon by the host system.

Except for attachment points, 0.75 mm clearance around the device is recommended for cooling airflow.

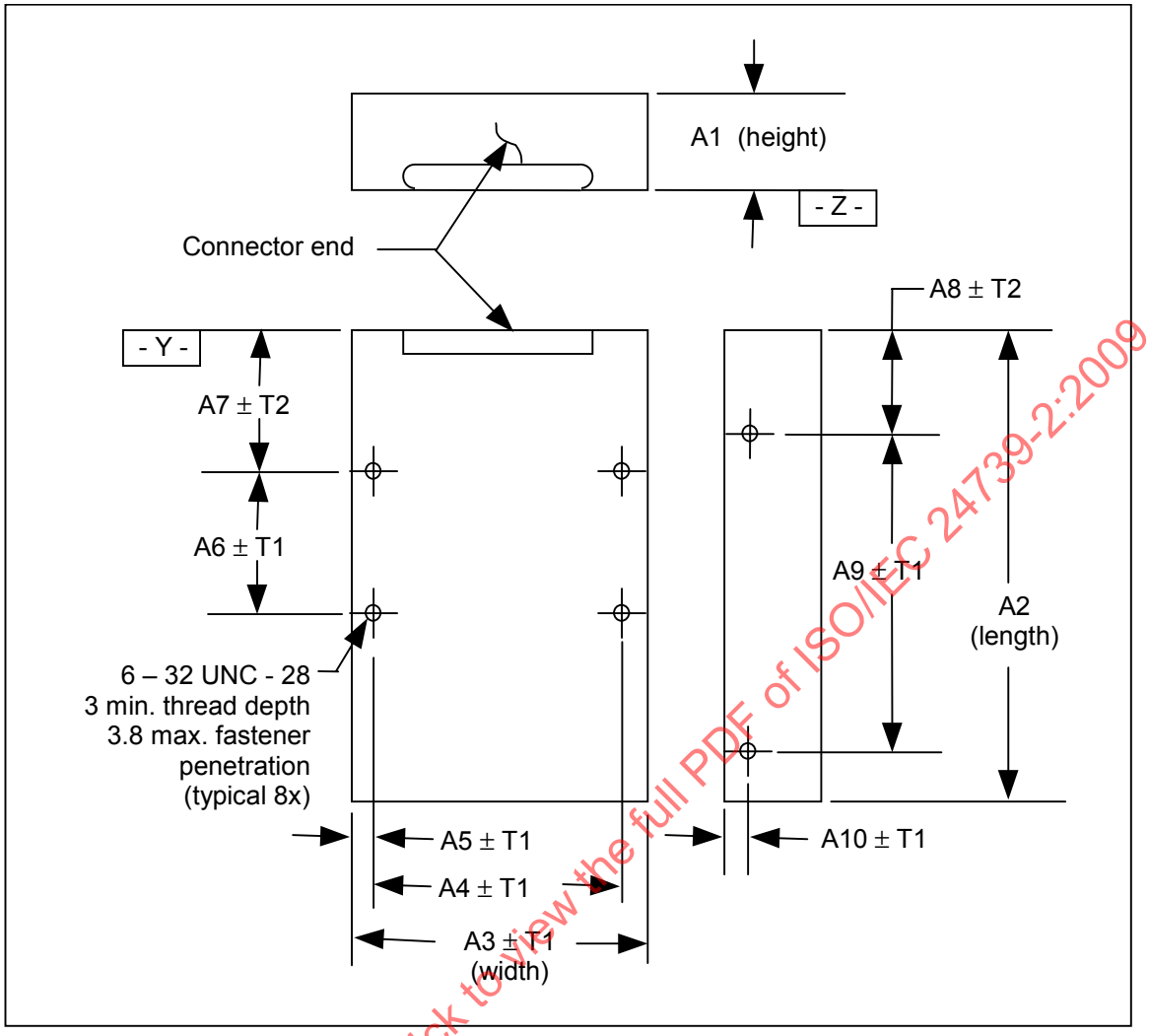


Figure 19 – 95 mm (3.5 in) form factor

Table 30 – 95 mm (3.5 in) form factor

Dimension	Value mm	Value in
A1	26.10 max	1.028 max.
A1	42.00 max	1.654 max.
A2	147.00 max	5.787 max.
A3	101.60	4.000
A4	95.25	3.750
A5	3.18	0.125
A6	44.45	1.750
A7	41.28	1.625
A8	28.50	1.122
A9	101.60	4.000
A10	6.35	0.250
T1	0.25	0.010
T2	0.50	0.020

7.4.1.2 Connector location for 95 mm (3.5 in) form factor

A 95 mm (3.5 in) form factor device may use the 40-pin signal connector (see 7.3.2) and the 4-pin power connector (see 7.3.3) or one of the Unitized connectors (see 7.3.4). The location of connectors on the 95 mm (3.5 in) form factor is not specified.

7.4.2 65 mm (2.5 in) form factor

7.4.2.1 General

The 65 mm (2.5 in) form factor is shown in Figure 20 with dimensions shown in Table 31. Physical dimensions shall be measured at 20 °C ± 2 °C. The device shall not be exposed to any conditions (transit temperatures, shock, etc.) beyond the manufacturer's specified limits before measurement.

Sixteen mounting holes are defined in Figure 20. Only eight of these mounting holes need be implemented, as shown in Figure 21.

The Device PCB may extend beyond the HDA. If it does, there is a space at the end of the HDA underneath or above the PCB overhang. This dead space shall not be encroached upon by the host system.

Except for attachment points, 0.75 mm clearance around the device is recommended for cooling airflow.

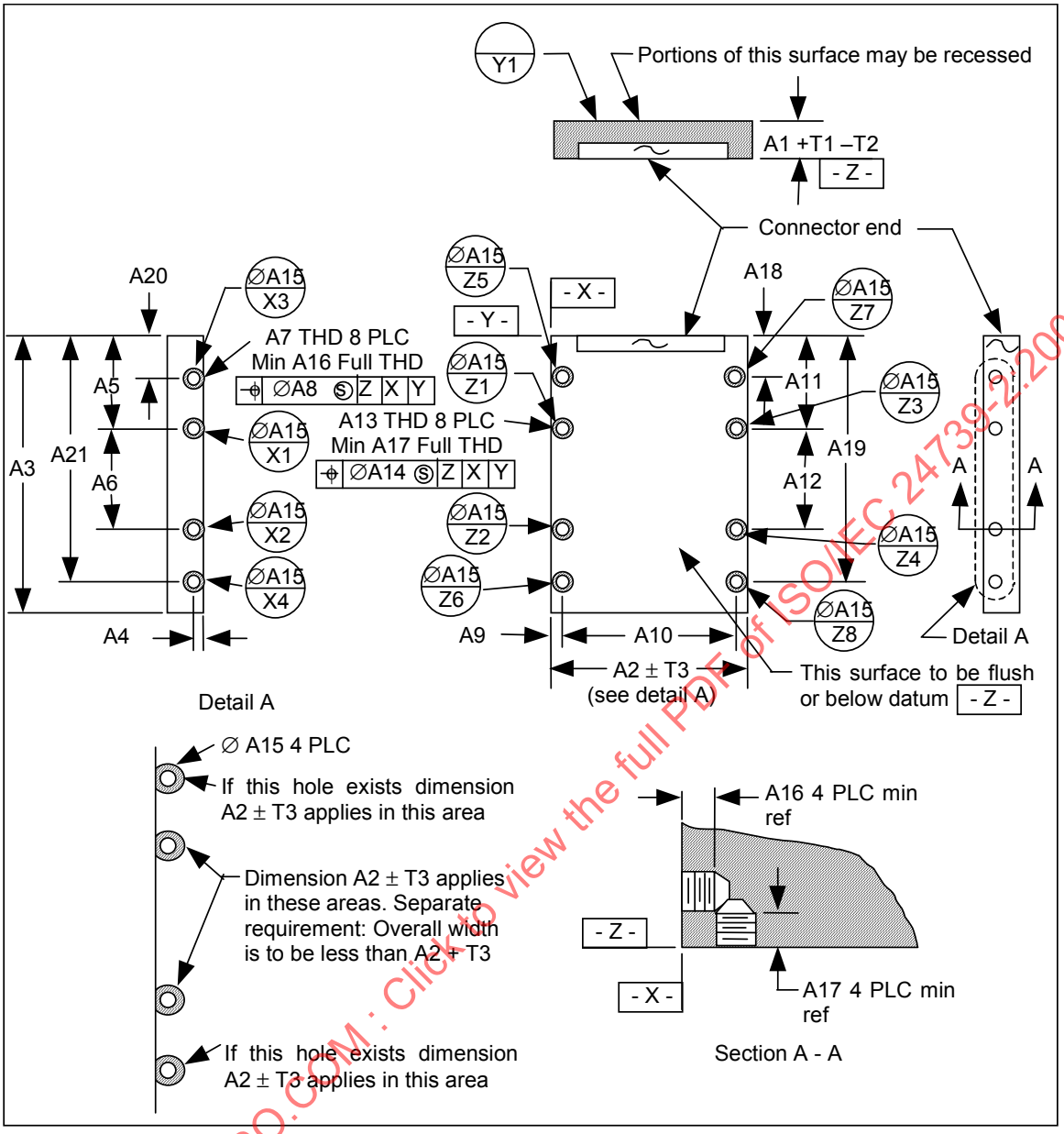


Figure 20 – 65 mm (2.5 in) form factor

Table 31 – 65 mm (2.5 in) form factor

Dimension	Value mm	Value in
A1	19.05	0.750
A1	17.00	0.669
A1	15.00	0.591
A1	12.70	0.500
A1	10.50	0.413
A1	9.50	0.374
A1	8.47	0.333
A1	7.00	0.276
A2	69.85	2.750
A3	101.85 max.	4.010 max.
A4	3.00	0.118
A5	34.93	1.375
A6	38.10	1.500
A7	M3	n/a
A8	0.50	0.020
A9	4.07	0.160
A10	61.72	2.430
A11	34/93	1.375
A12	38.10	1.500
A13	M3	n/a
A14	0.50	0.020
A15	8.00	0.315
A16	3.00 min.	0.118 min.
A17	2.50	0.098 min.
A18	14.00	0.551
A19	90.60	3.567
A20	14.00	0.551
A21	90.60	3.567
T1	0.00	0.000
T2	0.50	0.020
T3	0.25	0.010

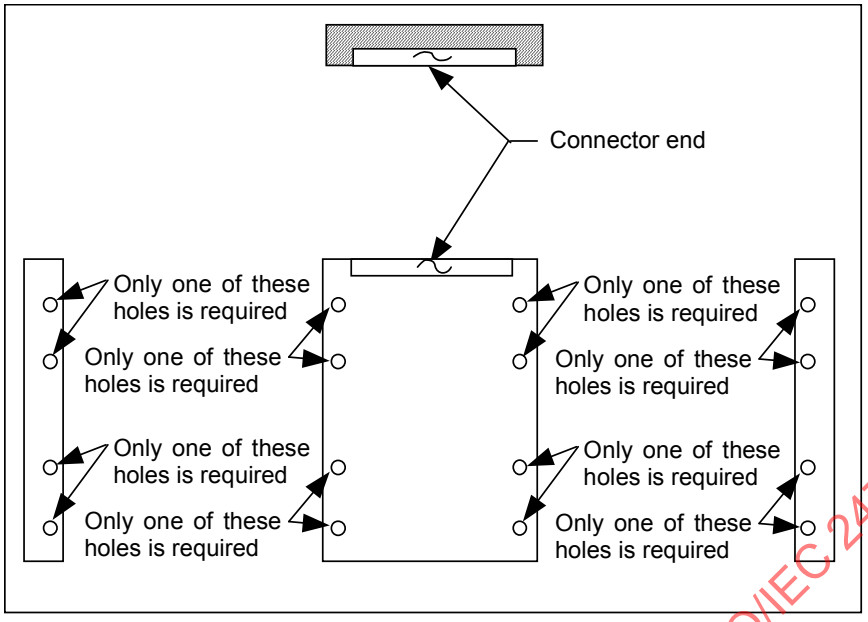


Figure 21 – 65 mm (2.5 in) form factor mounting holes

7.4.2.2 Connector location for 65 mm (2.5 in) form factor

A 65 mm (2.5 in) form factor device shall use the 50-pin connector (see 7.3.5). The location of the connector on the 65 mm (2.5 in) form factor is defined in Figure 22 with dimensions shown in Table 32.

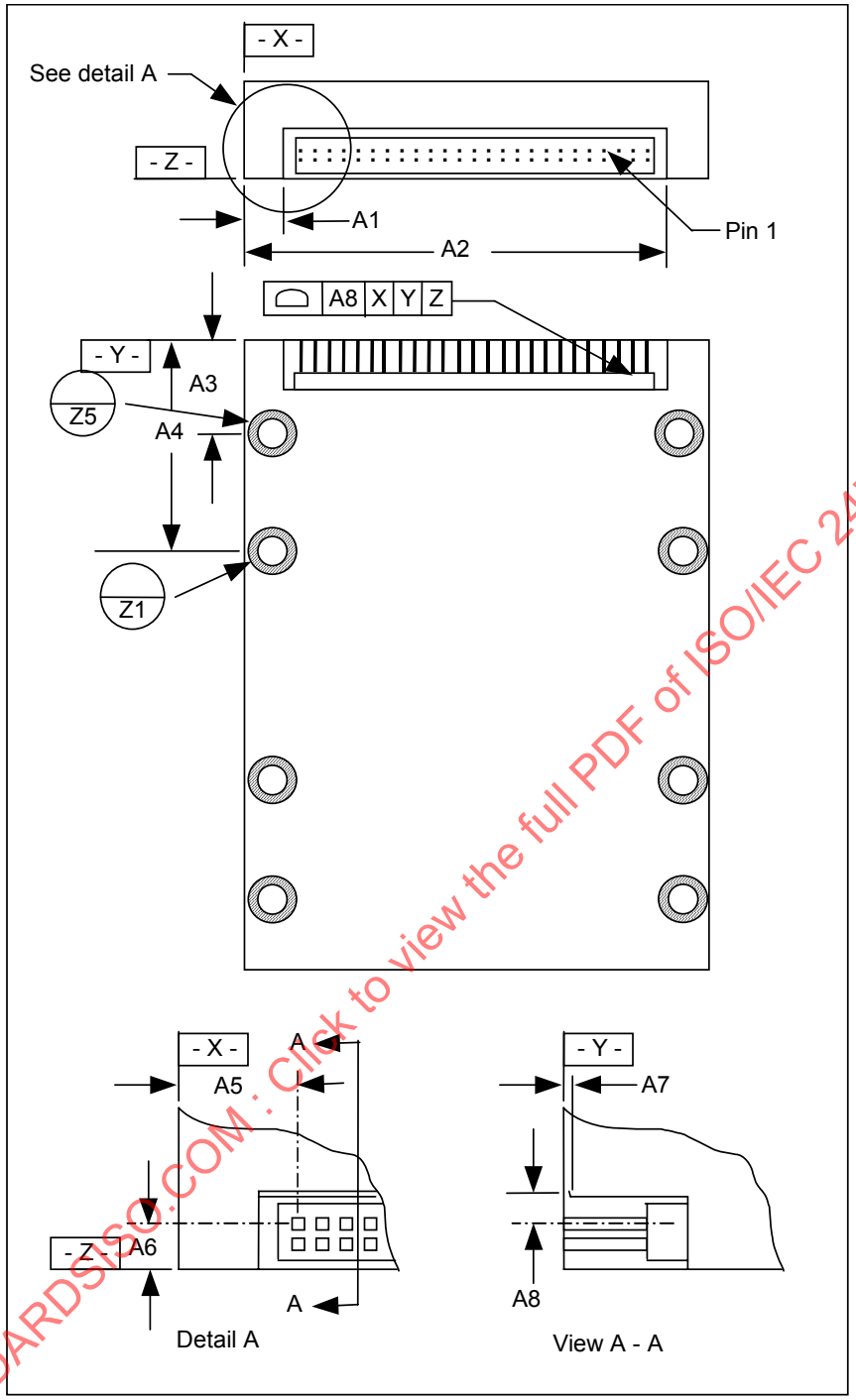


Figure 22 – 65 mm (2.5 in) form factor connector location

Table 32 – 65 mm (2.5 in) form factor connector location

Dimension	Value mm	Value in
A1	8.00 max.	0.315 max.
A2	60.20 min.	2.370 min.
A3	10.24	0.403
A4	31.17	1.227
A5	10.14	0.399
A6	3.99	0.157
A7	0.25 min.	0.010 min.
A8	1.25 min.	0.049 min.

7.4.3 48 mm (1.8 in) PCMCIA form factor

7.4.3.1 General

The 48 mm (1.8 in) PCMCIA form factor is defined in the PC Card Standard.

7.4.3.2 Connector location for 48 mm (1.8 in) PCMCIA form factor

The connector location for the 48 mm (1.8 in) PCMCIA form factor is defined in the PC Card Standard.

7.4.4 48 mm (1.8 in) 5 V parallel form factor

7.4.4.1 General

The 48 mm (1.8 in) 5 V parallel form factor is shown in Figure 23 with dimensions shown in Table 33. Physical dimensions shall be measured at 20 °C ± 2 °C. The device shall not be exposed to any conditions (transit temperatures, shock, etc.) beyond the manufacturer's specified limits before measurement.

Eight mounting holes are defined in Figure 23. All of these mounting holes shall be implemented.

The Device PCB may extend beyond the HDA. If it does, there is a space at the end of the HDA underneath or above the PCB overhang. Such dead space shall not be encroached upon by the host system.

Except for attachment points, 0.75 mm clearance around the device is recommended for cooling airflow.

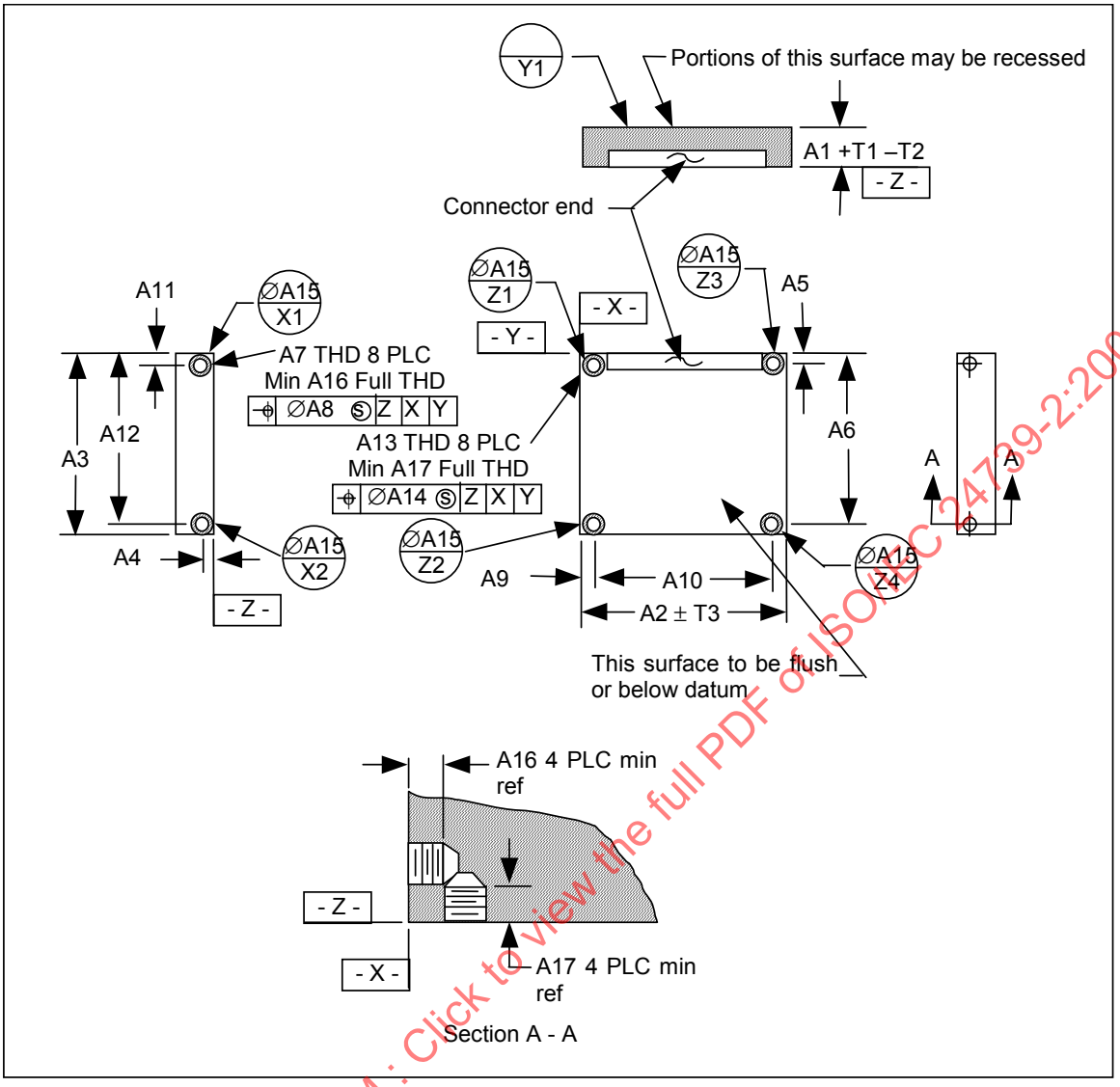


Figure 23 – 48 mm (1.8 in) 5 V parallel form factor

Table 33 – 48 mm (1.8 in) 5 V parallel form factor

Dimension	Value mm	Value in
A1	9.50	0.374
A1	7.00	0.276
A2	69.85	2.750
A3	60.00	2.362
A4	2.82	0.111
A5	2.95	0.116
A6	57.05	2.246
A7	0.00	0.000
A8	0.50	0.020
A9	3.20	0.126
A10	63.45	2.498
A11	2.95	0.116
A12	57.05	2.246
A13	0.00	0.000
A14	0.50	0.020
A15	4.00	0.157
A16	2.80	0.110
A17	2.80	0.110
T1	0.00	0.000
T2	0.50	0.020
T3	0.25	0.010

7.4.4.2 Connector location for 48 mm (1.8 in) 5 V parallel form factor

A 48 mm (1.8 in) 5 V parallel form factor device shall use the 50-pin connector (see 7.3.5). The location of the connector on the device is defined in Figure 24 with dimensions as shown in Table 34.

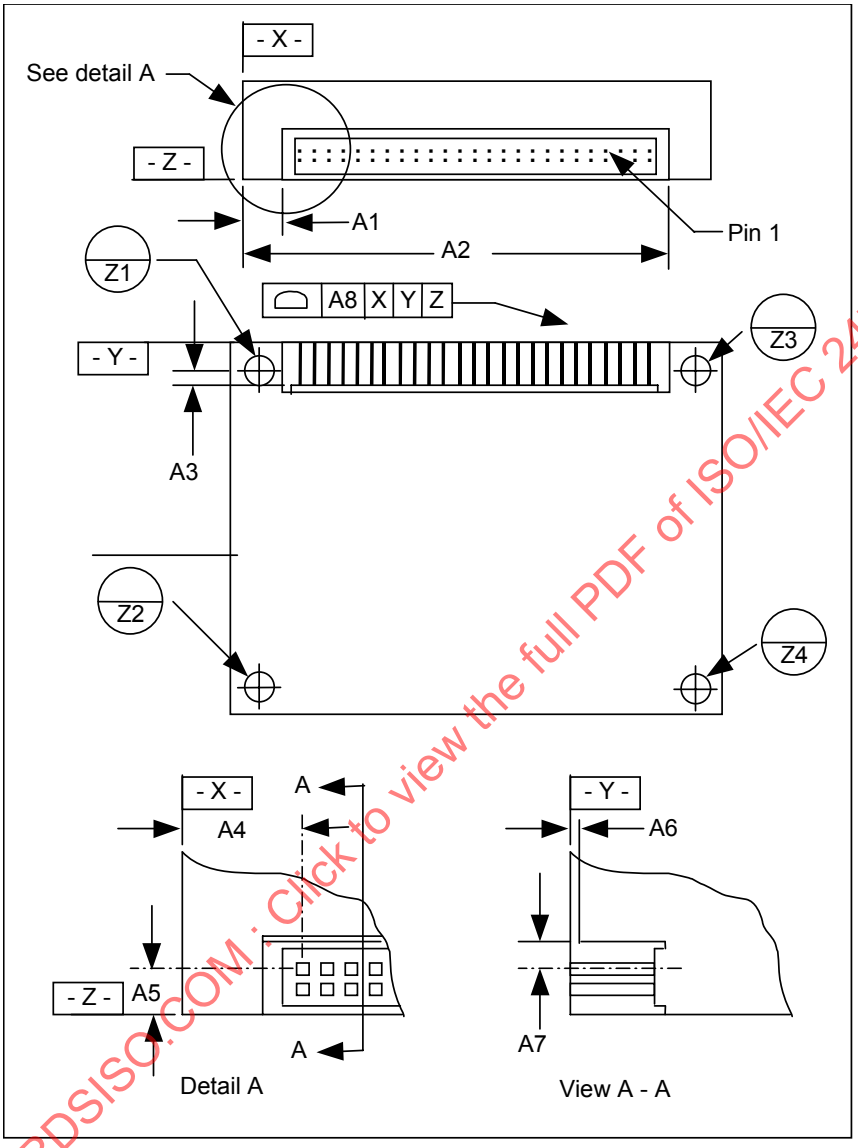


Figure 24 – 48 mm (1.8 in) 5 V parallel form factor connector location

Table 34 – 48 mm (1.8 in) 5 V parallel form factor connector location

Dimension	Value mm	Value in
A1	8.00 max.	0.315 max.
A2	60.20 min.	2.370 min.
A3	0.91	0.036
A4	10.14	0.399
A5	3.99	0.157
A6	0.25 min.	0.010 min.
A7	1.25 min.	0.049 min.

7.4.5 48 mm (1.8 in) 3.3 V parallel form factor

7.4.5.1 General

The 48 mm (1.8 in) 3.3 V parallel form factor is shown in Figure 25 with dimensions shown in Table 35. Physical dimensions shall be measured at 20 °C ± 2 °C. The device shall not be exposed to any conditions (transit temperatures, shock, etc.) beyond the manufacturer's specified limits before measurement.

The mounting area is defined in Figure 25. The device shall be guided or fixed by the interconnect or mounting area.

Except for attachment points, 0.75 mm clearance around the device is recommended for cooling airflow.

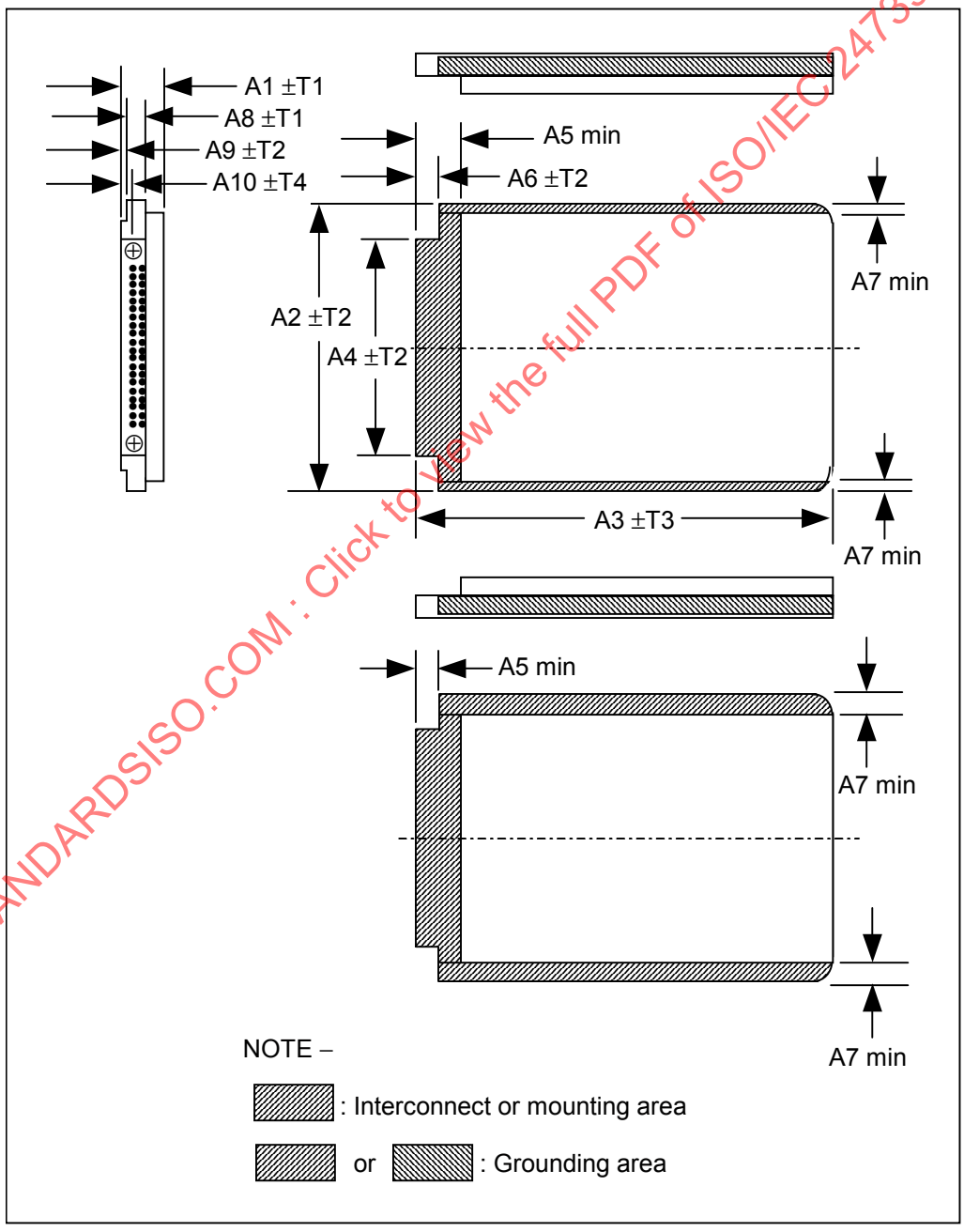


Figure 25 – 48 mm (1.8 in) 3.3 V parallel form factor

Table 35 – 48 mm (1.8 in) 3.3 V parallel form factor

Dimension	Value mm	Value in
A1	5.00	0.197
A1	8.00	0.315
A2	54.00	2.126
A3	78.50	3.090
A4	40.00	1.575
A5	6.50	0.256
A6	3.50	0.138
A7	1.50	0.059
A8	3.30	0.130
A9	0.85	0.033
A10	1.65	0.065
T1	0.15	0.006
T2	0.20	0.008
T3	0.30	0.012
T4	0.10	0.004

7.4.5.2 Connector location for 48 mm (1.8 in) 3.3 V parallel form factor

The connector location for the 48 mm (1.8 in) 3.3 V parallel connector is described in 7.3.7.

7.4.6 130 mm (5.25 in) form factor

7.4.6.1 130 mm (5.25 in) HDD form factor

7.4.6.1.1 General

The 130 mm (5.25 in) HDD form factor is shown in Figure 26 with dimensions shown in Table 36. Physical dimensions shall be measured at 20 °C ± 2 °C. The device shall not be exposed to any conditions (transit temperatures, shock, etc.) beyond the manufacturer's specified limits before measurement.

The position of four mounting holes on the bottom of the device and four mounting holes on each side of the device are specitfied.

Except for attachment points, 0.75 mm clearance around the device is recommended for cooling airflow.

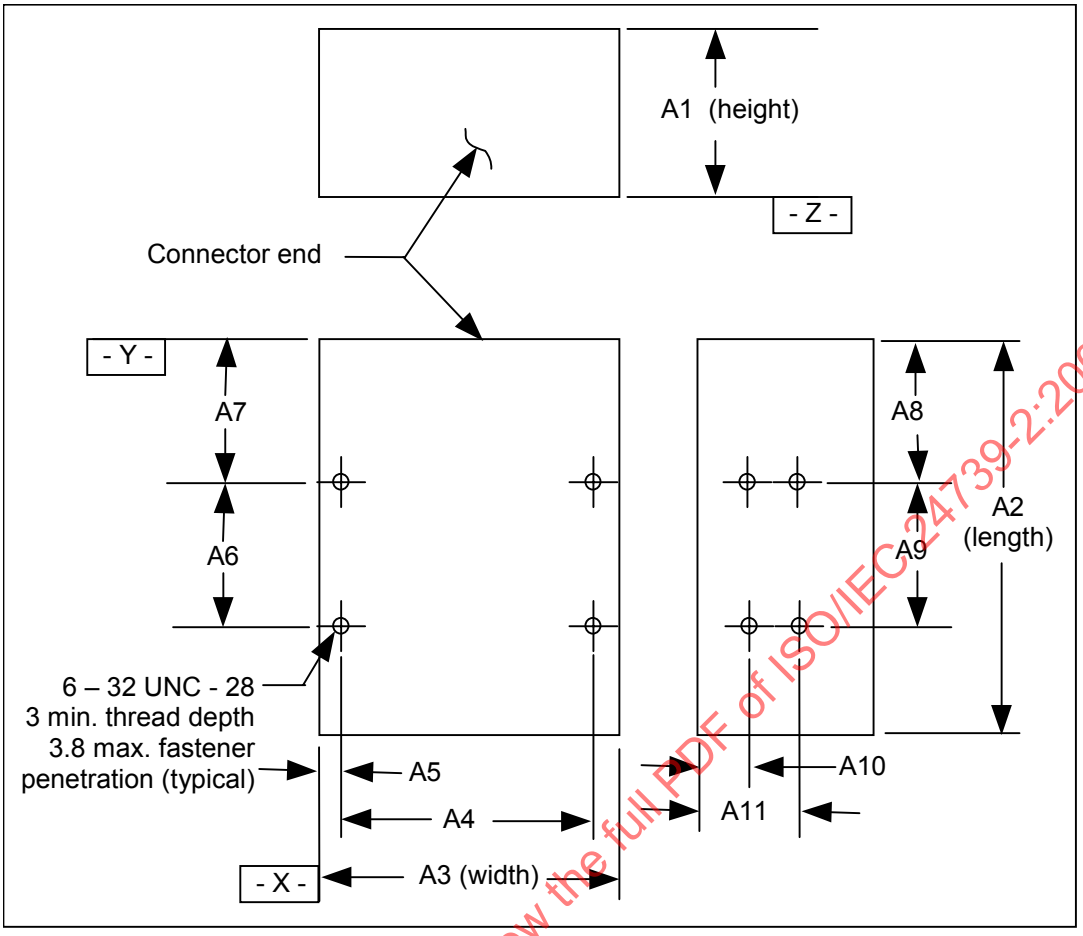


Figure 26 – 130 mm (5.25 in) HDD form factor

Table 36 – 130 mm (5.25 in) HDD form factor

Dimension	Value mm	Value in
A1	82.55 max.	3.250 max.
A2	204.72	8.060
A3	146.05	5.750
A4	139.70	5.500
A5	3.05	0.120
A6	79.24	3.120
A7	80.30	3.161
A8	80.20	3.157
A9	79.24	3.120
A10	9.91	0.390
A11	21.84	0.860

7.4.6.1.2 130 mm (5.25 in) HDD form factor connector location

A 130 mm (5.25 in) HDD form factor device may use the 40-pin signal connector (see 7.3.2) and the 4-pin power connector (see 7.3.3) or one of the unitized connectors (see 7.3.4). The location of connectors on the 130 mm (5.25 in) HDD form factor is not specified.

7.4.6.2 130 mm (5.25 in) CD-ROM form factor

7.4.6.2.1 General

The 130 mm (5.25 in) CD-ROM form factor is shown in Figure 27 with dimensions as shown in Table 37. Physical dimensions shall be measured at 20 °C ± 2 °C. The device shall not be exposed to any conditions (transit temperatures, shock, etc.) beyond the manufacturer's specified limits before measurement.

The position of four mounting holes on the bottom of the device and four mounting holes on each side of the device are specified.

Except for attachment points, 0.75 mm clearance around the device is recommended for cooling airflow.

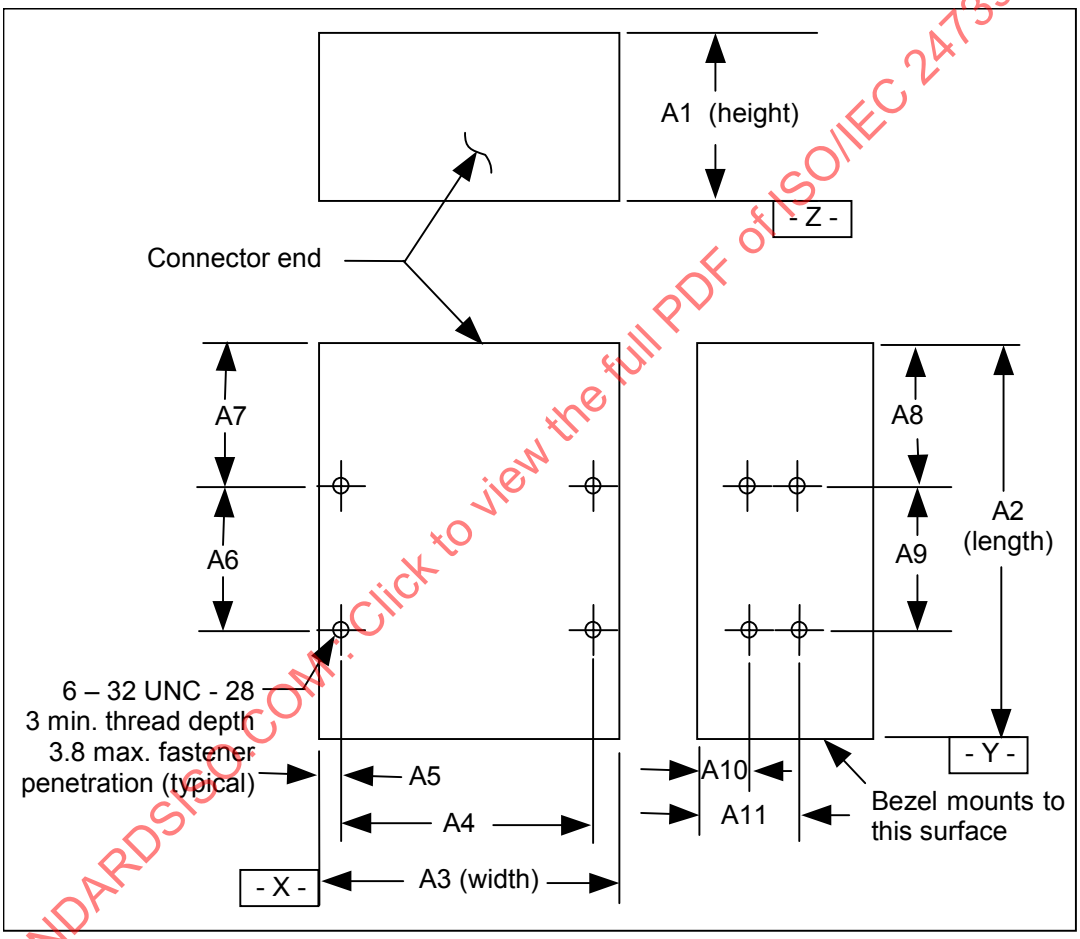


Figure 27 – 130 mm (5.25 in) CD-ROM form factor

Table 37 – 130 mm (5.25 in) CD-ROM form factor

Dimension	Value mm	Value in
A1	82.50t max	3.250 max.
A1	41.50 max.	1.634 max.
A1	25.90 max.	1.020 max.
A2	206.00	8.110
A3	146.00	5.748
A4	139.70	5.500
A5	3.15	0.124
A6	79.20	3.118
A7	52.40	2.063
A8	52.40	2.063
A9	79.20	3.118
A10	10.00	0.394
A11	21.80	0.858

7.4.6.2.2 130 mm (5.25 in) CD-ROM form factor connector location

A 130 mm (5.25 in) CD-ROM form factor device shall use the 40-pin signal connector (see 7.3.2) and the 4-pin power connector (see 7.3.3). The location of connectors of these connectors as well as the additional audio connectors is shown in Figure 28.

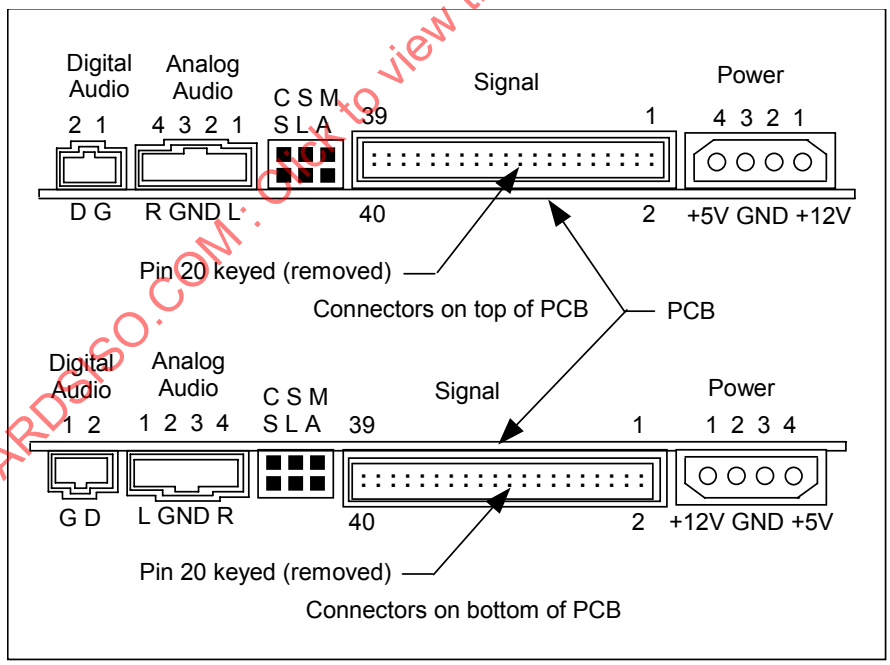


Figure 28 – 130 mm (5.25 in) CD-ROM connector location

8 Parallel interface signal assignments and descriptions

8.1 Signal summary

The physical interface consists of receivers and drivers communicating through a set of conductors using an asynchronous interface protocol. Table 38 defines the signal names. For connector descriptions, see 7.3. For driver and termination definition, see 7.2.3. For signal protocol and timing, see Clause 11 and Clause 12.

Table 38 – Interface signal name assignments

Description	Host	Dir	Dev	Acronym
Cable select		(See [a])		CSEL
Chip select 0			→	CS0-
Chip select 1			→	CS1-
Data bus bit 0		↔		DD0
Data bus bit 1		↔		DD1
Data bus bit 2		↔		DD2
Data bus bit 3		↔		DD3
Data bus bit 4		↔		DD4
Data bus bit 5		↔		DD5
Data bus bit 6		↔		DD6
Data bus bit 7		↔		DD7
Data bus bit 8		↔		DD8
Data bus bit 9		↔		DD9
Data bus bit 10		↔		DD10
Data bus bit 11		↔		DD11
Data bus bit 12		↔		DD12
Data bus bit 13		↔		DD13
Data bus bit 14		↔		DD14
Data bus bit 15		↔		DD15
Device active or slave (Device 1) present		(See [a])		DASP-
Device address bit 0			→	DA0
Device address bit 1			→	DA1
Device address bit 2			→	DA2
DMA acknowledge			→	DMACK-
DMA request	←			DMARQ
Interrupt request	←			INTRQ
I/O read			→	DIOR-
DMA ready during Ultra DMA data-in bursts			→	HDMARDY-
Data strobe during Ultra DMA data-out bursts			→	HSTROBE

Description	Host	Dir	Dev	Acronym
I/O ready	←			IORDY
DMA ready during Ultra DMA data-out bursts	←			DDMARDY-
Data strobe during Ultra DMA data-in bursts	←			DSTROBE
I/O write			→	DIOW-
Stop during Ultra DMA data bursts			→	STOP
Passed diagnostics		(See [a])		PDIAG-
Cable assembly type identifier		(See [a])		CBLID-
Reset			→	RESET-

[a] See signal descriptions in this standard and annex A of ISO/IEC 24739-1:2008 for information on the source of these signals.

8.2 Signal descriptions

8.2.1 CS(1:0)- (Chip select)

These are the chip select signals from the host used to select the Command Block or Control Block registers (see Clause 10). When DMACK- is asserted, CS0- and CS1- shall be negated and transfers shall be 16 bits wide.

8.2.2 DA(2:0) (Device address)

This is the 3-bit binary coded address asserted by the host to access a register or data port in the device (see Clause 10).

8.2.3 DASP- (device active, device 1 present)

During the reset protocol, DASP- shall be asserted by Device 1 to indicate that the device is present. At all other times, DASP- may be asserted by the selected active device.

8.2.4 DD(15:0) (Device data)

This is an 8- or 16-bit bi-directional data interface between the host and the device. DD(7:0) are used for 8-bit register transfers. Data transfers are 16-bits wide except for CFA devices that implement 8-bit data transfers.

8.2.5 DIOR-:HDMARDY-:HSTROBE (Device I/O read:Ultra DMA ready:Ultra DMA data strobe)

DIOR- is the strobe signal used by the host to read device registers or the Data port. Data is tranferred on the negation of this signal.

HDMARDY- is a flow control signal for Ultra DMA data-in bursts. This signal is asserted by the host to indicate to the device that the host is ready to receive Ultra DMA data-in bursts. The host may negate HDMARDY- to pause an Ultra DMA data-in burst.

HSTROBE is the data-out strobe signal from the host for an Ultra DMA data-out burst. Both the rising and falling edge of HSTROBE latch the data from DD(15:0) into the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.

8.2.6 DIOW-:STOP (Device I/O write:Stop Ultra DMA burst)

DIOW- is the strobe signal used by the host to write device registers or the Data port. Data is tranferred on the negation of this signal.

DIOW- shall be negated by the host prior to initiation of an Ultra DMA burst. STOP shall be negated by the host before data is transferred in an Ultra DMA burst. Assertion of STOP by the host during an Ultra DMA burst signals the termination of the Ultra DMA burst.

8.2.7 DMACK- (DMA acknowledge)

This signal shall be used by the host in response to DMARQ to initiate DMA transfers. For Multiword DMA transfers, the DMARQ/DMACK- handshake is used to provide flow control during the transfer. For Ultra DMA, the DMARQ/DMACK- handshake is used to indicate when the function of interface signals changes.

When DMACK- is asserted, CS0- and CS1- shall not be asserted and transfers shall be 16 bits wide.

8.2.8 DMARQ (DMA request)

This signal, used for DMA data transfers between host and device, shall be asserted by the device when the device is ready to transfer data to or from the host. For Mulitword DMA transfers, the direction of data transfer is controlled by DIOR- and DIOW-. This signal is used in a handshake manner with DMACK-, i.e., the device shall wait until the host asserts DMACK- before negating DMARQ and re-asserting DMARQ if there is more data to transfer. For Multiword DMA transfers, the DMARQ/DMACK- handshake is used to provide flow control during the transfer. For Ultra DMA, the DMARQ/DMACK- handshake is used to indicate when the function of interface signals changes.

This signal shall be released when the device is not selected.

See 9.2 and 9.3.

8.2.9 INTRQ (Device interrupt)

This signal is used by the selected device to interrupt the host system when Interrupt Pending is set. When the nIEN bit is cleared to zero and the device is selected, INTRQ shall be enabled through a tri-state buffer. When the nIEN bit is set to one or the device is not selected, the INTRQ signal shall be released.

When asserted, this signal shall be negated by the device within 400 ns of the negation of DIOR- that reads the Status register to clear Interrupt Pending. When asserted, this signal shall be negated by the device within 400 ns of the negation of DIOW- that writes the Command register to clear Interrupt Pending.

When the device is selected by writing to the Device register while Interrupt Pending is set, INTRQ shall be asserted within 400 ns of the negation of DIOW- that writes the Device register. When the device is deselected by writing to the Device register while Interrupt Pending is set, INTRQ shall be released within 400 ns of the negation of DIOW- that writes the Device register.

For devices implementing the Overlapped feature set, if INTRQ assertion is being disabled using nIEN at the same instant that the device asserts INTRQ, the minimum pulse width shall be at least 40 ns.

This signal shall be released when the device is not selected.

8.2.10 IORDY:DDMARDY-:DSTROBE (I/O channel ready:Ultra DMA ready:Ultra DMA data strobe)

IORDY is negated to extend the host transfer cycle of any host register access (read or write) when the device is not ready to respond to a data transfer request. If the device requires that

the host transfer cycle time be extended for PIO modes 3 and above, the device shall use IORDY. Hosts that use PIO modes 3 and above shall support IORDY.

DDMARDY- is a flow control signal for Ultra DMA data-out bursts. This signal is asserted by the device to indicate to the host that the device is ready to receive Ultra DMA data-out bursts. The device may negate DDMARDY- to pause an Ultra DMA data-out burst.

DSTROBE is the data-in strobe signal from the device for an Ultra DMA data-in burst. Both the rising and falling edge of DSTROBE latch the data from DD(15:0) into the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-in burst.

This signal shall be released when the device is not selected.

8.2.11 PDIAG-:CBLID- (passed diagnostics: cable assembly type identifier)

PDIAG- shall be asserted by Device 1 to indicate to Device 0 that Device 1 has completed diagnostics (see Clause 11).

The host may sample CBLID- after a power-on or hardware reset in order to detect the presence of an 80-conductor cable assembly by performing the following steps.

a) Wait until the power-on or hardware reset protocol is complete for all devices on the cable; remember which devices are present for the last step.

b) If Device 1 is not present, go to step d).

c) Issue IDENTIFY DEVICE or IDENTIFY PACKET DEVICE to Device 1. From the information returned, save word 80 and word 93 for the last step.

NOTE 1 Word 80 bit 3 indicates compliance with ATA-3 or subsequent standards and word 93 bits (15:13) indicate support of and results from sampling CBLID- at the device.

d) Issue IDENTIFY DEVICE or IDENTIFY PACKET DEVICE to Device 0. From the information returned, save Word 93 for the last step.

NOTE 2 Word 93 bits (15:13) indicate support of and results from sampling CBLID- at the device.

e) Detect the state of the CBLID- signal at the host connector and save the result for the last step.

NOTE 3 Any device compliant with ATA-3 or subsequent standards releases PDIAG- no later than after the first command following a power-on or hardware reset sequence and will not interfere with host detection of CBLID- in this step. Some devices claiming compliance with ATA-3 or subsequent standards are known to continue to assert CBLID-:PDIAG- which sometimes causes a 40-conductor cable assembly to be detected as an 80-conductor cable assembly.

f) Look up the output in Table 39 based on the inputs saved from steps a), c), d) and e).

Table 39 – Cable type identification

Inputs				Output
Sensed CBLID-	**Device 1 Word 80 bit 3**	**Device 1 Word 93 bits (15:13)**	**Device 0 Word 93 bits (15:13)**	**Cable conductors**
High	X	XXX	XXX	40
Low	Device absent	Device absent	00X or 1XX	80
Low	Device absent	Device absent	010	(See [b])
Low	Device absent	Device absent	011	80
Low	0	00X or 1XX	Device absent	(See [a])
Low	0	00X or 1XX	00X or 1XX	(See [a])
Low	0	00X or 1XX	010	(See [b])
Low	0	00X or 1XX	011	80
Low	0	010	Device absent	(See [b])
Low	0	010	XXX	(See [b])
Low	0	011	Device absent	80
Low	0	011	00X or 1XX	80
Low	0	011	010	(See [b])
Low	0	011	011	80
Low	1	00X or 1XX	Device absent	80
Low	1	00X or 1XX	00X or 1XX	80
Low	1	00X or 1XX	010	(See [b])
Low	1	00X or 1XX	011	80
Low	1	010	Device absent	(See [b])
Low	1	010	XXX	(See [b])
Low	1	011	Device absent	80
Low	1	011	00X or 1XX	80
Low	1	011	010	(See [b])
Low	1	011	011	80

NOTE X represents a don't-care input.

[a] Host cannot determine cable type due to insufficient information. For these cases, host should not use Ultra DMA modes higher than mode 2 without using other means to confirm presence of 80-conductor cable.

[b] Host cannot determine cable type due to conflicting information. For these cases, host should not use Ultra DMA modes higher than mode 2 without using other means to confirm presence of 80-conductor cable.

See Annex A of ISO/IEC 24739-1 for a description of the non-standard device determination of cable type.

8.2.12 RESET- (Hardware reset)

This signal, referred to as hardware reset, shall be used by the host to reset the device (see 11.2).

NOTE While a minimum slew rate is not specified, some hosts assert RESET- with an extremely slow rise time when powering up. This may cause some devices to fail to recognize the assertion. Such hosts should negate then reassert RESET- once power has been established.

8.2.13 CSEL (cable select)

8.2.13.1 General

If CSEL is enabled in the device, the device is configured as either Device 0 or Device 1 depending upon the value of CSEL.

- if CSEL is negated, the device number is 0.
- if CSEL is asserted, the device number is 1.

The state of this signal may be sampled at any time by the device.

CSEL shall be grounded by the host.

8.2.13.2 CSEL with 40-conductor cable

Special cabling may be used to selectively ground CSEL. CSEL of Device 0 is connected to the CSEL conductor in the cable and is grounded, thus allowing the device to recognize itself as Device 0. CSEL of Device 1 is not connected to the CSEL conductor, thus the device recognizes itself as Device 1. If a single device is configured at the end of the cable using CSEL, a Device 1 only configuration results. See Figure 29 and Figure 30.

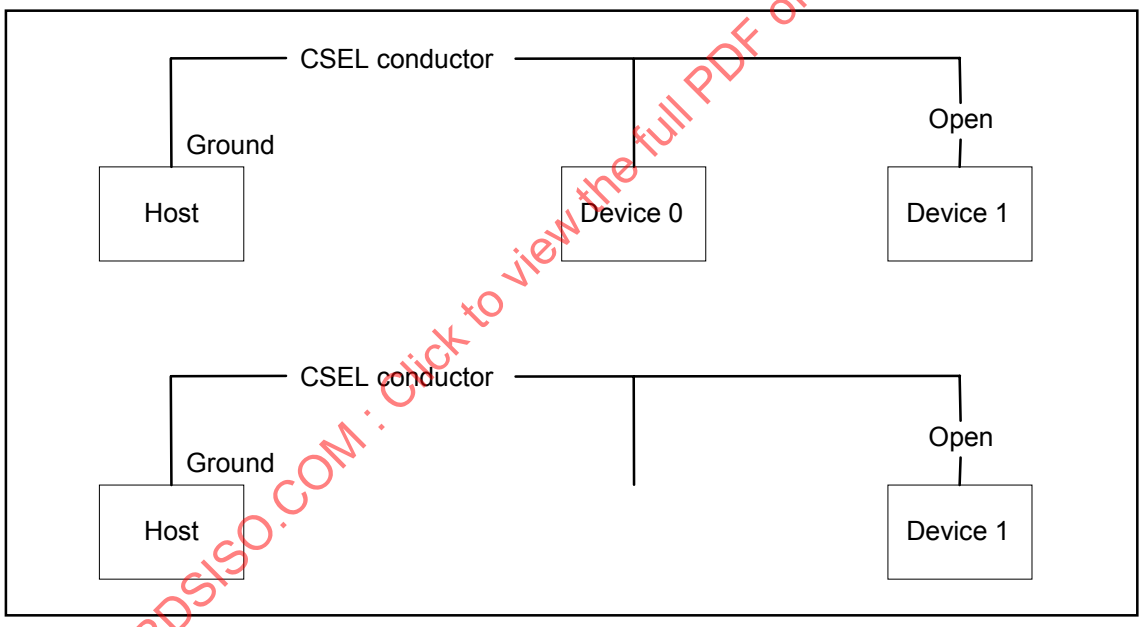


Figure 29 – Cable select example

8.2.13.3 CSEL with 80-conductor cable

For designated cable assemblies (including all 80-conductor cable assemblies), these assemblies are constructed so that CSEL is connected from the host connector to the connector at the opposite end of the cable from the host (see Figure 30). Therefore, Device 0 shall be at the opposite end of the cable from the host. Single device configurations with the device not at the end of the cable shall not be used with Ultra DMA modes.

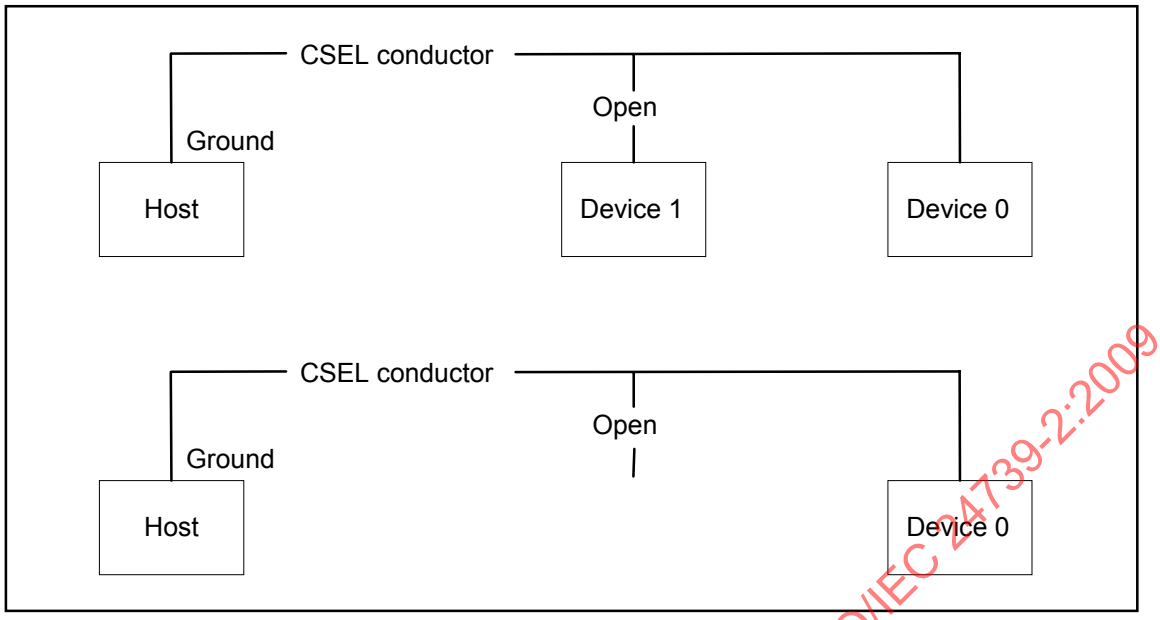


Figure 30 – Alternate cable select example

9 Parallel interface general operational requirements of the physical, data link and transport layers

9.1 Interrupts

INTRQ is used by the selected device to notify the host of an event. The device internal Interrupt Pending state is set when such an event occurs. If nIEN is cleared to zero, INTRQ is asserted (see 8.2.9).

The device shall enter the Interrupt Pending state when

1) any command except a PIO data-in command reaches command completion successfully;
2) any command reaches command completion with error;
3) the device is ready to send a data block during a PIO data-in command;
4) the device is ready to accept a data block after the first data block during a PIO data-out command;
5) a device implementing the PACKET Command feature set is ready to receive the command packet and bits (6:5) in word 0 of the IDENTIFY PACKET DEVICE data have the value 01b;
6) a device implementing the PACKET Command feature set is ready to transfer a DRQ data block during a PIO transfer;
7) a device implementing the Overlap feature set performs a bus release if the bus release interrupt is enabled;
8) a device implementing the Overlap feature set has performed a bus release and is now ready to continue the command execution;
9) a device implementing the Overlap feature set is ready to transfer data after a SERVICE command if the Service interrupt is enabled;
10) Device 0 completes an EXECUTE DEVICE DIAGNOSTIC command. Device 1 shall not enter the Interrupt Pending state when completing an EXECUTE DEVICE DIAGNOSTIC command.

The device shall not exit the Interrupt Pending state as a result of the host changing the state of the DEV bit.

The device shall exit the Interrupt Pending state when

1) the device is selected, BSY is cleared to zero and the Status register is read;
2) the device is selected, both BSY and DRQ are cleared to zero and the Command register is written;
3) the RESET- signal is asserted;
4) the SRST bit is set to one.

9.2 Multiword DMA

Multiword DMA is a mandatory data transfer protocol used with the READ DMA, READ DMA EXT, WRITE DMA, WRITE DMA EXT, READ DMA QUEUED, READ DMA QUEUED EXT, WRITE DMA QUEUED, WRITE DMA QUEUED EXT and PACKET commands. When a Multiword DMA transfer is enabled as indicated by IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (see ISO/IEC 24739-1:2008, Clause 6) data, this data transfer protocol shall be used for the data transfers associated with these commands. DMA transfer modes may be changed using the SET FEATURES 03h subcommand (see ISO/IEC 24739-1:2008, Clause 6). Signal timing for this protocol is described in 12.2.4.

The DMARQ and DMACK- signals are used to signify when a Multiword DMA transfer is to be executed. The DMARQ and DMACK- signals are also used to control the data flow of a Multiword DMA data transfer.

When a device is ready to transfer data associated with a Multiword DMA transfer, the device shall assert DMARQ. The host shall then respond by negating CS0- and CS1-, asserting DMACK- and begin the data transfer by asserting, then negating, DIOW- or DIOR- for each word transferred. CS0- and CS1- shall remain negated as long as DMACK- is asserted. The host shall not assert DMACK- until DMARQ has been asserted by the device. The host shall initiate DMA read or write cycles only when both DMARQ and DMACK- are asserted. Having asserted DMARQ and DMACK-, these signals shall remain asserted until at least one word of data has been transferred.

The device may pause the transfer for flow control purposes by negating DMARQ. The host shall negate DMACK- in response to the negation of DMARQ. The device may then reassert DMARQ to continue the data transfer when the device is ready to transfer more data and DMACK- has been negated by the host.

The host may pause the transfer for flow control purposes by either pausing the assertion of DIOW- or DIOR- pulses or by negating DMACK-. The device may leave DMARQ asserted if DMACK- is negated. The host may then reassert DMACK- when DMARQ is asserted and begin asserting DIOW- or DIOR- pulses to continue the data transfer.

When the Multiword DMA data transfer is complete, the device shall negate DMARQ and the host shall negate DMACK- in response.

DMARQ shall be driven from the first assertion at the beginning of a DMA transfer until the negation after the last word is transferred. This signal shall be released at all other times.

If the device detects an error before data transfer for the command is complete, the device may complete the data transfer or may terminate the data transfer before completion and shall report the error in either case.

NOTE If a data transfer is terminated before completion, the assertion of INTRQ should be passed through to the host software driver regardless of whether all data requested by the command has been transferred.

9.3 Ultra DMA feature set

9.3.1 Overview

Ultra DMA is an optional data transfer protocol used with the READ DMA, READ DMA EXT, WRITE DMA, WRITE DMA EXT, READ DMA QUEUED, READ DMA QUEUED EXT, WRITE DMA QUEUED, WRITE DMA QUEUED EXT and PACKET commands. When this protocol is enabled, the Ultra DMA protocol shall be used instead of the Multiword DMA protocol when these commands are issued by the host. This protocol applies to the Ultra DMA data burst only. When this protocol is used there are no changes to other elements of the ATA protocol (e.g., Command Block Register access).

Several signal lines are redefined to provide different functions during an Ultra DMA burst. These lines assume these definitions when

a) an Ultra DMA mode is selected and

b) a host issues a READ DMA, WRITE DMA, READ DMA QUEUED, WRITE DMA QUEUED, or a PACKET command requiring data transfer and

c) the host asserts DMACK-.

These signal lines revert back to the definitions used for non-Ultra DMA transfers upon the negation of DMACK- by the host at the termination of an Ultra DMA burst.

With the Ultra DMA protocol, the STROBE signal that latches data from DD(15:0) is generated by the same agent (either host or device) that drives the data onto the bus. Ownership of DD(15:0) and this data strobe signal are given either to the device during an Ultra DMA data-in burst or to the host for an Ultra DMA data-out burst.

During an Ultra DMA burst a sender shall always drive data onto the bus and, after a sufficient time to allow for propagation delay, cable settling and setup time, the sender shall generate a STROBE edge to latch the data. Both edges of STROBE are used for data transfers so that the frequency of STROBE is limited to the same frequency as the data.

Words in the IDENTIFY DEVICE data indicate support of the Ultra DMA feature and the Ultra DMA modes the device is capable of supporting. The Set transfer mode subcommand in the SET FEATURES command shall be used by a host to select the Ultra DMA mode at which the system operates. The Ultra DMA mode selected by a host shall be less than or equal to the fastest mode of which the device is capable. Only one Ultra DMA mode shall be selected at any given time. All timing requirements for a selected Ultra DMA mode shall be satisfied. Devices supporting any Ultra DMA mode shall also support all slower Ultra DMA modes.

An Ultra DMA capable device shall retain the previously selected Ultra DMA mode after executing a software reset sequence or the sequence caused by receipt of a DEVICE RESET command if a SET FEATURES disable reverting to defaults command has been issued. The device may revert to a Multiword DMA mode if a SET FEATURES enable reverting to default has been issued. An Ultra DMA capable device shall clear any previously selected Ultra DMA mode and revert to the default non-Ultra DMA modes after executing a power-on or hardware reset.

Both the host and device perform a CRC function during an Ultra DMA burst. At the end of an Ultra DMA burst the host sends its CRC data to the device. The device compares its CRC data to the data sent from the host. If the two values do not match, the device reports an error in the error register. If an error occurs during one or more Ultra DMA bursts for any one command, the device shall report the first error that occurred. If the device detects that a CRC error has occurred before data transfer for the command is complete, the device may complete the transfer and report the error or abort the command and report the error.

NOTE If a data transfer is terminated before completion, the assertion of INTRQ should be passed through to the host software driver regardless of whether all data requested by the command has been transferred.

9.3.2 Phases of operation

9.3.2.1 General

An Ultra DMA data transfer is accomplished through a series of Ultra DMA data-in or data-out bursts. Each Ultra DMA burst has three mandatory phases of operation: the initiation phase, the data transfer phase and the Ultra DMA burst termination phase. In addition, an Ultra DMA burst may be paused during the data transfer phase (see 11.13 and 11.14 for the detailed protocol descriptions for each of these phases, 12.2.5 defines the specific timing requirements). In the following rules DMARDY- is used in cases that could apply to either DDMARDY- or HDMARDY- and STROBE is used in cases that could apply to either DSTROBE or HSTROBE. The following are general Ultra DMA rules.

1) An Ultra DMA burst is defined as the period from an assertion of DMACK- by the host to the subsequent negation of DMACK-.
2) When operating in Ultra DMA modes 2, 1 or 0 a recipient shall be prepared to receive up to two data words whenever an Ultra DMA burst is paused. When operating in Ultra DMA modes 6, 5, 4 or 3 a recipient shall be prepared to receive up to three data words whenever an Ultra DMA burst is paused.

9.3.2.2 Ultra DMA burst initiation phase rules

The following rules apply to Ultra DMA burst initiation.

1) An Ultra DMA burst initiation phase begins with the assertion of DMARQ by a device and ends when the sender generates a STROBE edge to transfer the first data word.
2) An Ultra DMA burst shall always be requested by a device asserting DMARQ.
3) When ready to initiate the requested Ultra DMA burst, the host shall respond by asserting DMACK-.
4) A host shall never assert DMACK- without first detecting that DMARQ is asserted.
5) For Ultra DMA data-in bursts: a device may begin driving DD(15:0) after detecting that DMACK- is asserted, STOP negated and HDMARDY- is asserted.
6) After asserting DMARQ or asserting DDMARDY- for an Ultra DMA data-out burst, a device shall not negate either signal until the first STROBE edge is generated.
7) After negating STOP or asserting HDMARDY- for an Ultra DMA data-in burst, a host shall not change the state of either signal until the first STROBE edge is generated.

9.3.2.3 Data transfer phase rules

The following rules apply to Data transfer.

1) The data transfer phase is in effect from after Ultra DMA burst initiation until Ultra DMA burst termination.
2) A recipient pauses an Ultra DMA burst by negating DMARDY- and resumes an Ultra DMA burst by reasserting DMARDY-.
3) A sender pauses an Ultra DMA burst by not generating STROBE edges and resumes by generating STROBE edges.
4) A recipient shall not signal a termination request immediately when the sender stops generating STROBE edges. In the absence of a termination from the sender the recipient shall always negate DMARDY- and wait the required period before signaling a termination request.
5) A sender may generate STROBE edges at greater than the minimum period specified by the enabled Ultra DMA mode. The sender shall not generate STROBE edges at less than the minimum period specified by the enabled Ultra DMA mode. A recipient shall be able to receive data at the minimum period specified by the enabled Ultra DMA mode.

9.3.2.4 Ultra DMA burst termination phase rules

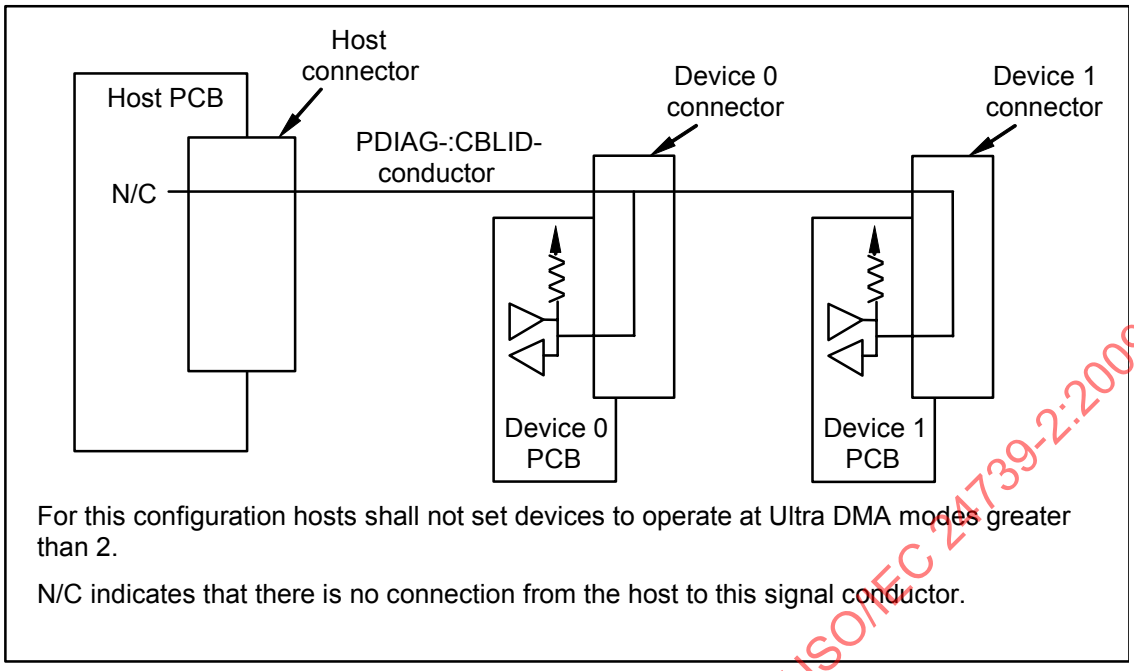
The following rules apply to Ultra DMA burst termination.

1) Either a sender or a recipient may terminate an Ultra DMA burst.
2) Ultra DMA burst termination is not the same as command completion. If an Ultra DMA burst termination occurs before command completion, the command shall be completed by initiation of a new Ultra DMA burst at some later time or aborted by the host issuing a hardware or software reset or DEVICE RESET command if implemented by the device.
3) An Ultra DMA burst shall be paused before a recipient requests a termination.
4) A host requests a termination by asserting STOP. A device acknowledges a termination request by negating DMARQ.
5) A device requests a termination by negating DMARQ. A host acknowledges a termination request by asserting STOP.
6) Once a sender requests a termination, the sender shall not change the state of STROBE until the recipient acknowledges the request. Then, if STROBE is not in the asserted state, the sender shall return STROBE to the asserted state. No data shall be transferred on this transition of STROBE.
7) A sender shall return STROBE to the asserted state whenever the sender detects a termination request from the recipient. No data shall be transferred nor CRC calculated on this edge of DSTROBE.
8) Once a recipient requests a termination, the responder shall not change DMARDY from the negated state for the remainder of an Ultra DMA burst.
9) A recipient shall ignore a STROBE edge when DMARQ is negated or STOP is asserted.

9.4 Host determination of cable type by detecting CBLID-

In a system using a cable, hosts shall determine that an 80-conductor cable is installed in a system before operating with transfer modes faster than Ultra DMA mode 2. Hosts shall detect that CBLID- is connected to ground to determine the cable type. See 8.2.11.

For detecting that CBLID- is connected to ground, the host shall test to see if CBLID- is below V_{IL} or above V_{IH}. If the signal is below V_{IL}, then an 80-conductor cable assembly is installed in the system because this signal is grounded in the 80-conductor cable assembly's host connector. If the signal is above V_{IH}, then a 40-conductor cable assembly is installed because this signal is connected to the device(s) and is pulled up through a 10 kΩ resistor at each device.



For this configuration hosts shall not set devices to operate at Ultra DMA modes greater than 2.

N/C indicates that there is no connection from the host to this signal conductor.

Figure 31 – Example configuration of a system with a 40-conductor cable

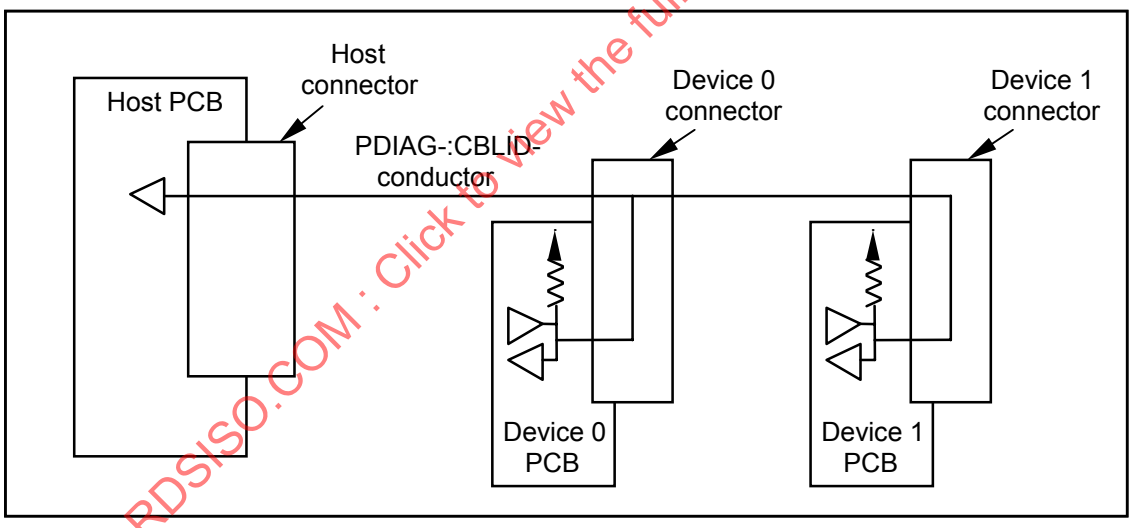


Figure 32 – Example configuration of a system where the host detects a 40-conductor cable

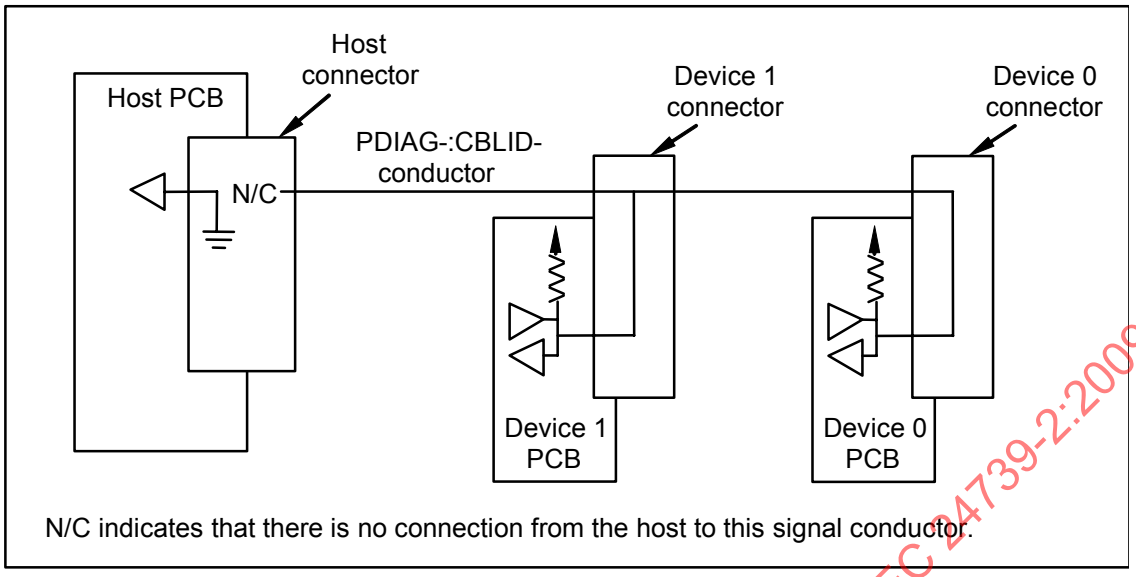


Figure 33 – Example configuration of a system where the host detects an 80-conductor cable

Table 40 – Host detection of CBLID-

Cable assembly type	Device 1 releases PDIAG-	Electrical state of CBLID- at host	Host-determined cable type	Determination correct?
40-conductor	Yes	1	40-conductor	Yes
80-conductor	Yes	0	80-conductor	Yes
40-conductor	No	0	80-conductor	No (see [a])
80-conductor	No	0	80-conductor	Yes

[a] Ultra DMA mode 3, 4, 5 or 6 may be set incorrectly resulting in ICRC errors.

10 Parallel interface register addressing

Registers have different meanings depending on if the register is being written or being read and additionally whether the PACKET command feature set is implemented (see ISO/IEC 24739-1:2008), as indicated in Table 41.

Table 41 – I/O registers

Registers used by devices not implementing the PACKET command feature set		**Registers used by devices implementing the PACKET command feature set**	
Command Block registers		**Command Block registers**	
When read	**When written**	**When read**	**When written**
Data	Data	Data	Data
Error	Features	Error	Features
Sector Count	Sector Count	Interrupt reason	
LBA Low	LBA Low		
LBA Mid	LBA Mid	Byte Count Low	Byte Count Low
LBA High	LBA High	Byte Count High	Byte Count High
Device	Device	Device select	Device select
Status	Command	Status	Command
Control Block registers		**Control Block registers**	
Alternate Status	Device Control	Alternate Status	Device Control

For transport protocols and timing, see Clauses 11 and 12.

When the host initiates a register or Data port read or write cycle by asserting then negating either DIOW- or DIOR-, the device(s) shall determine how to respond and what action(s), if any, are to be taken. The following text and tables describe this decision process.

The device response begins with these steps:

1) for a device that is not in Sleep mode, see Table 42.
2) if DMACK- is asserted, a device in Sleep mode shall ignore all DIOW-/DIOR- activity. If DMACK- is not asserted, a device in Sleep mode shall respond as described in Table 47, if the device does not implement the PACKET Command feature set or Table 48, if the device does implement the PACKET Command feature set.

Table 42 – Device response to DIOW-/DIOR-

Is the device selected? [a]	Is DMACK- asserted?	Action/Response
No	No	See Table 43
No	Yes	DIOW-/DIOR- cycle is ignored (possible DMA transfer with the other device)
Yes	No	See Table 44.
Yes	Yes	See Table 45 (see [b]).
Device 1 is selected but there is no Device 1 and Device 0 responds for Device 1.	No	See Table 46 and ISO/IEC 24739-1:2008, Clause 5.
Device 1 is selected but there is no Device 1 and Device 0 responds for Device 1.	Yes	DIOW-/DIOR- cycle is ignored (possible malfunction of the host)

[a] Device selected means that the DEV bit in the Device register matches the logical device number of the device.

[b] Applicable only to Multiword DMA, not applicable to Ultra DMA.

Table 43 – Device is not selected, DMACK- is not asserted

CS0-	CS1-	DA2	DA1	DA0	DIOx-	DMARQ	BSY	DRQ	Device response
N	N	X	X	X	X	Z	X	X	DIOW-/DIOR- cycle is ignored.
N	A	N	X	X	X	Z	X	X	
N	A	A	N	X	X	Z	X	X	
N	A	A	A	N	W	Z	X	X	Place new data into the Device Control register and respond to the new values of the nIEN and SRST bits.
N	A	A	A	N	R	Z	X	X	DIOW-/DIOR- cycle is ignored.
N	A	A	A	A	X	Z	X	X	
A	N	N	N	N	X	Z	X	X	
A	N	N	N	A	W	Z	0	X	Place new data into the Feature register.
A	N	N	N	A	W	Z	1	X	DIOW-/DIOR- cycle is ignored.
A	N	N	N	A	R	Z	X	X	
A	N	N	A	N	W	Z	0	X	Place new data into the Sector Count register.
A	N	N	A	N	W	Z	1	X	DIOW-/DIOR- cycle is ignored.
A	N	N	A	N	R	Z	X	X	
A	N	N	A	A	W	Z	0	X	Place new data into the LBA Low register.
A	N	N	A	A	W	Z	1	X	DIOW-/DIOR- cycle is ignored.
A	N	N	A	A	R	Z	X	X	
A	N	A	N	N	W	Z	0	X	Place new data into the LBA Mid register.
A	N	A	N	N	W	Z	1	X	DIOW-/DIOR- cycle is ignored.
A	N	A	N	N	R	Z	X	X	
A	N	A	N	A	W	Z	0	X	Place new data into the LBA High register.
A	N	A	N	A	W	Z	1	X	DIOW-/DIOR- cycle is ignored.
A	N	A	N	A	R	Z	X	X	
A	N	A	A	N	W	Z	0	X	Place new data into the Device register. Respond to the new value of the DEV bit.
A	N	A	A	N	W	Z	1	X	DIOW-/DIOR- cycle is ignored.
A	N	A	A	N	R	Z	X	X	
A	N	A	A	A	W	Z	0	X	Place new data into the Command register. Do not respond unless the command is EXECUTE DEVICE DIAGNOSTICS.
A	N	A	A	A	W	Z	1	X	DIOW-/DIOR- cycle is ignored.
A	N	A	A	A	R	Z	X	X	
A	A	X	X	X	X	Z	X	X	DIOW-/DIOR- cycle is ignored.

NOTE 1 Except in the DIOx- column, A = asserted, N = negated, Z = released, X = don't care.

NOTE 2 In the DIOx- column, R = DIOR- asserted, W = DIOW- asserted, X = either DIOR- or DIOW- is asserted.

NOTE 3 Device is selected if the DEV bit in the Device register is the logical device number of the device.

Table 44 – Device is selected, DMACK- is not asserted

CS0-	CS1-	DA2	DA1	DA0	DIOx-	DMARQ	BSY	DRQ	Device response
N	N	X	X	X	X	X	X	X	DIOW-/DIOR- cycle is ignored.
N	A	N	X	X	X	X	X	X	
N	A	A	N	X	X	X	X	X	
N	A	A	A	N	W	X	X	X	Place new data into the Device Control register and respond to the new values of the nIEN and SRST bits.
N	A	A	A	N	R	X	X	X	Place Status register contents on the data bus (do not change the Interrupt Pending state).
N	A	A	A	A	X	X	X	X	DIOW-/DIOR- cycle is ignored.
A	N	N	N	N	X	X	0	0	
A	N	N	N	N	X	X	0	1	PIO data transfer for this device, a 16-bit data word is transferred via the Data register.
A	N	N	N	N	X	X	1	X	Result of DIOW-/DIOR- cycle is indeterminate.
A	N	N	N	A	W	X	0	0	Place new data into the Features register.
A	N	N	N	A	W	X	0	1	DIOW- is ignored, this is a malfunction of the host.
A	N	N	N	A	W	X	1	X	Result of DIOW-/DIOR- cycle is indeterminate.
A	N	N	N	A	R	X	0	X	Place the contents of the Error register on the data bus.
A	N	N	N	A	R	X	1	X	Place the contents of the Status register on the data bus.
A	N	N	A	N	W	X	0	0	Place new data into the Sector Count register.
A	N	N	A	N	W	X	0	1	DIOW- is ignored, this is a malfunction of the host.
A	N	N	A	N	W	X	1	X	Result of DIOW-/DIOR- cycle is indeterminate.
A	N	N	A	N	R	X	0	X	Place the contents of the Sector Count register on the data bus.
A	N	N	A	N	R	X	1	X	Place the contents of the Status register on the data bus.
A	N	N	A	A	W	X	0	0	Place new data into the LBA Low register.
A	N	N	A	A	W	X	0	1	DIOW- is ignored, this is a malfunction of the host.
A	N	N	A	A	W	X	1	X	Result of DIOW-/DIOR- cycle is indeterminate.
A	N	N	A	A	R	X	0	X	Place the contents of the LBA Low register on the data bus.
A	N	N	A	A	R	X	1	X	Place the contents of the Status register on the data bus.
A	N	A	N	N	W	X	0	0	Place new data into the LBA Mid register.
A	N	A	N	N	W	X	0	1	DIOW- is ignored, this is a malfunction of the host.
A	N	A	N	N	W	X	1	X	Result of DIOW-/DIOR- cycle is indeterminate.
A	N	A	N	N	R	X	0	X	Place the contents of the LBA Mid register on the data bus.
A	N	A	N	N	R	X	1	X	Place the contents of the Status register on the data bus.
A	N	A	N	A	W	X	0	0	Place new data into the LBA High register.

(continued)

Table 44 – Device is selected, DMACK- is not asserted *(continued)*

CS0-	CS1-	DA2	DA1	DA0	DIOx-	DMARQ	BSY	DRQ	Device response
A	N	A	N	A	W	X	0	1	DIOW- is ignored, this is a malfunction of the host.
A	N	A	N	A	W	X	1	X	Result of DIOW-/DIOR- cycle is indeterminate.
A	N	A	N	A	R	X	0	X	Place the contents of the LBA High register on the data bus.
A	N	A	N	A	R	X	1	X	Place the contents of the Status register on the data bus.
A	N	A	A	N	W	X	0	0	Place new data into the Device register. Respond to the new value of the DEV bit.
A	N	A	A	N	W	X	0	1	DIOW- is ignored, this is a malfunction of the host.
A	N	A	A	N	W	X	1	X	Result of DIOW-/DIOR- cycle is indeterminate.
A	N	A	A	N	R	X	0	X	Place the contents of the Device register on the data bus.
A	N	A	A	N	R	X	1	X	Place the contents of the Status register on the data bus.
A	N	A	A	A	W	X	0	0	Place new data into the Command register and respond to the new command (exit the Interrupt Pending State).
A A	N N	A A	A A	A A	W W	X X	0 1	1 X	Result of DIOW-/DIOR- cycle is indeterminate, unless the device supports DEVICE RESET. If the device supports the DEVICE RESET command, exit the Interrupt Pending state.
A	N	A	A	A	R	X	X	X	Place contents of Status register on the data bus and exit the Interrupt Pending state.
A	A	X	X	X	X	X	X	X	DIOW-/DIOR- cycle is ignored.

NOTE 1 Except in the DIOx- column, A = asserted, N = negated, X = don't care.

NOTE 2 In the DIOx- column, R = DIOR- asserted, W = DIOW- asserted, X = either DIOR- or DIOW- is asserted.

NOTE 3 Device is selected if the DEV bit in the Device register is the logical device number of the device.

NOTE 4 For devices implementing the 48-bit Address feature set, the HOB bit in the Device Control register defines whether the current or previous content of the registers is placed on DD(7:0).

(concluded)

Table 45 – Device is selected, DMACK- is asserted (for Multiword DMA only)

CS0-	CS1-	DA2	DA1	DA0	DIOx-	DMARQ	BSY	DRQ	Device response
N N	N N	X X	X X	X X	X X	N N	1 0	X X	This could be the final DIOW-/DIOR- of a Multiword DMA transfer burst, or a possible malfunction of the host that is ignored.
N N	N N	X X	X X	X X	X X	A A	1 0	X 1	DMA transfer for this device, a 16-bit word of data is transferred via the Data Port.
X A	A X	X X	X X	X X	X X	X X	X X	X X	DIOW-/DIOR- cycle is ignored (possible malfunction of the host).

NOTE 1 Except in the DIOx- column, A = asserted, N = negated, Z = released, X = don't care.

NOTE 2 In the DIOx- column, R = DIOR- asserted, W = DIOW- asserted, X = either DIOR- or DIOW- is asserted.

NOTE 3 Device is selected if the DEV bit in the Device register is the logical device number of the device.

Table 46 –Device 1 is selected and Device 0 is responding for Device 1

CS0-	CS1-	DA2	DA1	DA0	DIOx-	DMARQ	BSY	DRQ	Device Response
N	N	X	X	X	X	Z	0	0	DIOW-/DIOR- cycle is ignored.
N	A	N	X	X	X	Z	0	0	
N	A	A	N	X	X	X	0	0	
N	A	A	A	N	W	X	0	0	Place new data into the Device 0 Device Control register and respond to the new values of the nIEN and SRST bits.
N	A	A	A	N	R	X	0	0	Place 00H on the data bus.
N	A	A	A	A	X	X	0	0	DIOW-/DIOR- cycle is ignored.
A	N	N	N	N	X	X	0	0	
A	N	N	N	A	W	X	0	0	Place new data into the Device 0 Feature register.
A	N	N	N	A	R	X	0	0	Place the contents of the Device 0 Error register on the data bus.
A	N	N	A	N	W	X	0	0	Place new data into Device 0 Sector Count register.
A	N	N	A	N	R	X	0	0	If the device does not implement the PACKET Command feature set, the device shall place the contents of the Device 0 Sector Count register on the data bus. If the device implements the PACKET Command feature set, the device shall place 00h on the data bus.
A	N	N	A	A	W	X	0	0	Place new data into Device 0 LBA Low register.
A	N	N	A	A	R	X	0	0	If the device does not implement the PACKET Command feature set, the device shall place the contents of the Device 0 LBA Low register on the data bus. If the device implements the PACKET Command feature set, the device shall place 00h on the data bus.
A	N	A	N	N	W	X	0	0	Place new data into Device 0 LBA Mid register.
A	N	A	N	N	R	X	0	0	If the device does not implement the PACKET Command feature set, the device shall place the contents of the Device 0 LBA Mid register on the data bus. If the device implements the PACKET Command feature set, the device shall place 00h on the data bus.
A	N	A	N	A	W	X	0	0	Place new data into Device 0 LBA High register.
A	N	A	N	A	R	X	0	0	If the device does not implement the PACKET Command feature set, the device shall place the contents of the Device 0 LBA High register on the data bus. If the device implements the PACKET Command feature set, the device shall place 00h on the data bus.
A	N	A	A	N	W	X	0	0	Place new data into the Device 0 Device register. Respond to the new value of the DEV bit.

(continued)

Table 46 – Device 1 is selected and Device 0 is responding for Device 1 *(continued)*

CS0-	CS1-	DA2	DA1	DA0	DIOx-	DMARQ	BSY	DRQ	Device response
A	N	A	A	N	R	X	0	0	If the device does not implement the PACKET Command feature set, the device shall place the contents of the Device 0 Device register, with the DEV bit set to one, on the data bus. If the device implements the PACKET Command feature set, the device shall place 00h on the data bus.
A	N	A	A	A	W	X	0	0	Place new data into the Command register of Device 0. Do not respond unless the command is EXECUTE DEVICE DIAGNOSTICS.
A	N	A	A	A	R	X	0	0	Place 00H on the data bus.
A	A	X	X	X	X	X	0	0	DIOW-/DIOR- cycle is ignored.

NOTE 1 Except in the DIOx- column, A = asserted, N = negated, Z = released, X = don't care.

NOTE 2 In the DIOx- column, R = DIOR- asserted, W = DIOW- asserted, X = either DIOR- or DIOW- is asserted.

NOTE 3 Device is selected if the DEV bit in the Device register is the logical device number of the device.

Table 47 – Device is in Sleep mode, DEVICE RESET is not implemented, DMACK- is not asserted

CS0-	CS1-	DA2	DA1	DA0	DIOx-	DMARQ	BSY	DRQ	Device response
N	N	X	X	X	X	Z	X	X	DIOW-/DIOR- cycle is ignored.
N	A	N	X	X	X	Z	X	X	
N	A	A	N	X	X	Z	X	X	
N	A	A	A	N	W	Z	X	X	Place new data into the Device Control register SRST bit and respond only if SRST bit is 1.
N	A	A	A	N	R	Z	X	X	DIOW-/DIOR- cycle is ignored.
N	A	A	A	A	X	Z	X	X	
A	N	X	X	X	X	Z	X	X	
A	A	X	X	X	X	Z	X	X	

NOTE 1 Except in the DIOx- column, A = asserted, N = negated, Z = released, X = don't care.

NOTE 2 In the DIOx- column, R = DIOR- asserted, W = DIOW- asserted, X = either DIOR- or DIOW- is asserted.

NOTE 3 Device is selected if the DEV bit in the Device register is the logical device number of the device.

Table 48 – Device is in Sleep mode, DEVICE RESET is implemented, DMACK- is not asserted

CS0-	CS1-	DA2	DA1	DA0	DIOx-	DMARQ	BSY	DRQ	Device response
N	N	X	X	X	X	Z	X	X	DIOW-/DIOR- cycle is ignored.
N	A	N	X	X	X	Z	X	X	
N	A	A	N	X	X	Z	X	X	
N	A	A	A	N	W	Z	X	X	Place new data into the Device Control register SRST bit and respond only if SRST bit is 1.
N	A	A	A	N	R	Z	X	X	DIOW-/DIOR- cycle is ignored.
N	A	A	A	A	X	Z	X	X	
A	N	N	X	X	X	Z	X	X	
A	N	A	N	X	X	Z	X	X	
A	N	A	A	N	W	Z	X	X	Place new data into the Device register DEV bit.
A	N	A	A	N	R	Z	X	X	DIOR- cycle is ignored.
A	N	A	A	A	W	Z	X	X	DIOW- cycle is ignored unless the device is selected and the command is DEVICE RESET.
A	N	A	A	A	R	Z	X	X	DIOR- cycle is ignored.
A	A	X	X	X	X	Z	X	X	DIOW-/DIOR- cycle is ignored.

NOTE 1 Except in the DIOx- column, A = asserted, N = negated, Z = released, X = don't care.

NOTE 2 In the DIOx- column, R = DIOR- asserted, W = DIOW- asserted, X = either DIOR- or DIOW- is asserted.

NOTE 3 Device is selected if the DEV bit in the Device register is the logical device number of the device.

11 Parallel interface transport protocol

11.1 General

Commands are grouped into different classes according to the protocol followed for command execution. The command classes with their associated protocol are defined in state diagrams in this clause, one state diagram for host actions and a second state diagram for device actions. Figure 34 shows the overall relationship of the host protocol state diagrams. Figure 35 shows the overall relationship of the device protocol state diagrams. State diagrams defining these protocols are not normative descriptions of implementations, they are normative descriptions of externally apparent device or host behavior. Different implementations are allowed. See 3.3.8 for state diagram conventions.

A device shall not timeout any activity when waiting for a response from the host.

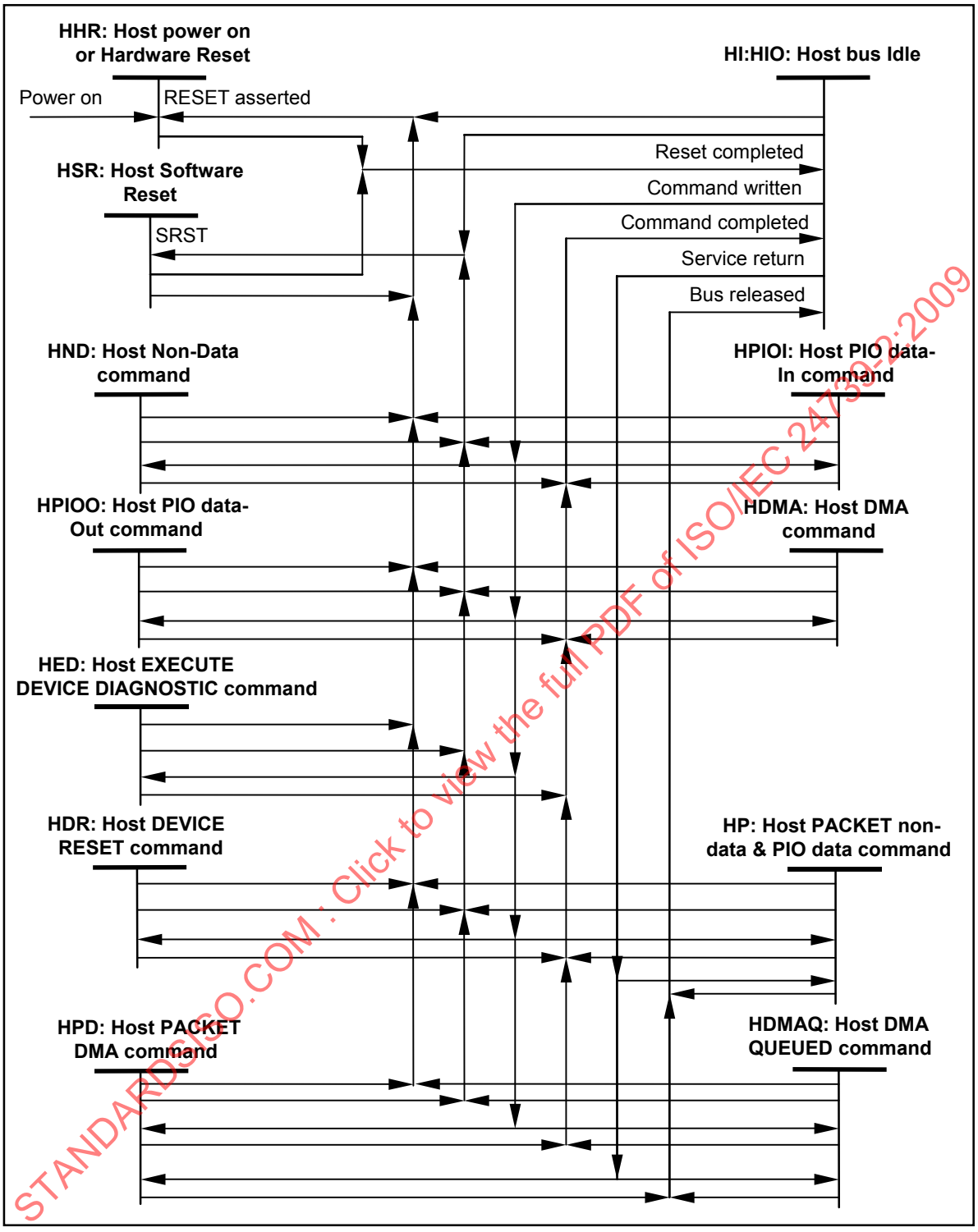


Figure 34 – Overall host protocol state sequence

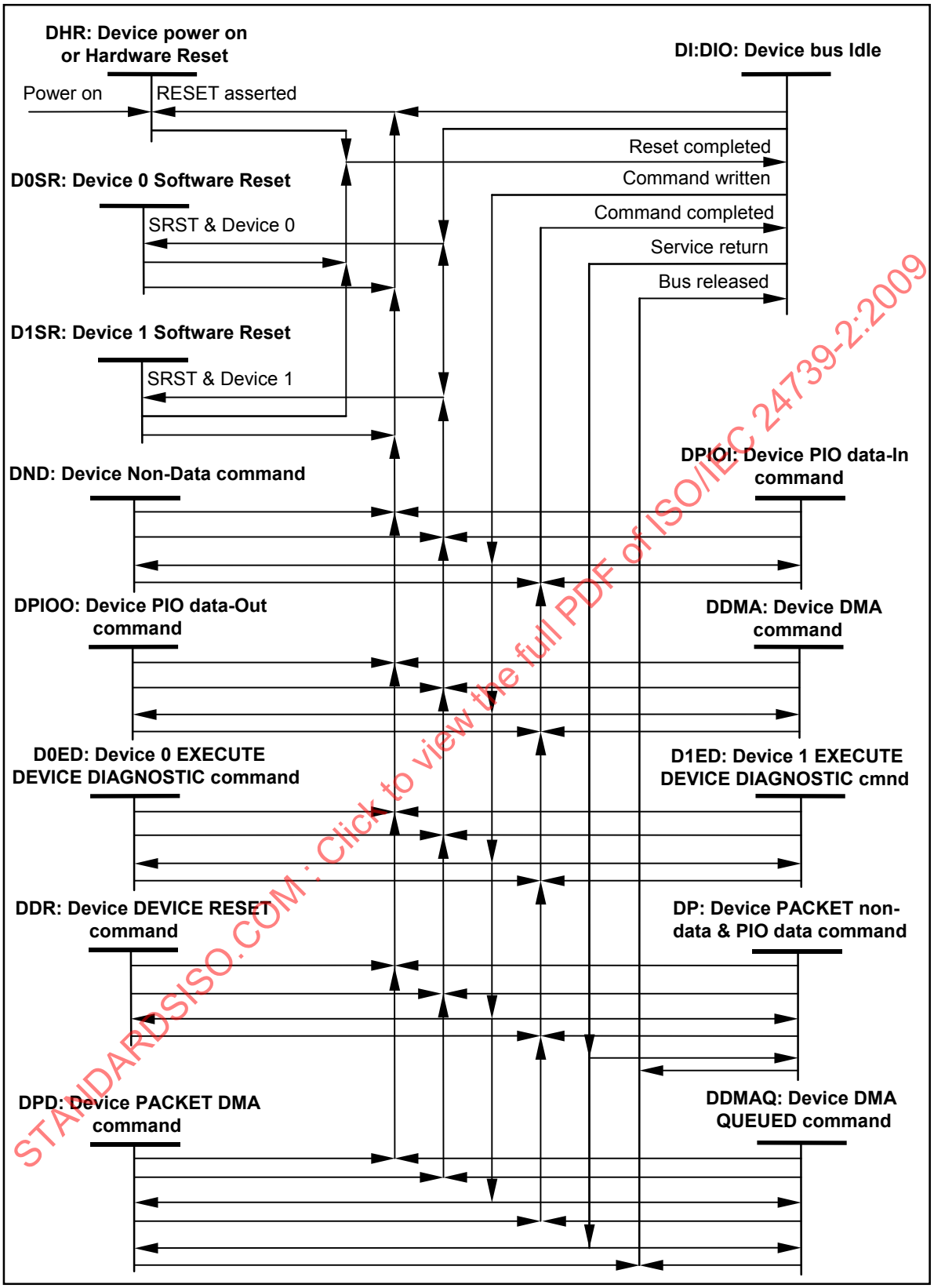


Figure 35 – Overall device protocol state sequence

11.2 Power-on and hardware reset protocol

This clause describes the protocol for processing of power-on and hardware resets.

If the host asserts RESET-, regardless of the power management mode, the device shall execute the hardware reset protocol. If the host reasserts RESET- before a device has completed the power-on or hardware reset protocol, then the device shall restart the protocol from the beginning.

The host should not set the SRST bit to one in the Device Control register or issue a DEVICE RESET command while the BSY bit is set to one in either device Status register as a result of executing the power-on or hardware reset protocol. If the host sets the SRST bit in the Device Control register to one or issues a DEVICE RESET command before devices have completed execution of the power-on or hardware reset protocol, then the devices shall ignore the software reset or DEVICE RESET command.

A host should issue an IDENTIFY DEVICE and/or IDENTIFY PACKET DEVICE command after the power-on or hardware reset protocol has completed to determine the current status of features implemented by the device(s).

NOTE Serial implementations of ATA have different hardware reset timeout requirements, see ISO/IEC 24739-3.

Figure 36 and the text following the figure decribe the power-on or hardware reset protocol for the host. Figure 37 and the text following the figure decribe the power-on or hardware reset protocol for the devices.

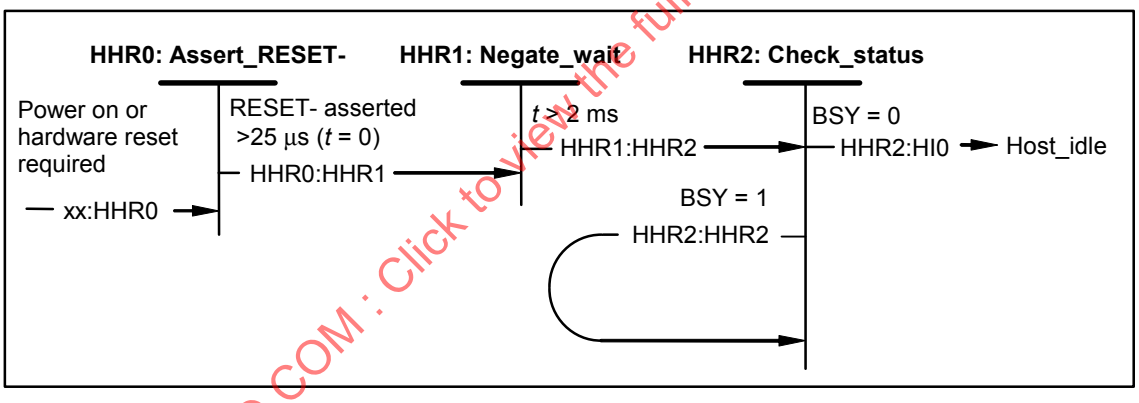


Figure 36 – Host power-on or hardware reset state diagram

HHR0: Assert_RESET- State: This state is entered at power-on or when the host recognizes that a hardware reset is required.

When in this state, the host asserts RESET-. The host shall remain in this state with RESET- asserted for at least 25 µs. The host shall negate CS(1:0), DA(2:0), DMACK-, DIOR- and DIOW- and release DD(15:0).

Transition HHR0:HHR1: When the host has had RESET- asserted for at least 25 µs, the host shall make a transition to the HHR1: Negate_wait state.

HHR1: Negate_wait State: This state is entered when RESET- has been asserted for at least 25 µs.

When in this state, the host shall negate RESET-. The host shall remain in this state for at least 2 ms after negating RESET-. If the host tests CBLID- it shall do so at this time.

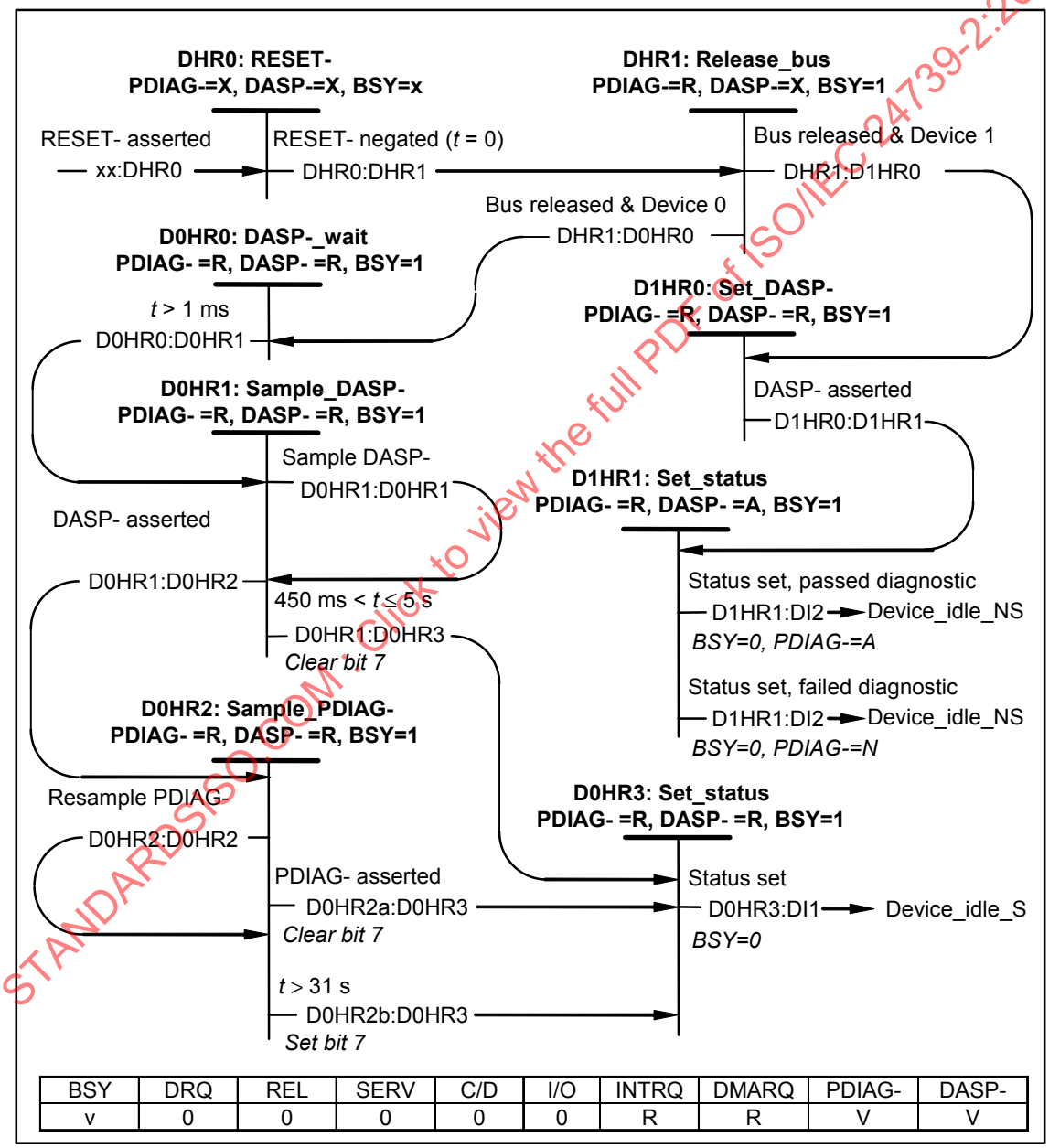
Transition HHR1:HHR2: When RESET- has been negated for at least 2 ms, the host shall make a transition to the HHR2: Check_status state.

HHR2: Check_status State: This state is entered when RESET- has been negated for at least 2 ms.

When in this state, the host shall read the Status or Alternate Status register.

Transition HHR2:HHR2: When BSY is set to one, the host shall make a transition to the HHR2: Check_status state.

Transition HHR2:HI0: When BSY is cleared to zero, the host shall make a transition to the HI0: Host_idle state (See Figure 41). If status indicates that an error has occurred, the host shall take appropriate error recovery action.



BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
v	0	0	0	0	0	R	R	V	V

Figure 37 – Device power-on or hardware reset state diagram

DHR0: RESET State: This state is entered when a valid assertion of the RESET- signal is recognized. The device shall not recognize a RESET- assertion shorter than 20 ns as valid. Devices may recognize a RESET- assertion greater that 20 ns as valid and shall recognize a RESET- assertion equal to or greater than 25 µs as valid.

Transition DHR0:DHR1: When a valid RESET- signal is negated, the device shall make a transition to the DHR1: Release_Bus state.

DHR1: Release_bus State: This state is entered when a valid RESET- signal is negated.

When in this state, the device shall release bus signals PDIAG-, INTRQ, IORDY, DMARQ and DD(15:0) and shall set BSY to one within 400 ns after entering this state. The device shall determine if the device is Device 0 or Device 1 by checking the jumper, switch or CSEL.

Transition DHR1:D0HR0: When the device has determined that the device is Device 0, has released the bus signals and has set BSY to one, then the device shall make a transition to the D0HR0: DASP-_wait state.

Transition DHR1:D1HR0: When the device has determined that the device is Device 1, has released the bus signals and has set BSY to one, then the device shall make a transition to the D1HR0: Set_DASP- state.

D0HR0: DASP-_wait State: This state is entered when the device has released the bus signals, set BSY to one and determined that the device is Device 0.

When in this state, the device shall release DASP- and clear the DEV bit in the Device register to zero within 1 ms of the negation of RESET-.

Transition D0HR0:D0HR1: When at least 1 ms has elapsed since the negation of RESET-, the device shall make a transition to the D0HR1: Sample_DASP- state.

D0HR1: Sample_DASP- State: This state is entered when at least 1 ms has elapsed since the negation of RESET-.

When in this state, the device should begin performing the hardware initialization and self-diagnostic testing. This may revert the device to the default condition (the device's settings may now be different than they were before the host asserted RESET-). All Ultra DMA modes shall be disabled.

When in this state, the device shall sample the DASP- signal.

Transition D0HR1:D0HR2: When the sample indicates that DASP- is asserted, the device shall make a transition to the D0HR2: Sample_PDIAG- state.

Transition D0HR1:D0HR1: When the sample indicates that DASP- is negated and less than 450 ms have elapsed since the negation of RESET-, then the device shall make a transition to the D0HR1: Sample_DASP- state. When the sample indicates that DASP- is negated and greater than 450 ms but less than 5 s have elapsed since the negation of RESET-, then the device may make a transition to the D0HR1: Sample_DASP- state.

Transition D0HR1:D0HR3: When the sample indicates that DASP- is negated and 5 s have elapsed since the negation of RESET-, then the device shall clear bit 7 in the Error register and make a transition to the D0HR3: Set_status state. When the sample indicates that DASP- is negated and greater than 450 ms, but less than 5 s have elapsed since the negation of RESET-, then the device may clear bit 7 in the Error register and make a transition to the D0HR3: Set_status state.

D0HR2: Sample_PDIAG- State: This state is entered when the device has recognized that DASP- is asserted.

When in this state, the device shall sample the PDIAG- signal.

Transition D0HR2a:D0HR3: When the sample indicates that PDIAG- is asserted, the device shall clear bit 7 in the Error register and make a transition to the D0HR3: Set_status state.

Transition D0HR2b:D0HR3: When the sample indicates that PDIAG- is not asserted and 31 s have elapsed since the negation of RESET-, then the device shall set bit 7 in the Error register and make a transition to the D0HR3: Set_status state.

Transition D0HR2:D0HR2: When the sample indicates that PDIAG- is not asserted and less than 31 s have elapsed since the negation of RESET-, then the device shall make a transition to the D0HR2: Sample_PDIAG- state.

D0HR3: Set_status State: This state is entered when bit 7 in the Error register has been set or cleared.

When in this state the device shall complete the hardware initialization and self-diagnostic testing begun in the Sample DASP- state if not already completed.

The EXECUTE DEVICE DIAGNOSTICS diagnostic code shall be placed in bits (6:0) of the Error register (see ISO/IEC 24739-1:2008, Clause 6). The device shall set the signature values (see ISO/IEC 24739-1:2008, Clause 5). The device shall clear the SRST bit to zero in the Device Control register if set set to one. The content of the Features register is undefined. The device shall set word 93 in the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data (see ISO/IEC 24739-1:2008, Clause 6).

If the device does not implement the PACKET command feature set, the device shall clear bits 3, 2 and 0 in the Status register to zero.

If the device implements the PACKET command feature set, the device shall clear bits 6, 5, 4, 3, 2 and 0 in the Status register to zero. The device shall return the operating modes to their specified initial conditions. MODE SELECT conditions shall be restored to their last saved values if saved values have been established. MODE SELECT conditions for which no values have been saved shall be returned to their default values.

Transition D0HR3:DI1: When hardware initialization and self-diagnostic testing is completed and the status has been set, the device shall clear BSY to zero and make a transition to the DI1: Device_idle_S state (see Figure 43).

D1HR0: Set_DASP- State: This state is entered when the device has released the bus, set BSY to one and determined that the device is Device 1.

When in this state, the device shall clear the DEV bit in the Device register to zero within 1 ms and shall assert DASP- within 400 ms of the negation of RESET-.

When in this state, the device should begin execution of the hardware initialization and self-diagnostic testing. The device may revert to the default condition (the device's settings may now be in different conditions than they were before RESET- was asserted by the host). All Ultra DMA modes shall be disabled.

Transition D1HR0:D1HR1: When DASP- has been asserted, the device shall make a transition to the D1HR1: Set_status state.

D1HR1: Set_status State: This state is entered when the device has asserted DASP-.

When in this state the device shall complete any hardware initialization and self-diagnostic testing begun in the Set DASP- state if not already completed. The EXECUTE DEVICE DIAGNOSTICS diagnostic code shall be placed in the Error register (see ISO/IEC 24739-1, Clause 6). If the device passed self-diagnostics, the device shall assert PDIAG-. The device

shall set word 93 in the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data (see ISO/IEC 24739-1:2008, Clause 6).

All actions required in this state shall be completed in ≤30 s.

The device shall set the signature values (see ISO/IEC 24739-1:2008, Clause 5). The content of the Features register is undefined. The device shall clear the SRST bit to zero in the Device Control register if set to one.

If the device does not implement the PACKET command feature set, the device shall clear bits 3, 2 and 0 in the Status register to zero.

If the device implements the PACKET command feature set, the device shall clear bits 6, 5, 4, 3, 2 and 0 in the Status register to zero. The device shall return the operating modes to their specified initial conditions. MODE SELECT conditions shall be restored to their last saved values if saved values have been established. MODE SELECT conditions for which no values have been saved shall be returned to their default values.

Transition D1HR1a:DI2: When hardware initialization and self-diagnostic testing is completed, the device passed its diagnostics and the status has been set, the device shall clear BSY to zero, assert PDIAG- and make a transition to the DI2: Device_idle_NS state (see Figure 43).

Transition D1HR1b:DI2: When hardware initialization and self-diagnostic testing is completed, the device failed its diagnostic and the status has been set, the device shall clear BSY to zero, negate PGIAG- and make a transition to the DI2: Device_idle_NS state (see Figure 43).

11.3 Software reset protocol

This subclause describes the protocol for processing of software reset when the host sets SRST.

If the host sets SRST in the Device Control register to one regardless of the power management mode, the device shall execute the software reset protocol. If the host asserts RESET- before a device has completed the software reset protocol, then the device shall execute the hardware reset protocol from the beginning.

The host should not set the SRST bit to one in the Device Control while the BSY bit is set to one in either device Status register as a result of executing the software reset protocol. If the host sets the SRST bit in the Device Control register to one before devices have completed execution of the software reset protocol, then the devices shall restart execution of the software reset protocol from the beginning. If the host issues a DEVICE RESET command before devices have completed execution of the software reset protocol, the command shall be ignored.

A host should issue an IDENTIFY DEVICE and/or IDENTIFY PACKET DEVICE command after the software reset protocol has completed to determine the current status of features implemented by the device(s).

Figure 38 and the text following the figure decribe the software reset protocol for the host. Figure 39 and the text following the figure describe the software reset protocol for Device 0. Figure 40 and the text following the figure describe the software reset protocol for Device 1.

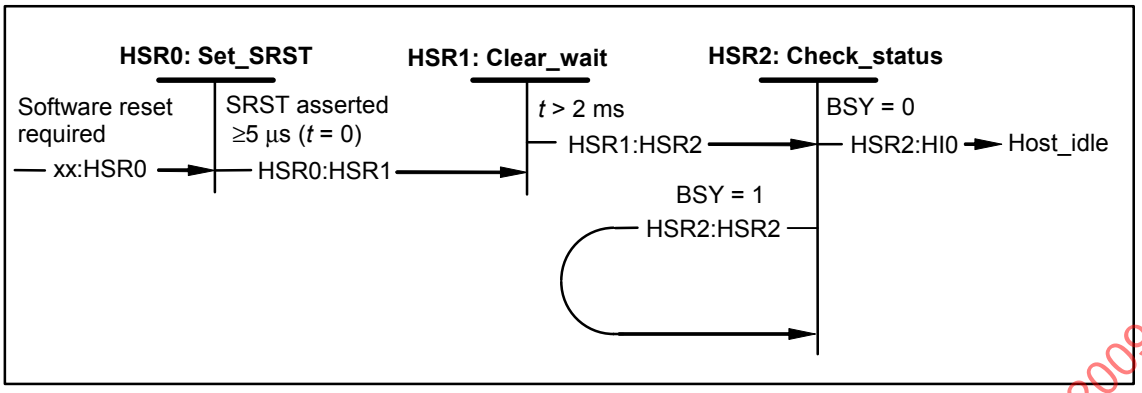


Figure 38 – Host software reset state diagram

HSR0: Set_SRST State: This state is entered when the host initiates a software reset.

When in this state, the host shall set SRST in the Device Control register to one. The SRST bit shall be written to both devices when the Device Control register is written. The host shall remain in this state with SRST set to one for at least 5 µs. The host shall not set SRST to one unless the bit has been cleared to zero for at least 5 µs.

Transition HSR0:HSR1: When the host has had SRST set to one for at least 5 µs, the host shall make a transition to the HSR1: Clear_wait state.

HSR1: Clear_wait State: This state is entered when SRST has been set to one for at least 5 µs.

When in this state, the host shall clear SRST in the Device Control register to zero. The host shall remain in this state for at least 2 ms.

Transition HSR1:HSR2: When SRST has been cleared to zero for at least 2 ms, the host shall make a transition to the HSR2: Check_status state.

HSR2: Check_status State: This state is entered when SRST has been cleared to zero for at least 2 ms.

When in this state the host shall read the Status or Alternate Status register.

Transition HSR2:HSR2: When BSY is set to one, the host shall make a transition to the HSR2: Check_status state.

Transition HSR2:HI0: When BSY is cleared to zero, the host shall check the ending status in the Error register and the signature (see ISO/IEC 24739-1:2008, Clause 5) and make a transition to the HI0: Host_idle state (see Figure 41).

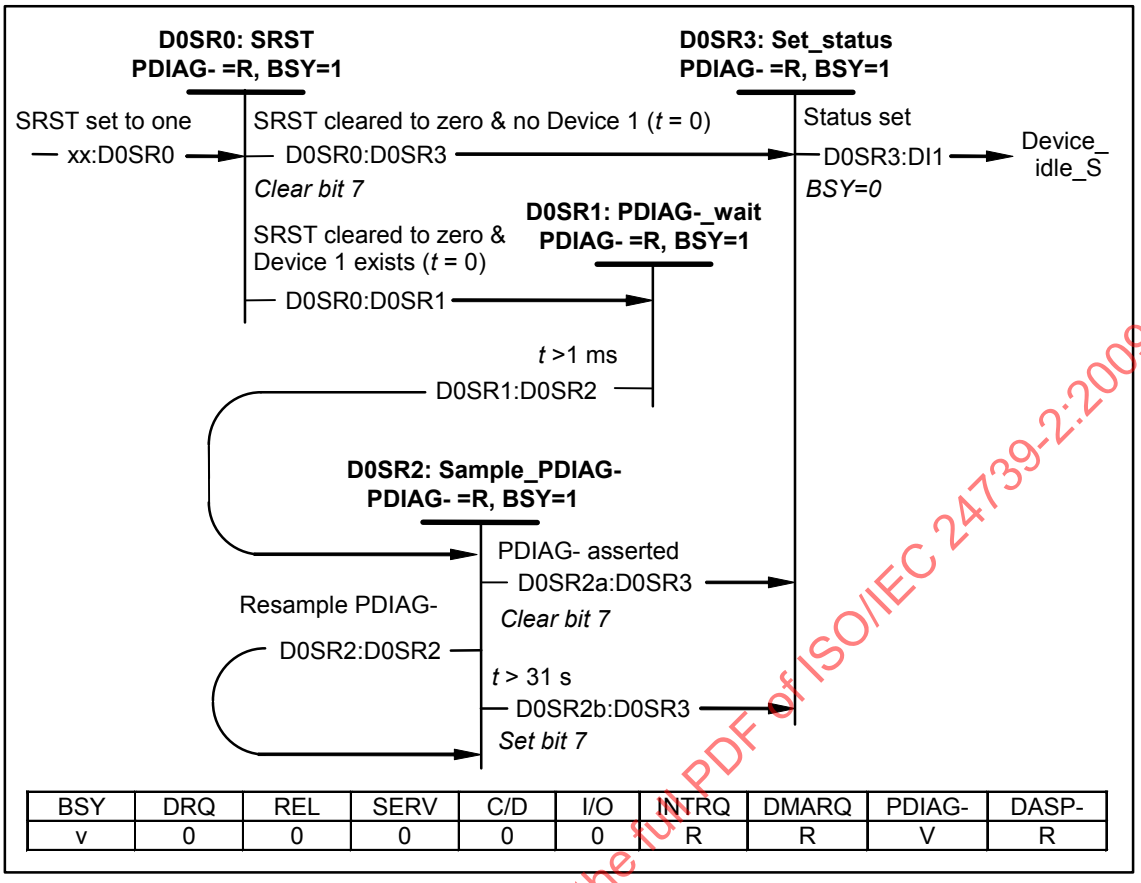


Figure 39 – Device 0 software reset state diagram

D0SR0: SRST State: This state is entered by Device 0 when the SRST bit is set to one in the Device Control register.

When in this state, the device shall release PDIAG-, INTRQ, IORDY, DMARQ and DD(15:0) within 400 ns after entering this state. The device shall set BSY to one within 400 ns after entering this state.

If the device does not implement the PACKET command feature set, the device should begin performing the hardware initialization and self-diagnostic testing. The device may revert to the default condition (the device's setting may now be in different conditions than they were before the SRST bit was set to one by the host). However, an Ultra DMA mode setting (either enabled or disabled) shall not be affected by the host setting SRST to one.

If the PACKET command feature set is implemented, the device may begin performing the hardware initialization and self-diagnostic testing and the device is not expected to stop any background device activity (e.g., immediate command, see MMC-2) that was started prior to the time that SRST was set to one. The device shall not revert to the default condition and an Ultra DMA mode setting (either enabled or disabled) shall not be affected by the host setting SRST to one.

Transition D0SR0:D0SR1: When SRST is cleared to zero and the assertion of DASP- by Device 1 was detected during the most recent power-on or hardware reset, the device shall make a transition to the D0SR1: PDIAG-_wait state.

Transition D0SR0:D0SR3: When SRST is cleared to zero and the assertion of DASP- by Device 1 was not detected during the most recent power-on or hardware reset, the device shall clear bit 7 to zero in the Error register and make a transition to the D0SR3: Set_status state.

D0SR1: PDIAG-_wait State: This state is entered when SRST has been cleared to zero and Device 1 is present.

The device shall remain in this state for at least 1 ms and shall clear the DEV bit in the Device register to zero within 1 ms.

Transition D0SR1:D0SR2: When at least 1 ms has elapsed since SRST was cleared to zero, the device shall make a transition to the D0SR2: Sample_PDIAG- state.

D0SR2: Sample_PDIAG- State: This state is entered when SRST has been cleared to zero for at least 1 ms.

When in this state, the device shall sample the PDIAG- signal.

Transition D0SR2:D0SR2: When the sample indicates that PDIAG- is not asserted and less than 31 s have elapsed since SRST was cleared to zero, then the device shall make a transition to the D0SR2: Sample_PDIAG- state.

Transition D0SR2a:D0SR3: When the sample indicates that PDIAG- is asserted, the device device shall clear bit 7 to zero in the Error register and shall make a transition to the D0SR3: Set_status state.

Transition D0SR2b:D0SR3: When the sample indicates that PDIAG- is not asserted and 31 s have elapsed since SRST was cleared to zero, the device shall set bit 7 to one in the Error register and shall make a transition to the D0SR3: Set_status state.

D0SR3: Set_status State: This state is entered when bit 7 in the Error register has been set or cleared or Device 1 does not exist.

When in this state, the device shall clear the DEV bit in the Device register to zero within 1 ms. The device shall complete any hardware initialization and self-diagnostic testing begun in the SRST state if not already completed.

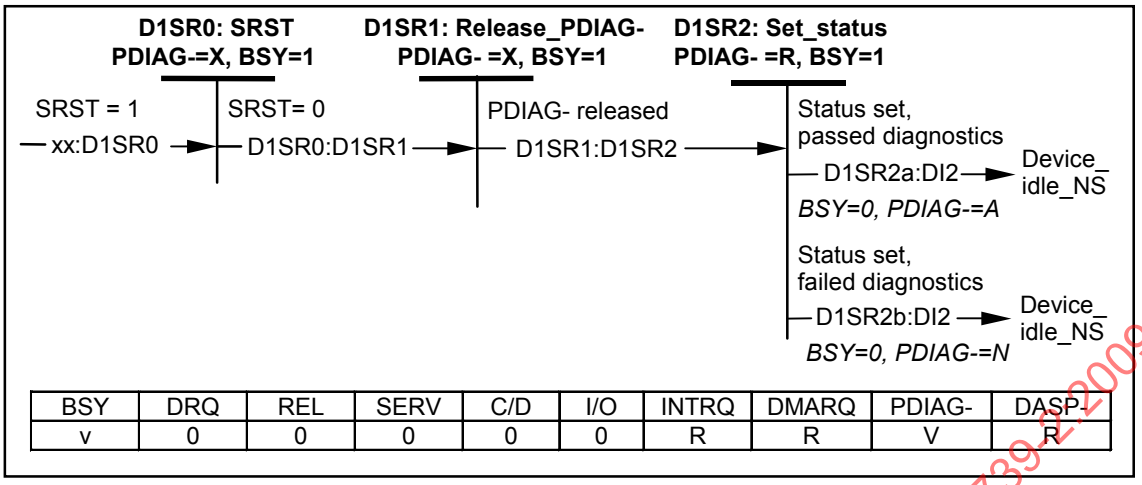
All actions required in this state shall be completed within 31 s.

The EXECUTE DEVICE DIAGNOSTICS diagnostic code shall be placed in bits (6:0) of the Error register (see ISO/IEC 24739-1:2008, Clause 6). The device shall set the signature values (see ISO/IEC 24739-1:2008, Clause 5). The content of the Features register is undefined.

If the device does not implement the PACKET command feature set, the device shall clear bits 3, 2 and 0 in the Status register to zero.

If the device implements the PACKET command feature set, the device shall clear bits 6, 5, 4, 3, 2 and 0 in the Status register to zero. The device shall return the operating modes to their specified initial conditions. MODE SELECT conditions shall be restored to their last saved values if saved values have been established. MODE SELECT conditions for which no values have been saved shall be returned to their default values.

Transition D0SR3:DI1: When hardware initialization and self-diagnostic testing is completed and the status has been set, the device shall clear BSY to zero and make a transition to the DI1: Device_idle_S state (see Figure 43).



BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
v	0	0	0	0	0	R	R	V	R

Figure 40 – Device 1 software reset state diagram

D1SR0: SRST State: This state is entered by Device 1 when the SRST bit is set to one in the Device Control register.

When in this state, the device shall release INTRQ, IORDY, DMARQ and DD(15:0) within 400 ns after entering this state. The device shall set BSY to one within 400 ns after entering this state.

If the device does not implement the PACKET command feature set, the device shall begin performing the hardware initialization and self-diagnostic testing. The device may revert to the default condition (the device's setting may now be in different conditions than they were before the SRST bit was set to one by the host). However, an Ultra DMA mode setting (either enabled or disabled) shall not be affected by the host setting SRST to one.

If the PACKET command feature set is implemented, the device may begin performing the hardware initialization and self-diagnostic testing and the device is not expected to stop any background device activity (e.g., immediate command, see MMC-2) that was started prior to the time that SRST was set to one. The device shall not revert to the default condition and an Ultra DMA mode setting (either enabled or disabled) shall not be affected by the host setting SRST to one.

Transition D1SR0:D1SR1: When SRST is cleared to zero, the device shall make a transition to the D1SR1: Release_PDIAG- state.

D1SR1: Release_PDIAG- State: This state is entered when SRST is cleared to zero.

When in this state, the device shall release PDIAG- and clear the DEV bit in the Device register to zero within 1 ms of entering this state.

Transition D1SR1:D1SR2: When PDIAG- has been released, the device shall make a transition to the D1SR2: Set_status state.

D1SR2: Set_status State: This state is entered when the device has negated PDIAG-.

When in this state the device shall complete the hardware initialization and self-diagnostic testing begun in the SRST state if not already completed. The EXECUTE DEVICE DIAGNOSTICS diagnostic code shall be placed in the Error register (see ISO/IEC 24739-1:2008, Clause 6). If the device passed the self-diagnostics, the device shall assert PDIAG-.

All actions required in this state shall be completed within 30 s.

The device shall set the signature values (see ISO/IEC 24739-1:2008, Clause 5). The contents of the Features register is undefined.

If the device does not implement the PACKET command feature set, the device shall clear bits 3, 2 and 0 in the Status register to zero.

If the device implements the PACKET command feature set, the device shall clear bits 6, 5, 4, 3, 2 and 0 in the Status register to zero. The device shall return the operating modes to their specified initial conditions. MODE SELECT conditions shall be restored to their last saved values if saved values have been established. MODE SELECT conditions for which no values have been saved shall be returned to their default values.

Transition D1SR2a:DI2: When hardware initialization, self-diagnostic testing is completed, the device passed the diagnostics and the status has been set, the device shall clear BSY to zero, assert PDIAG- and make a transition to the DI2: Device_idle_NS state (see Figure 43).

Transition D1SR2b:DI2: When hardware initialization, self-diagnostic testing is completed, the device failed the diagnostics and the status has been set, the device shall clear BSY to zero, negate PDIAG- and make a transition to the DI2: Device_idle_NS state (See Figure 43).

11.4 Bus idle protocol

When the selected device has BSY cleared to zero and DRQ cleared to zero the bus is idle.

If command overlap is implemented and enabled, the host may be waiting for a service request for a released command. In this case, the device is preparing for the data transfer for the released command.

If command overlap and command queuing are implemented and enabled, the host may be waiting for a service request for a number of released commands. In this case, the device is preparing for the data transfer for one of the released commands.

Figure 41 and the text following the figure describe the host state during bus idle for hosts not implementing command overlap and queuing. Figure 42 and the text following the figure describe the additional host state during bus idle required for command overlap and queuing. Figure 43 and the text following the figure describe the device state during bus idle for devices not implementing command overlap and queuing. Figure 44 and the text following the figure describe the additional device state during bus idle required for command overlap and queuing.

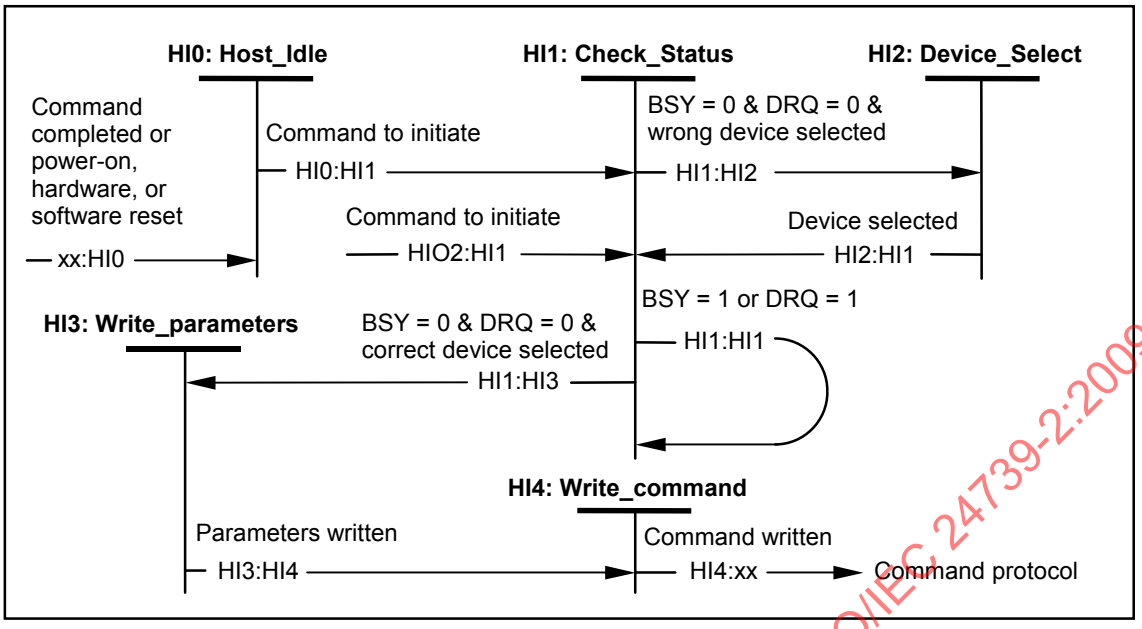


Figure 41 – Host bus idle state diagram

HI0: Host_Idle State: This state is entered when a device completes a command or when a power-on, hardware or software reset has occurred.

When in this state, the host waits for a command to be issued to a device.

Transition HI0:HI1: When the host has a command to issue to a device, the host shall make a transition to the HI1: Check_Status state.

HI1: Check_Status State: This state is entered when the host has a command to issue to a device.

When in this state, the host reads the device Status or Alternate Status register.

Transition HI1:HI2: When the status read indicates that both BSY and DRQ are cleared to zero but the wrong device is selected, then the host shall make a transition to the HI2: Device_Select state.

Transition HI1:HI1: When the status read indicates that either BSY or DRQ is set to one, the host shall make a transition to the HI1: Check_Status state to recheck the status of the selected device.

Transition HI1:HI3: When the status read indicates that both BSY and DRQ are cleared to zero and the correct device is selected, then the host shall make a transition to the HI3: Write_Parameters state.

HI2: Device_Select State: This state is entered when the wrong device is selected for issuing a new command.

When in this state, the host shall write to the Device register to select the correct device.

Transition HI2:HI1: When the Device register has been written to select the correct device, then the host shall make a transition to the HI1: Check_Status state.

HI3: Write_Parameters State: This state is entered when the host has determined that the correct device is selected and both BSY and DRQ are cleared to zero.

When in this state, the host writes all required command parameters to the device Command Block registers (see ISO/IEC 24739-1:2008, Clause 6).

Transition HI3:HI4: When all required command parameters have been written to the device Command Block registers, the host shall make a transition to the HI4: Write_Command state.

HI4: Write_Command State: This state is entered when the host has written all required command parameters to the device Command Block registers.

When in this state, the host writes the command to the device Command register.

Transition HI4:xx: When the host has written the command to the device Command register, the host shall make a transition to the command protocol for the command written as described in 11.5 through 11.12.

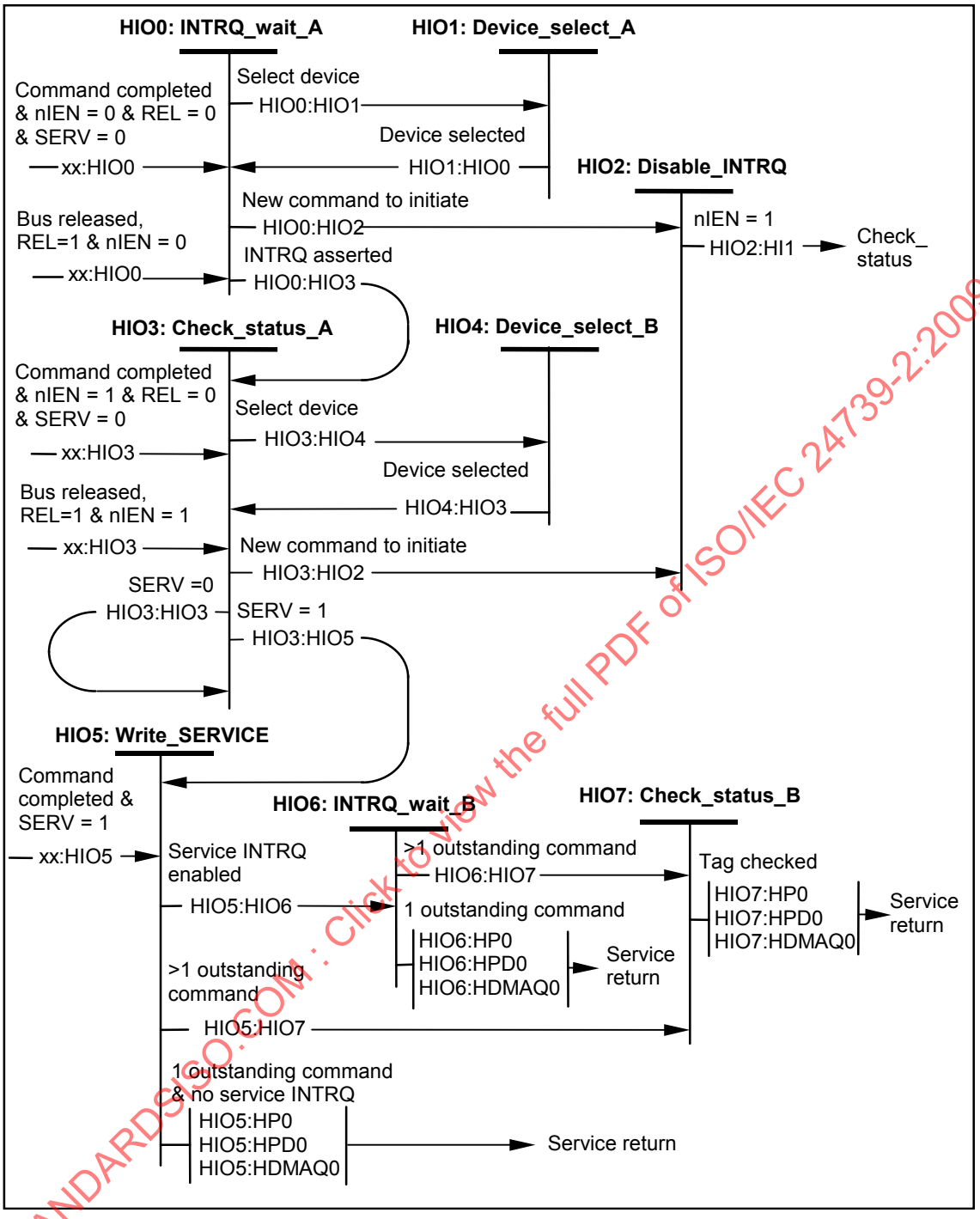


Figure 42 – Additional Host bus idle state diagram with overlap or overlap and queuing

HIO0: INTRQ_wait_A State: This state is entered when a command has completed with nIEN cleared to zero, REL set to one and SERV cleared to zero. This state is entered when the device has released the bus with nIEN cleared to zero. This state is entered when the host is waiting for INTRQ to be asserted for bus released commands.

When in this state, the host waits for INTRQ to be asserted indicating that a device is ready to resume execution of a bus released command.

Transition HIO0:HIO1: When the host has one or more commands outstanding to both devices, the host may make a transition to the HIO1: Device_select_A state to sample INTRQ for the other device.

Transition HIO0:HIO2: When the host has a new command to issue to a device and that device has no command released or supports command queuing, then the host shall make a transition to the HIO2: Disable_INTRQ state.

Transition HIO0:HIO3: When the host detects INTRQ asserted, the host shall make a transition to the HIO3: Check_status A state.

HIO1: Device_select_A State: This state is entered when the host has outstanding, bus released commands to both devices and nIEN is cleared to zero.

When in this state, the host shall disable INTRQ by setting nIEN to one, shall write the Device register to select the other device and then, shall enable INTRQ by clearing nIEN to zero.

Transition HIO1:HIO0: Having selected the other device, the host shall make a transition to the HIO0: INTRQ_wait_A state.

HIO2: Disable_INTRQ State: This state is entered when the host has a new command to issue to a device and that device has no outstanding, bus released command or supports command queuing.

When in this state, the host shall set nIEN to one. nIEN is set to one to prevent a race condition if the host has to select the other device to issue the command.

Transition HIO2:HI1: When nIEN has been set to one, the host shall make a transition to the HI1: Check_status state (see Figure 41).

HIO3: Check_status_A State: This state is entered when a command is completed with nIEN set to one, REL set to one and SERV cleared to zero. This state is entered when the device has released the bus and nIEN is set to one. This state is entered when an interrupt has occured indicating that a device is requesting service.

When in this state, the host shall read the Status register of the device requesting service.

Transition HIO3:HIO4: If SERV is cleared to zero and the host has released commands outstanding to both devices, then the host may make a transition to the HIO4: Device_select_B state.

Transition HIO3:HIO2: If SERV is cleared to zero and the host has a new command to issue to a device, then the host shall make a transition to the HIO2: Disable_INTRQ state.

Transition HIO3:HIO3: If SERV is cleared to zero and the host has no new command to issue, then the host shall make a transition to the HIO3: Check_status state.

Transition HIO3:HIO5: If SERV is set to one, the host shall make a transition to the HIO5: Write_SERVICE state.

HIO4: Device_select_B State: This state is entered when the host has outstanding, bus released commands to both devices and nIEN is set to one.

When in this state, the host shall disable INTRQ by setting nIEN to one, shall write the Device register to select the other device, and then, shall enable INTRQ by clearing nIEN to zero.

Transition HIO4:HIO3: Having selected the other device, the host shall make a transition to the HIO3: Check_status_A state.

HIO5: Write_SERVICE State: This state is entered when a device has set SERV to one indicating that the device requests service. This state is entered when a command has completed with SERV set to one.

When in this state, the host shall write the SERVICE command to the Command register.

Transition HIO5:HIO6: When the device is one that implements the PACKET command feature set and the Service interrupt is enabled, then the host shall make a transition to the HIO6: INTRQ_wait_B state.

Transition HIO5:HIO7: When the host has more than one released command outstanding to the device and the Service interrupt is disabled, the host shall make a transition to the HIO7: Check_status_B state.

Transition HIO5:xx: When the Service interrupt is disabled and the host has only one released command outstanding to the device, the host shall make a transition to the service return for the protocol for the command outstanding (see Figure 53, Figure 55, or Figure 57).

HIO6: INTRQ_wait_B State: This state is entered when the SERVICE command has been written to a device implementing the PACKET command feature set and the Service interrupt is enabled.

NOTE READ DMA QUEUED and WRITE DMA QUEUED commands do not implement the Service interrupt.

When in this state, the host waits for the assertion of INTRQ.

Transition HIO6:HIO7: When the host has more than one released command outstanding to the device and INTRQ is asserted, the host shall make a transition to the HIO7: Check_status_B state.

Transition HIO6:xx: When INTRQ has been asserted and the host has only one released command outstanding to the device, then the host shall make a transition to the service return for the transport protocol of the outstanding command (see Figure 53, Figure 55, or Figure 57).

HIO7: Check_status_B State: This state is entered when the SERVICE command has been written and the host has more than one released command outstanding to the device.

When in this state the host reads the command tag to determine which outstanding command service is requested for. If a DMA data transfer is required for the command, the host shall set up the DMA engine.

Transition HIO7:xx: When the command for which service is requested has been determined, the host shall make a transition to the service return for that command protocol (see Figure 53, Figure 55 or Figure 57).

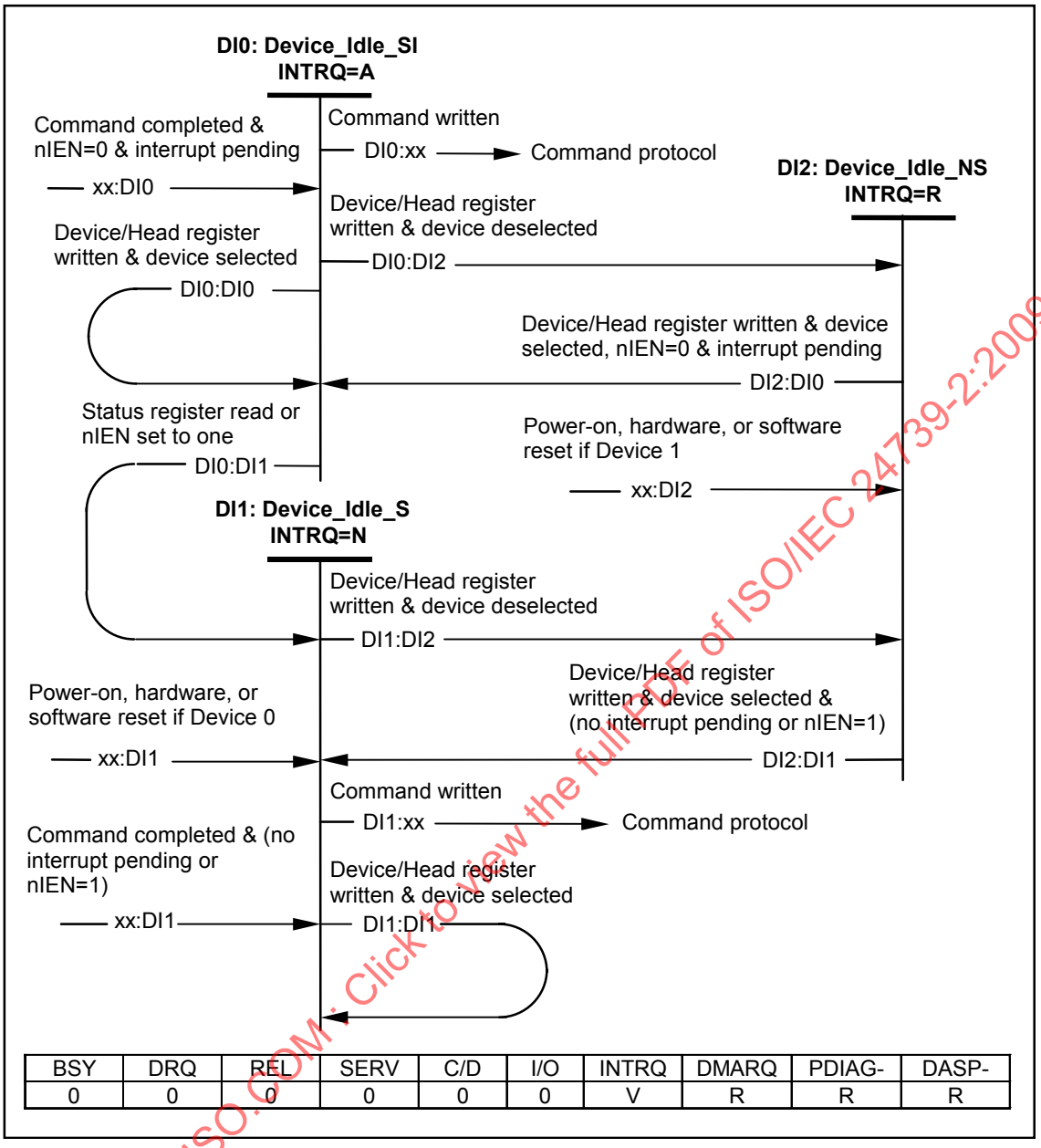


Figure 43 – Device bus idle state diagram

DI0: Device_Idle_SI State (selected/INTRQ asserted)**:** This state is entered when the device has completed the execution of a command protocol with Interrupt Pending and nIEN=0.

When in this state, the device shall have DRQ cleared to zero, INTRQ asserted and BSY cleared to zero. Reading any register except the Status register shall have no effect.

Transition DI0:xx: If the Command register is written, the device shall clear the device internal Interrupt Pending, shall negate or release INTRQ within 400 ns of the negation of DIOW-, shall release PDIAG- and DSAP- if asserted, and shall make a transition to the command protocol indicated by the content of the Command register. The host should not write to the Command register at this time.

Transition DI0:DI1: When the Status register is read, the device shall clear the device internal Interrupt Pending, negate or release INTRQ within 400 ns of the negation of DIOR- and make a transition to the DI1: Device_Idle_S state. When nIEN is set to one in the Device Control register, the device shall negate INTRQ and make a transition to the DI1: Device_Idle_S state.

Transition DI0:DI0: When the Device register is written and the DEV bit selects this device or any other register except the Command register is written, the device shall make a transition to the DI0: Device_Idle_SI state.

Transition DI0:DI2: When the Device register is written and the DEV bit selects the other device, then the device shall release INTRQ within 400 ns of the negation of DIOW- and make a transition to the DI2: Device_Idle_NS state.

DI1: Device_Idle_S State (selected/INTRQ negated)**:** This state is entered when the device has completed the execution of a command protocol with no Interrupt Pending or nIEN = 1, or when a Pending Interrupt is cleared. This state is also entered by Device 0 at the completion of a power-on, hardware or software reset.

When in this state, the device shall have BSY and DRQ cleared to zero and INTRQ negated or released.

When entering this state from a power-on, hardware or software reset, if the device does not implement the PACKET command feature set, the device shall set DRDY to one within 30 s of entering this state. When entering this state from a power-on, hardware or software reset, if the device does implement the PACKET command feature set, the device shall not set DRDY to one.

Transition DI1:xx: When the Command register is written, the device shall exit the Interrupt Pending state, release PDIAG- if asserted and make a transition to the command protocol indicated by the content of the Command register.

Transition DI1:DI1: When the Device register is written and the DEV bit selects this device or any register is written except the Command register, the device shall make a transition to the DI1: Device_Idle_S state.

Transition DI1:DI2: When the Device register is written and the DEV bit selects the other device, the device shall make a transition to the DI2: Device_Idle_NS state.

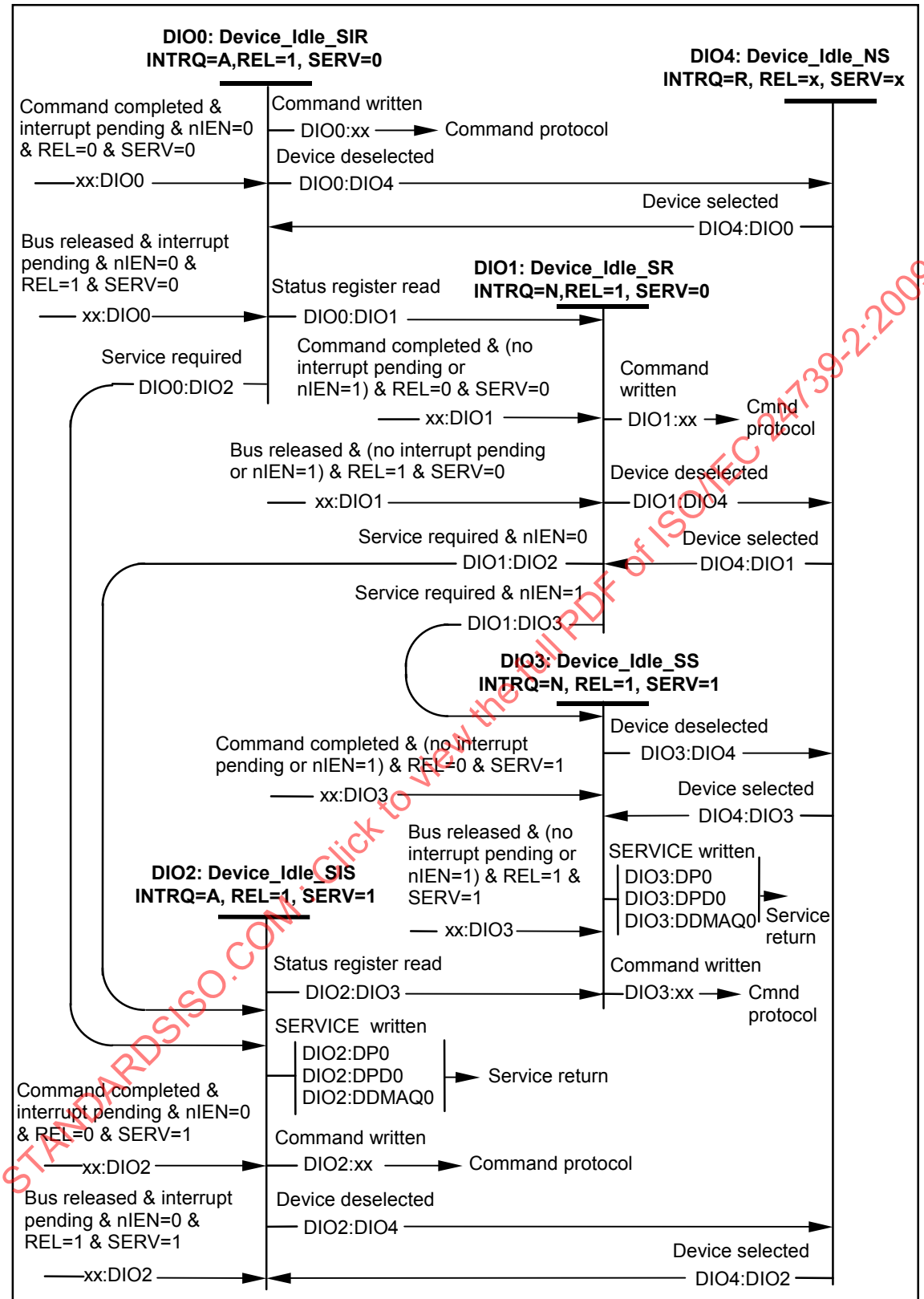
DI2: Device_Idle_NS State (not selected)**:** This state is entered when the device is deselected. This state is also entered by Device 1 at the completion of a power-on, hardware or software reset.

When in this state, the device shall have BSY and DRQ cleared to zero and INTRQ shall be released.

When entering this state from a power-on, hardware or software reset, if the device does not implement the PACKET command feature set, the device shall set DRDY to one within 30 s of entering this state and shall release DASP- and PDIAG- with 31 s of entering this state. When entering this state from a power-on, hardware or software reset, if the device does implement the PACKET command feature set, the device shall not set DRDY to one.

Transition DI2:DI0: When the Device register is written, the DEV bit selects this device, the device has an Interrupt Pending and nIEN is cleared to zero, then the device shall assert INTRQ within 400 ns of the negation of DIOW- and make a transition to the DI0: Device_Idle_SI state.

Transition DI2:DI1: When the Device register is written, the DEV bit selects this device and the device has no Interrupt Pending or nIEN is set to one, then the device shall make a transition to the DI1: Device_Idle_S state.



BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
0	0	v	v	x	x	V	R	R	R

Figure 44 – Additional device bus idle state diagram with overlap or overlap and queuing

DIO0: Device_Idle_SIR State (selected/INTRQ asserted/RELset to one)**:** This state is entered when the device has completed the execution of a command protocol with Interrupt Pending,

nIEN=0, REL set to one and SERV cleared to zero. This state is entered when the device has released an overlapped command with Interrupt Pending, nIEN=0, REL set to one and SERV cleared to zero.

When in this state, the device is preparing for completion of a released command. The device shall have BSY and DRQ cleared to zero and INTRQ asserted.

Transition DIO0:xx: When the Command register is written, the device shall clear the Interrupt Pending, shall negate or release INTRQ within 400 ns of the negation of DIOW- and shall make a transition to the command protocol indicated by the content of the Command register.

NOTE Since a queue exists, only commands in the queued command set may be written to the Command register. If any other command is written to the Command register, the queue is aborted and command aborted is returned for the command see ISO/IEC 24739-1:2008,, Clause 4.

Transition DIO0:DIO1: When the Status register is read, the device shall clear the Interrupt Pending, negate or release INTRQ within 400 ns of the negation of DIOR- and make a transition to the DIO1: Device_Idle_SR state.

Transition DIO0:DIO2: When the Device register is written and the DEV bit selects the other device, then the device shall release INTRQ within 400 ns of the negation of DIOW- and make a transition to the DIO2: Device_Idle_NS state.

Transition DIO0:DIO2: When the device is ready to continue the execution of a released command, the device shall make a transition to the DIO2: Device_idle_SIS state.

DIO1: Device_Idle_SR State (selected/INTRQ negated/REL set to one)**:** This state is entered when the device has completed the execution of a command protocol with no Interrupt Pending or nIEN=1, REL set to one and SERV cleared to zero. This state is entered when the device has released an overlapped command with no Interrupt Pending or nIEN=1, REL set to one and SERV cleared to zero. This state is entered when a pending interrupt is cleared, REL is set to one and SERV is cleared to zero.

When in this state, the device is preparing for completion of a released command. The device shall have BSY and DRQ cleared to zero and INTRQ negated or released.

Transition DIO1:xx: When the Command register is written, the device shall make a transition to the command protocol indicated by the content of the Command register.

NOTE Since a queue exists, only commands in the queued command set may be written to the Command register. If any other command is written to the Command register, the queue is aborted and command aborted is returned for the command (ISO/IEC 24739-1:2008, Clause 4, Overlapped Feature Set).

Transition DIO1:DIO4: When the Device register is written and the DEV bit selects the other device, the device shall make a transition to the DIO4: Device_Idle_NS state.

Transition DIO1:DIO2: When the device is ready to continue the execution of a released command and nIEN=0, the device shall make a transition to the DIO2: Device_idle_SIS state.

Transition DIO1:DIO3: When the device is ready to continue the execution of a released command and nIEN=1, the device shall make a transition to the DIO3: Device_idle_SS state.

DIO2: Device_Idle_SIS State (selected/INTRQ asserted/SERV set to one)**:** This state is entered when the device has completed the execution of a command protocol with Interrupt Pending, nIEN=0, REL set to one and SERV set to one. This state is entered when the device has released an overlapped with Interrupt Pending, nIEN=0, REL set to one and SERV set to one.

Transition DIO2:DIO3: When the Status register is read, the device shall clear the Interrupt Pending, negate or release INTRQ within 400 ns of the negation of DIOR-, and make a transition to the DIO3: Device_Idle_SS state.

Transition DIO2: DIO4: When the Device register is written and the DEV bit selects the other device, the device shall release INTRQ within 400 ns of the negation of DIOW- and make a transition to the DIO4: Device_Idle_NS state.

Transition DIO2:DP0/DPD0/DDMAQ0: When the SERVICE command is written into the Command register, the device shall set the Tag for the command to be serviced, negate or release INTRQ within 400 ns of the negation of DIOW-, and make a transition to the Service return of the command ready for service (see Figure 54, Device PACKET non-data and PIO data command protocol, Figure 56, Device PACKET DMA command protocol or Figure 58, Device DMA QUEUED command protocol).

Transition DIO2:xx: When any overlapped command other than SERVICE is written to the Command register, the device shall negate or release INTRQ within 400 ns of the negation of DIOW- and make a transition to the protocol for the new command.

DIO3: Device_Idle_SS State (selected/INTRQ negated/SERV set to one)**:** This state is entered when the device has completed the execution of a command protocol with no Interrupt Pending or nIEN=1, REL set to one, and SERV set to one. This state is entered when the device has released an overlapped with no Interrupt Pending or nIEN=1, REL set to one and SERV set to one.

Transition DIO3: DIO4: When the Device register is written and the DEV bit selects the other device, the device shall make a transition to the DIO4: Device_Idle_NS state.

Transition DIO3:DP0/DPD0/DDMAQ0: When the SERVICE command is written into the Command register, the device shall set the Tag for the command to be serviced and make a transition to the Service return of the command ready for service (see Figure 54, Figure 56 or Figure 58).

Transition DIO3:xx: When any overlapped command other than SERVICE is written to the Command register, the device shall make a transition to the protocol for the new command.

DIO4: Device_Idle_NS State (not selected)**:** This state is entered when the device is deselected with REL or SERV set to one.

When in this state, the device shall have BSY and DRQ cleared to zero and INTRQ shall be released.

Transition DIO4:DIO0: When the Device register is written, the DEV bit selects this device, the device has an Interrupt Pending, nIEN is cleared to zero, REL is set to one and SERV is cleared to zero, then the device shall assert INTRQ within 400 ns of the negation of DIOW- and make a transition to the DIO0: Device_Idle_SIR state.

Transition DIO4:DIO1: When the Device register is written, the DEV bit selects this device, the device has no Interrupt Pending or nIEN is set to one, REL is set to one and SERV is cleared to zero, then the device shall make a transition to the DIO1: Device_Idle_SIR state.

Transition DIO4:DIO2: When the Device register is written, the DEV bit selects this device, the device has an Interrupt Pending, nIEN is cleared to zero, REL is set to one and SERV is set to one, then the device shall assert INTRQ within 400 ns of the negation of DIOW- and make a transition to the DIO2: Device_Idle_SIS state.

Transition DIO4:DIO3: When the Device register is written, the DEV bit selects this device, the device has no Interrupt Pending or nIEN is set to one, REL is set to one and SERV is set to one, then the device shall make a transition to the DIO3: Device_Idle_SIR state.

11.5 Non-data command protocol

This class includes:

- CFA ERASE SECTORS
- CFA REQUEST EXTENDED ERROR CODE
- CHECK MEDIA CARD TYPE
- CHECK POWER MODE
- CONFIGURE STREAM
- DEVICE CONFIGURATION FREEZE LOCK
- DEVICE CONFIGURATION RESTORE
- FLUSH CACHE
- FLUSH CACHE EXT
- GET MEDIA STATUS
- IDLE
- IDLE IMMEDIATE
- MEDIA EJECT
- MEDIA LOCK
- MEDIA UNLOCK
- NOP
- READ NATIVE MAX ADDRESS
- READ NATIVE MAX ADDRESS EXT
- READ VERIFY SECTOR(S)
- READ VERIFY SECTOR(S) EXT
- SECURITY ERASE PREPARE
- SECURITY FREEZE LOCK
- SET FEATURES
- SET MAX ADDRESS
- SET MAX ADDRESS EXT
- SET MULTIPLE MODE
- SLEEP
- SMART DISABLE OPERATION
- SMART ENABLE/DISABLE AUTOSAVE
- SMART ENABLE OPERATIONS
- SMART EXECUTE OFFLINE IMMEDIATE
- SMART RETURN STATUS
- STANDBY
- STANDBY IMMEDIATE

Execution of these commands involves no data transfer. Figure 45 and the text following the figure describe the host state. Figure 46 and the text following the figure decribe the device state.

See the NOP command description and the SLEEP command in ISO/IEC 24739-1:2008, Clause 6 for additional protocol requirements.

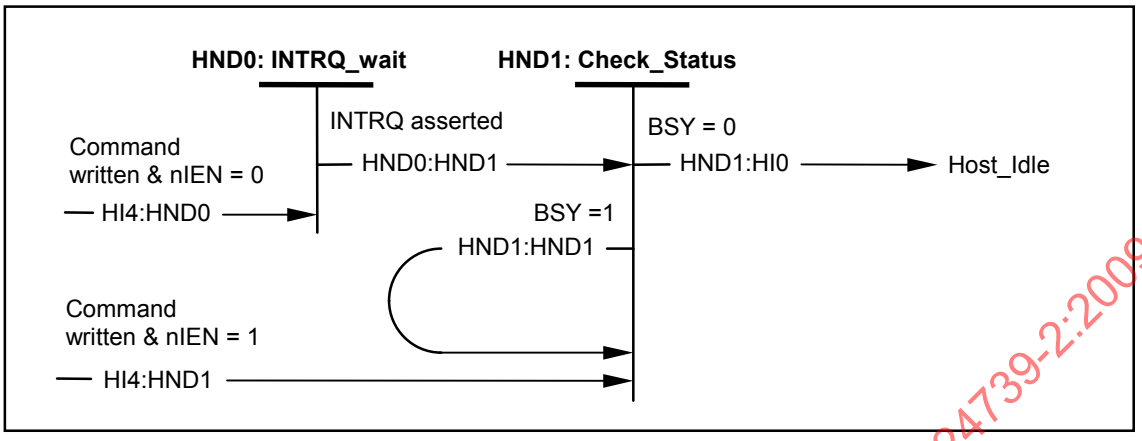


Figure 45 – Host non-data state diagram

HND0: INTRQ_Wait_State: This state is entered when the host has written a non-data command to the device and the nIEN bit in the device has been cleared to zero.

When in this state the host may wait for INTRQ to be asserted by the device.

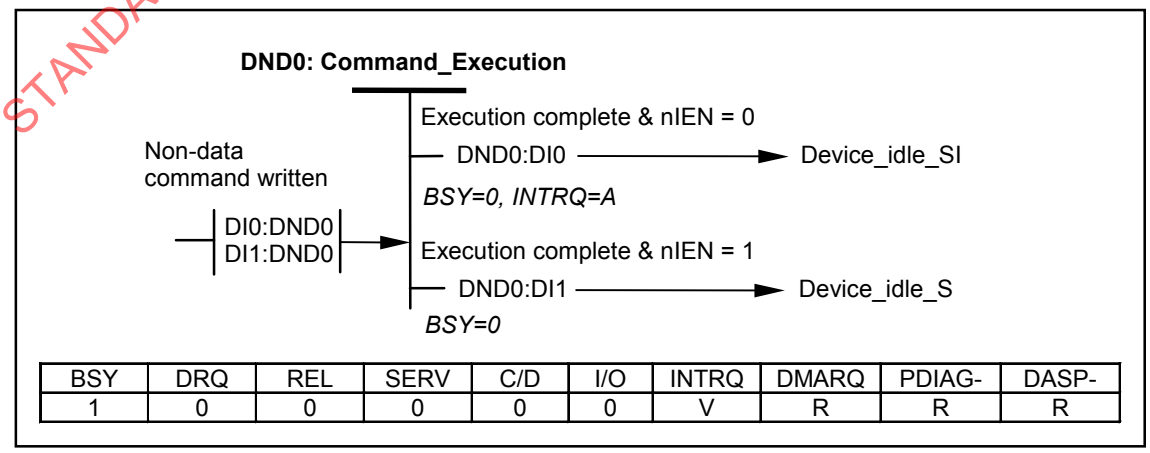
Transition HND0:HND1: When the device asserts INTRQ, the host shall make a transition to the HND1: Check_Status state.

HND1: Check_Status State: This state is entered when the host has written a non-data command to the device and the nIEN bit in the device has been set to one or when INTRQ has been asserted.

When in this state, the host shall read the device Status register. When entering this state from another state other than when an interrupt has occurred, the host shall wait 400 ns before reading the Status register.

Transition HND1:HI0: When the status read indicates that BSY is cleared to zero, the host shall make a transition to the HI0: Host_Idle state (see Figure 41). If status indicates that an error has occurred, the host shall take appropriate error recovery action.

Transition HND1:HND1: When the status read indicates that BSY is set to one, the host shall make a transition to the HND1: Check_Status state to recheck device status.



BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
1	0	0	0	0	0	V	R	R	R

Figure 46 – Device non-data state diagram

DND0: Command_Execution State: This state is entered when a non-data command has been written to the device Command register.

When in this state, the device shall set BSY to one within 400 ns of the writing of the Command register, shall execute the requested command and shall set the Interrupt Pending.

Transition DND0:DI0: When command execution completes and nIEN is cleared to zero, then the device shall set error bits, if appropriate, clear BSY to zero, assert INTRQ and make a transition to the DI0: Device_Idle_SI state (see Figure 43).

Transition DND0:DI1: When command execution completes and nIEN is set to one, the device shall set error bits if appropriate, clear BSY to zero and make a transition to the DI1: Device_Idle_S state (see Figure 43).

11.6 PIO data-in command protocol

This class includes:

- CFA TRANSLATE SECTOR
- DEVICE CONFIGURATION IDENTIFY
- IDENTIFY DEVICE
- IDENTIFY PACKET DEVICE
- READ BUFFER
- READ LOG EXT
- READ MULTIPLE
- READ MULTIPLE EXT
- READ SECTOR(S)
- READ SECTOR(S) EXT
- SMART READ DATA
- SMART READ LOG
- READ STREAM PIO EXT

Execution of this class of command includes the transfer of one or more blocks of data from the device to the host. Figure 47 and the text following the figure describe the host states. Figure 48 and the text following the figure describe the device states.

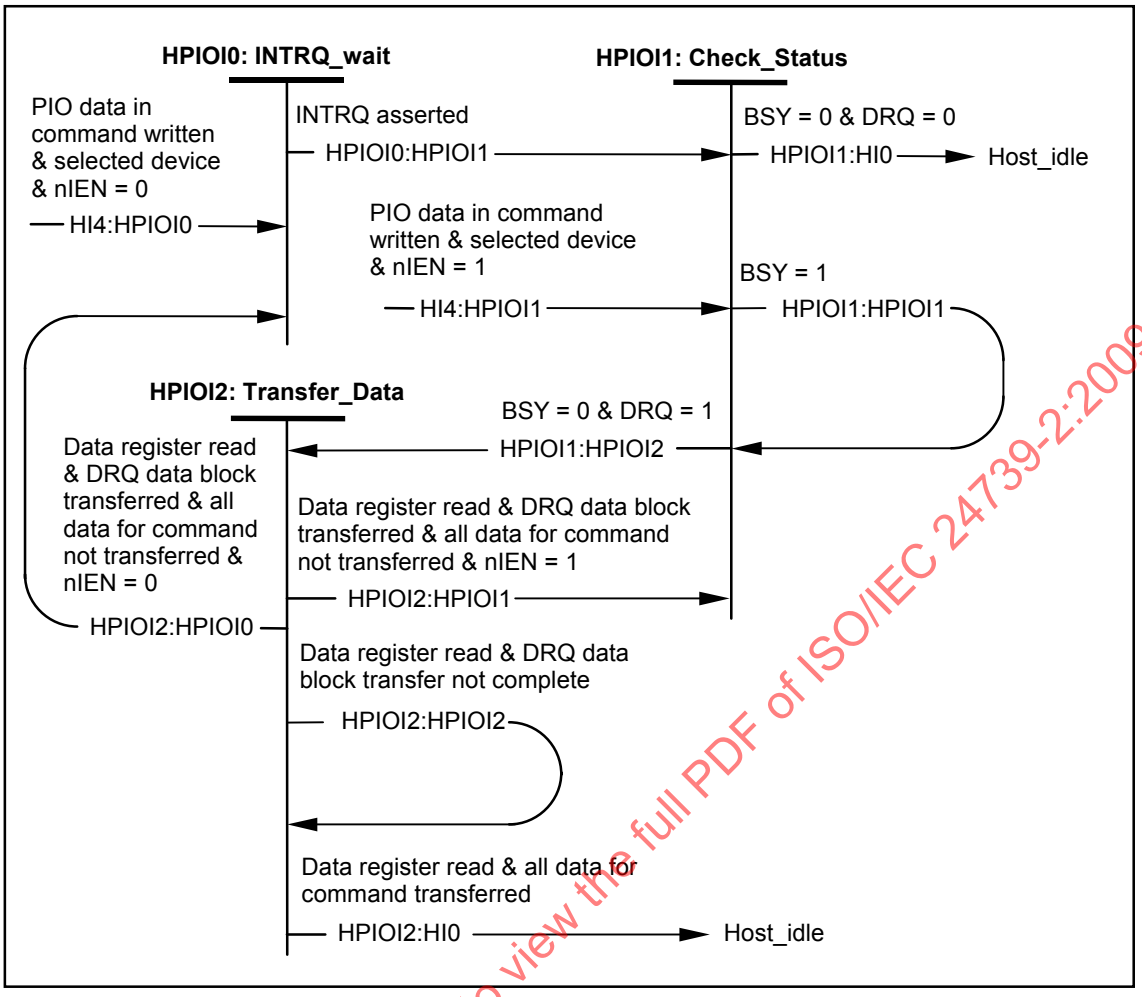


Figure 47 – Host PIO data-in state diagram

HPIOI0: INTRQ_Wait State: This state is entered when the host has written a PIO data-in command to the device and nIEN is cleared to zero, or at the completion of a DRQ data block transfer if all the data for the command has not been transferred and nIEN is cleared to zero.

When in this state, the host shall wait for INTRQ to be asserted.

Transition HPIOI0:HPIOI1: When INTRQ is asserted, the host shall make a transition to the HPIOI1: Check_Status state.

HPIOI1: Check_Status State: This state is entered when the host has written a PIO data-in command to the device and nIEN is set to one or when INTRQ is asserted.

When in this state, the host shall read the device Status register. When entering this state from the HI4 state, the host shall wait 400 ns before reading the Status register. When entering this state from the HPIOI2 state, the host shall wait one PIO transfer cycle time before reading the Status register. The wait may be accomplished by reading the Alternate Status register and ignoring the result.

Transition HPIOI1:HI0: When BSY is cleared to zero and DRQ is cleared to zero, then the device has completed the command with an error. The host shall perform appropriate error recovery and make a transition to the HI0: Host_Idle state (see Figure 41).

Transition HPIOI1:HPIOI1: When BSY is set to one, the host shall make a transition to the HPIOI1: Check_Status state.

Transition HPIOI1:HPIOI2: When BSY is cleared to zero and DRQ is set to one, the host shall make a transition to the HPIOI2: Transfer_Data state.

HPIOI2: Transfer_Data State: This state is entered when the BSY is cleared to zero, DRQ is set to one and the DRQ data block transfer has not completed.

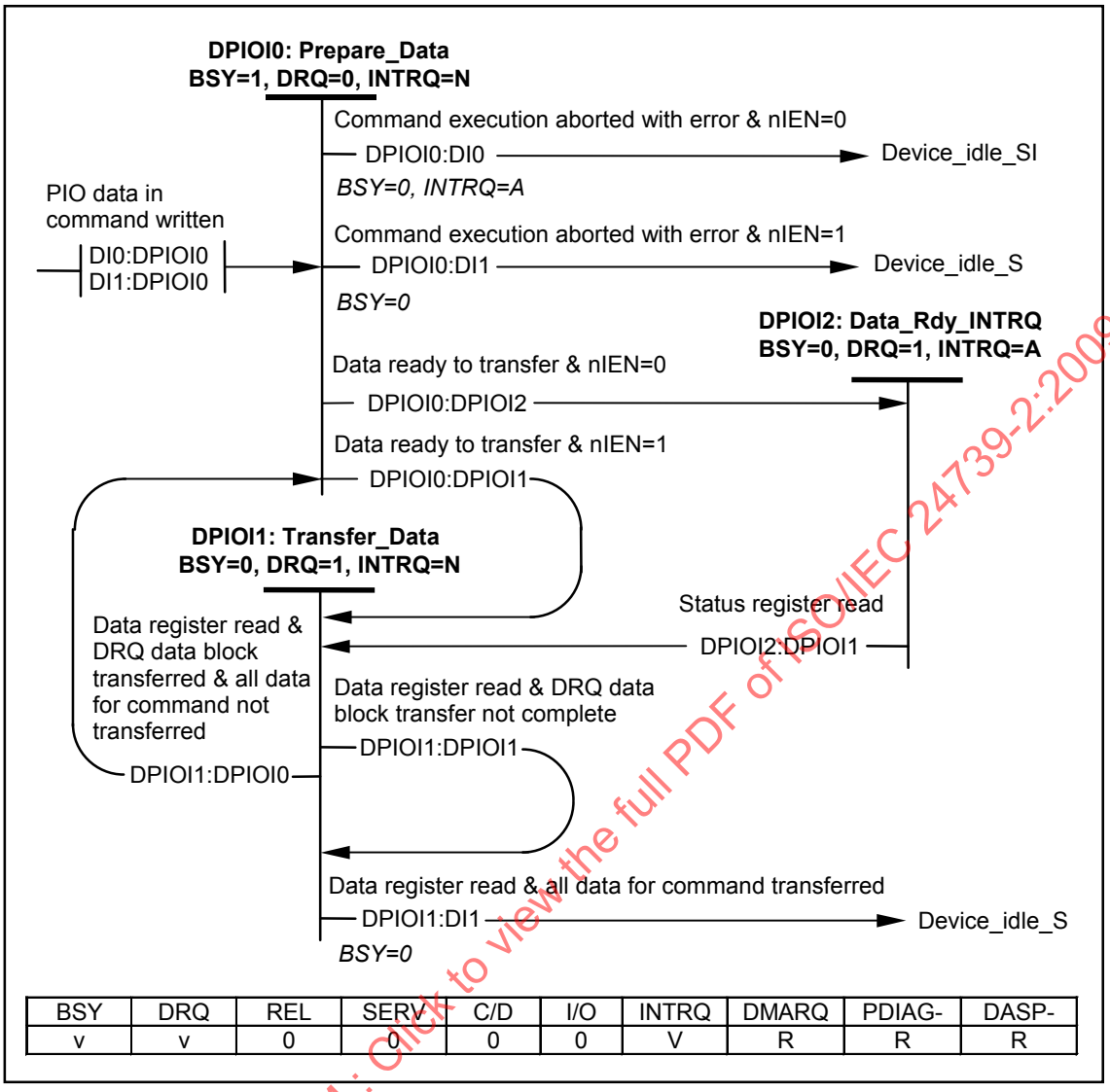
When in this state, the host shall read the device Data register to transfer data.

Transition HPIOI2:HPIOI0: When the host has read the device Data register and the DRQ data block has been transferred, all blocks for the command have not been transferred and nIEN is cleared to zero, then the host shall make a transition to the HPIOI0: INTRQ_Wait state.

Transition HPIOI2:HPIOI1: When the host has read the device Data register and the DRQ data block has been transferred, all blocks for the command have not been transferred and nIEN is set to one, then the host shall make a transition to the HPIOI1: Check_Status state.

Transition HPIOI2:HPIOI2: When the host has read the device status register and the DRQ data block transfer has not completed, then the host shall make a transition to the HPIOI2: Transfer_Data state.

Transition HPIOI2:HI0: When the host has read the device Data register and all blocks for the command have been transferred, then the host shall make a transition to the HI0: Host_Idle state (see Figure 41). The host may read the Status register.



BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
v	v	0	0	0	0	V	R	R	R

Figure 48 – Device PIO data-in state diagram

DPIOI0: Prepare_Data State: This state is entered when the device has a PIO data-in command written to the Command register.

When in this state, device shall set BSY to one within 400 ns of the writing of the Command register and prepare the requested data for transfer to the host.

For IDENTIFY DEVICE and IDENTIFY PACKET DEVICE commands, if the device tests CBLID- it shall do so and update bit 13 in word 93.

Transition DPIOI0:DI0: When an error is detected that causes the command to abort and nIEN is cleared to zero, then the device shall set the appropriate error bits, clear BSY to zero, assert INTRQ and make a transition to the DI0: Device_Idle_SI state (see Figure 43).

Transition DPIOI0:DI1: When an error is detected that causes the command to abort and nIEN is set to one, then the device shall set the appropriate error bits, clear BSY to zero and make a transition to the DI1: Device_Idle_S state (see Figure 43).

Transition DPIOI0:DPIOI1: When the device has a DRQ data block ready to transfer and nIEN is set to one, then the device shall make a transition to the DPIOI1: Transfer_Data state.

Transition DPIOI0:DPIOI2: When the device has a DRQ data block ready to transfer and nIEN is cleared to zero, then the device shall make a transition to the DPIOI2: Data_Ready_INTRQ state.

DPIOI1: Data_Transfer State: This state is entered when the device is ready to transfer a DRQ data block and nIEN is set to one or when the INTRQ indicating that the device is ready to transfer a DRQ data block has been acknowleged by a read of the Status register.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is negated, and the device has a data word ready in the Data register for transfer to the host.

Transition DPIOI1:DPIOI1: When the Data register is read and transfer of the DRQ data block has not completed, then the device shall make a transition to the DPIOI1: Data_Transfer state.

Transition DPIOI1:DPIOI0: When the Data register is read and the transfer of the current DRQ data block has completed, but all blocks for this request have not been transferred, then the device shall make a transition to the DPIOI0: Prepare_Data state.

Transition DPIOI1:DI1: When the Data register is read and all blocks for this request have been transferred, then the device shall clear BSY to zero and make a transition to the DI1: Device_Idle_S state (see Figure 43). The Interrupt Pending is not set on this transition.

DPIOI2: Data_Ready_INTRQ State: This state is entered when the device has a DRQ data block ready to transfer and nIEN is cleared to zero.

When in this state, BSY is cleared to zero, DRQ is set to one and INTRQ is asserted.

Transition DPIOI2:DPIOI1: When the Status register is read, then the device shall clear the Interrupt Pending, negate INTRQ and make a transition to the DPIOI1: Data_Transfer state.

11.7 PIO data-out command protocol

This class includes:

- CFA WRITE MULTIPLE WITHOUT ERASE
- CFA WRITE SECTORS WITHOUT ERASE
- DEVICE CONFIGURATION SET
- DOWNLOAD MICROCODE
- SECURITY DISABLE PASSWORD
- SECURITY ERASE UNIT
- SECURITY SET PASSWORD
- SECUITY UNLOCK
- SMART WRITE LOG
- WRITE BUFFER
- WRITE LOG EXT
- WRITE MULTIPLE
- WRITE MULTIPLE EXT
- WRITE MULTIPLE FUA EXT
- WRITE SECTOR(S)
- WRITE SECTOR(S) EXT
- WRITE STREAM PIO EXT

Execution of this class of command includes the transfer of one or more blocks of data from the host to the device. Figure 49 and the text following the figure describe the host states. Figure 50 and the text following the figure describe the device states.

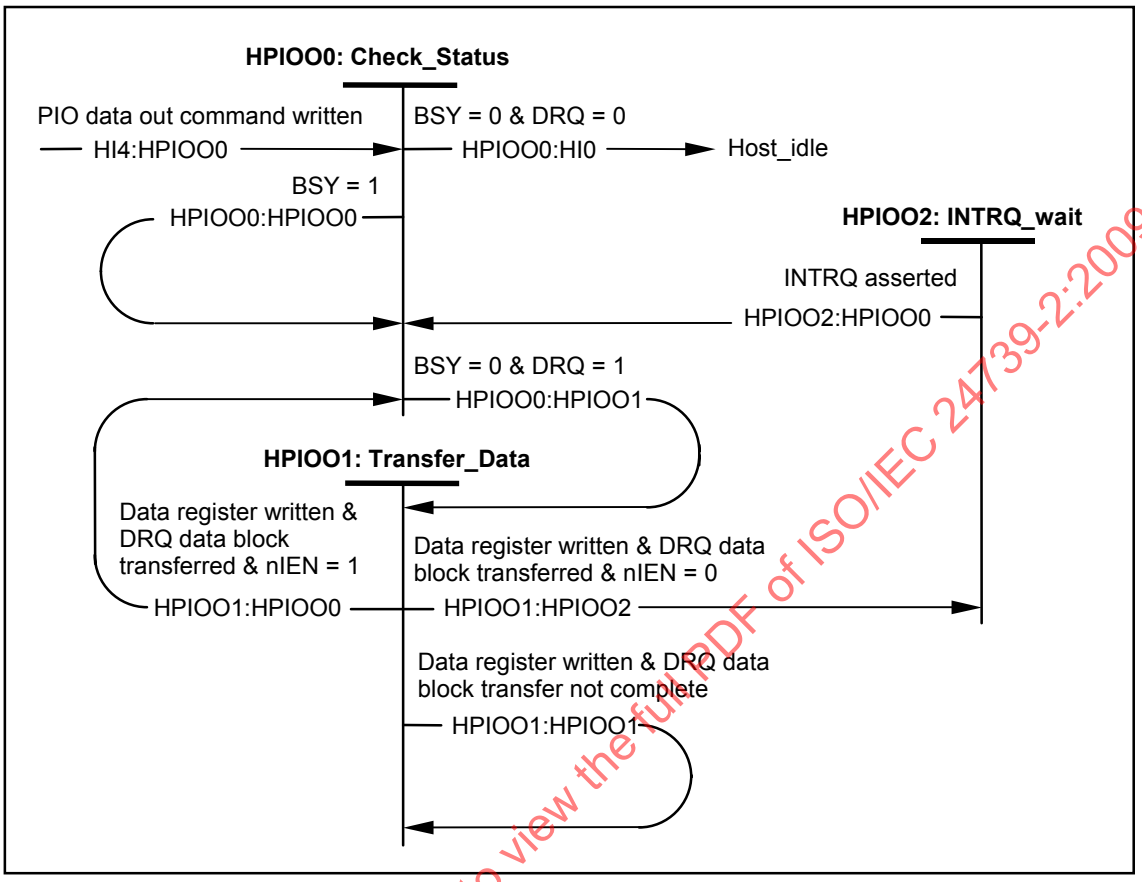


Figure 49 – Host PIO data-out state diagram

HPIOO0: Check_Status State: This state is entered when the host has written a PIO data-out command to the device; when a DRQ data block has been written and nIEN is set to one; or when a DRQ data block has been written, nIEN is cleared to zero and INTRQ has been asserted.

When in this state, the host shall read the device Status register. When entering this state from the HI4 state, the host shall wait 400 ns before reading the Status register. When entering this state from the HPIOO1 state, the host shall wait one PIO transfer cycle time before reading the Status register. The wait may be accomplished by reading the Alternate Status register and ignoring the result.

Transition HPIOO0:HI0: When BSY is cleared to zero and DRQ is cleared to zero, then the device has completed the command and shall make a transition to the HI0: Host_Idle state (see Figure 41). If an error is reported, the host shall perform appropriate error recovery.

Transition HPIOO0:HPIOO0: When BSY is set to one and DRQ is cleared to zero, the host shall make a transition to the HPIOO0: Check_Status state.

Transition HPIOO0:HPIOO1: When BSY is cleared to zero and DRQ is set to one, the host shall make a transition to the HPIOO1: Transfer_Data state.

HPIOO1: Transfer_Data State: This state is entered when the BSY is cleared to zero, DRQ is set to one.

When in this state, the host shall write the device Data register to transfer data.

Transition HPIOO1:HPIOO2: When the host has written the device Data register, the DRQ data block has been transferred and nIEN is cleared to zero, then the host shall make a transition to the HPIOO2: INTRQ_Wait state.

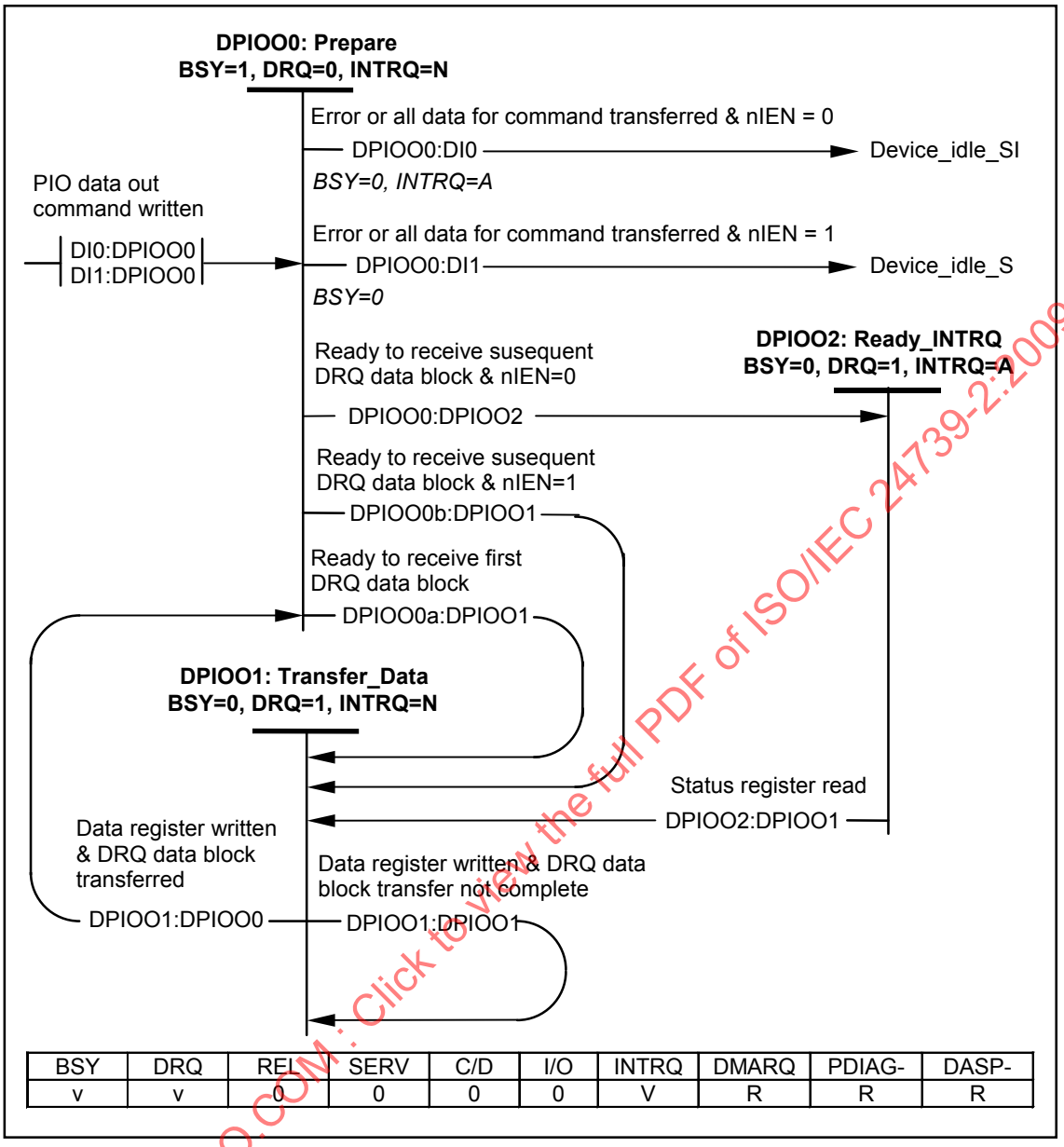
Transition HPIOO1:HPIOO0: When the host has written the device Data register, the DRQ data block has been transferred and nIEN is set to one, then the host shall make a transition to the HPIOO0: Check_Status state.

Transition HPIOO1:HPIOO1: When the host has written the device Data register and the DRQ data block transfer has not completed, then the host shall make a transition to the HPIOO1: Transfer_Data state.

HPIOO2: INTRQ_Wait State: This state is entered when the host has completed a DRQ data block transfer and nIEN is cleared to zero.

When in this state, the host shall wait for INTRQ to be asserted.

Transition HPIOO2:HPIOO0: When INTRQ is asserted, the host shall make a transition to the HPIOO0: Check_Status state.



BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
v	v	0	0	0	0	V	R	R	R

Figure 50 – Device PIO data-out state diagram

DPIOO0: Prepare State: This state is entered when the device has a PIO data-out command written to the Command register or when a DRQ data block has been transferred.

When in this state, device shall set BSY to one within 400 ns of the writing of the Command register, shall clear DRQ to zero and negate INTRQ. The device shall check for errors, determine if the data transfer is complete, and if not, prepare to receive the next DRQ data block.

Transition DPIOO0a:DPIOO1: When the device is ready to receive the first DRQ data block for a command, the device shall make a transition to the DPIOO1: Transfer_Data state.

Transition DPIOO0b:DPIOO1: When the device is ready to receive a subsequent DRQ data block for a command and nIEN is set to one, then the device shall set the Interrupt Pending and make a transition to the DPIOO1: Transfer_Data state.

Transition DPIOO0:DPIOO2: When the device is ready to receive a subsequent DRQ data block for a command and nIEN is cleared to zero, then the device shall set the Interrupt Pending and make a transition to the DPIOO2: Ready_INTRQ state.

Transition DPIOO0:DI0: When all data for the command has been transferred or an error occurs that causes the command to abort and nIEN is cleared to zero, then the device shall set the Interrupt Pending, set appropriate error bits, clear BSY to zero, assert INTRQ and make a transition to the DI0: Device_Idle_SI state (see Figure 43).

Transition DPIOO0:DI1: When all data for the command has been transferred or an error occurs that causes the command to abort and nIEN is set to one, then the device shall set the Interrupt Pending, set appropriate error bits, clear BSY to zero and make a transition to the DI1: Device_Idle_S state (see Figure 43).

DPIOO1: Data_Transfer State: This state is entered when the device is ready to receive a DRQ data block.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is negated and the device receives a data word in the Data register.

Transition DPIOO1:DPIOO1: When the Data register is written and transfer of the DRQ data block has not completed, then the device shall make a transition to the DPIOO1: Data_Transfer state.

Transition DPIOO1:DPIOO0: When the Data register is written and the transfer of the current DRQ data block has completed, then the device shall make a transition to the DPIOO0: Prepare state.

DPIOO2: Ready_INTRQ State: This state is entered when the device is ready to receive a DRQ data block and nIEN is cleared to zero.

When in this state, BSY is cleared to zero, DRQ is set to one and INTRQ is asserted.

Transition DPIOO2:DPIOO1: When the Status register is read, the device shall clear the Interrupt Pending, negate INTRQ and make a transition to the DPIOO1: Data_Transfer state.

11.8 DMA command protocol

This class includes:

- READ DMA
- READ DMA EXT
- READ STREAM DMA EXT
- WRITE DMA
- WRITE DMA EXT
- WRITE DMA FUA EXT
- WRITE STREAM DMA EXT

Execution of this class of command includes the transfer of one or more blocks of data from the host to the device or from the device to the host using DMA transfer. The host shall initialize the DMA channel prior to transferring data. A single interrupt is issued at the completion of the successful transfer of all data required by the command or when the transfer is aborted due to an error. Figure 51 and the text following the figure describe the host states. Figure 52 and the text following the figure describe the device states.

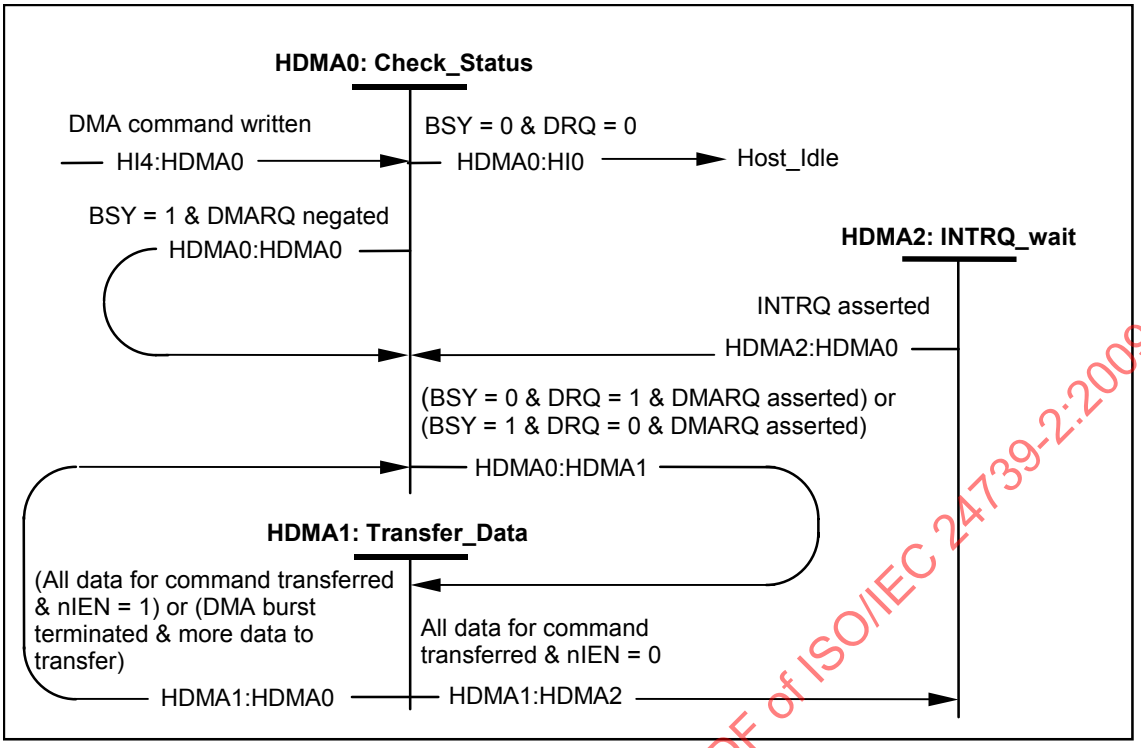


Figure 51 – Host DMA state diagram

HDMA0: Check_Status State: This state is entered when the host has written a DMA command to the device; when all data for the command has been transferred and nIEN is set to one; or when all data for the command has been transferred, nIEN is cleared zero and INTRQ has been asserted.

When in this state, the host shall read the device Status register. When entering this state from the HI4 state, the host shall wait 400 ns before reading the Status register. When entering this state from the HDMA1 state, the host shall wait one PIO transfer cycle time before reading the Status register. The wait may be accomplished by reading the Alternate Status register and ignoring the result.

Transition HDMA0:HI0: When the BSY is cleared to zero and DRQ is cleared to zero, then the device has completed the command and shall make a transition to the HI0: Host_Idle state (see Figure 41). If an error is reported, the host shall perform appropriate error recovery.

Transition HDMA0:HDMA0: When BSY is set to one, DRQ is cleared to zero and DMARQ is negated, then the host shall make a transition to the HDMA0: Check_Status state.

Transition HDMA0:HDMA1: When BSY is cleared to zero, DRQ is set to one and DMARQ is asserted; or if BSY is set to one, DRQ is cleared to zero and DMARQ is asserted, then the host shall make a transition to the HDMA1: Transfer_Data state. The host shall have set up the host DMA engine prior to making this transition.

HDMA1: Transfer_Data State: This state is entered when BSY is cleared to zero, DRQ is set to one and DMARQ is asserted; or BSY is set to one, DRQ is cleared to zero and DMARQ is asserted. The host shall have initialized the DMA channel prior to entering this state.

When in this state, the host shall perform the data transfer as described in the Multiword DMA timing or the Ultra DMA protocol.

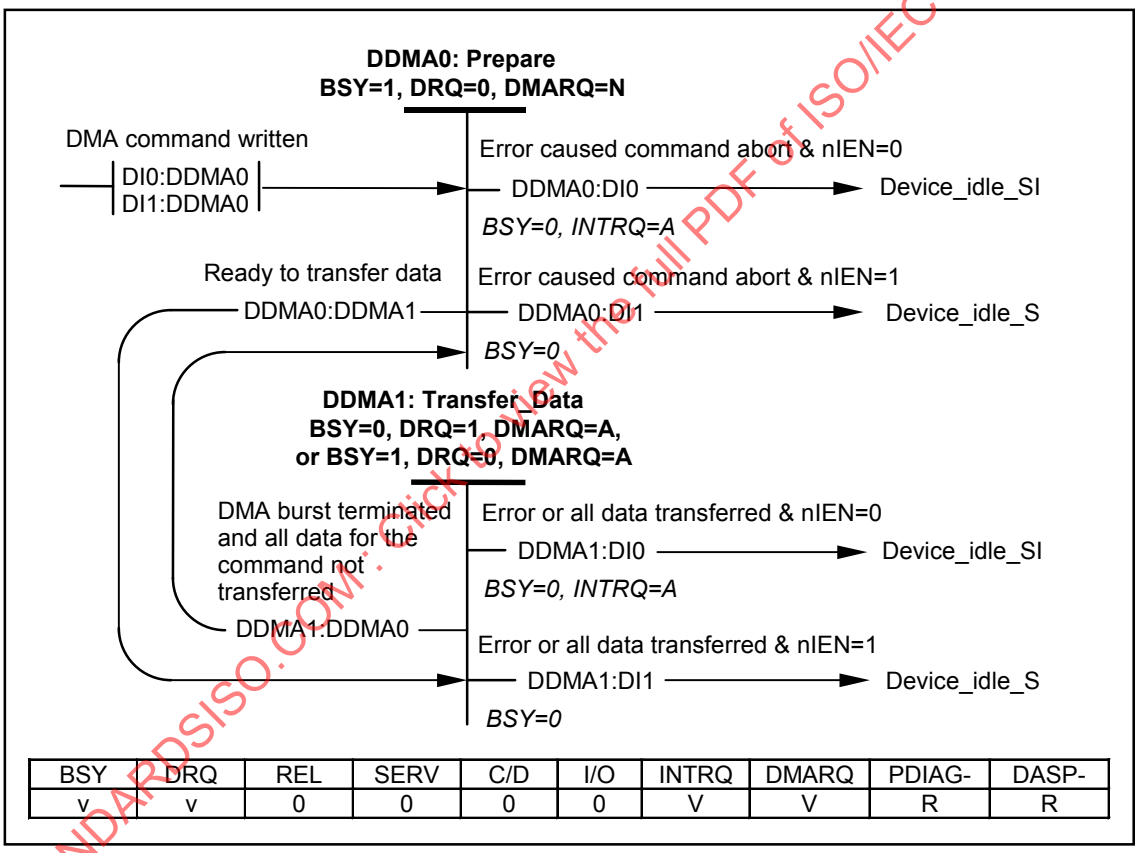
Transition HDMA1:HDMA2: When the host has transferred all data for the command and nIEN is cleared to zero, then the host shall make a transition to the HDMA2: INTRQ_Wait state.

Transition HDMA1:HDMA0: The host shall make a transition to the HDMA0: Check_Status state when (1), the host has transferred all data for the command and nIEN is set to one, or (2), the DMA burst has been terminated and all data for the command has not been transferred.

HDMA2: INTRQ_Wait State: This state is entered when the host has completed the transfer of all data for the command and nIEN is cleared to zero.

When in this state, the host shall wait for INTRQ to be asserted.

Transition HDMA2:HDMA0: When INTRQ is asserted, the host shall make a transition to the HDMA0: Check_Status state.



BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
v	v	0	0	0	0	V	V	R	R

Figure 52 – Device DMA state diagram

DDMA0: Prepare State: This state is entered when the device has a DMA command written to the Command register.

When in this state, the device shall set BSY to one, shall clear DRQ to zero and negate INTRQ. The device shall check for errors and prepare to transfer data.

Transition DDMA0:DI0: When an error is detected that causes the command to abort and nIEN is cleared to zero, the device shall set the appropriate error bits, enter the Interrupt Pending state and make a transition to the DI0: Device_Idle_SI state (see Figure 43).

Transition DDMA0:DI1: When an error is detected that causes the command to abort and nIEN is set to one, then the device shall set the appropriate error bits, enter the Interrupt Pending state and make a transition to the DI1: Device_Idle_S state (see Figure 43).

Transition DDMA0:DDMA1: When the device is ready to transfer data for the command, the device shall make a transition to the DDMA1: Transfer_Data state.

DDMA1: Data_Transfer State: This state is entered when the device is ready to transfer data.

When in this state, BSY is cleared to zero, DRQ is set to one and INTRQ is negated; or BSY is set to one, DRQ is cleared to zero and INTRQ is negated. Data is transferred as decribed in Multiword DMA timing or Ultra DMA protocol.

Transition DDMA1:DDMA0: When the DMA burst is terminated and all data for the command has not been transferred, the device shall make a transition to the DDMA0: Prepare state.

Transition DDMA1:DI0: When the data transfer has completed or the device chooses to abort the command due to an error and nIEN is cleared to zero, then the device shall set error bits if appropriate, enter the Interrupt Pending state and make a transition to the DI0: Device_Idle_SI state (see Figure 43).

Transition DDMA2:DI1: When the data transfer has completed or the device chooses to abort the command due to an error and nIEN is set to one, then the device shall set error bits if appropriate, enter the Interrupt Pending state and make a transition to the DI1: Device_Idle_S state (see Figure 43).

11.9 PACKET command protocol

This class includes:

- PACKET

The PACKET command has a set of protocols for non-DMA data transfer commands and a set of protocols for DMA data transfer commands. Figure 53 and the text following the figure describe the host protocol for the PACKET command when non-data, PIO data-in or PIO data-out is requested. Figure 54 and the text following the figure describe the device protocol for the PACKET command when non-data, PIO data-in or PIO data-out is requested. Figure 55 and the text following the figure describe the host protocol for the PACKET command when DMA data transfer is requested. Figure 56 and the text following the figure describe the device protocol for the PACKET command when DMA data transfer is requested.

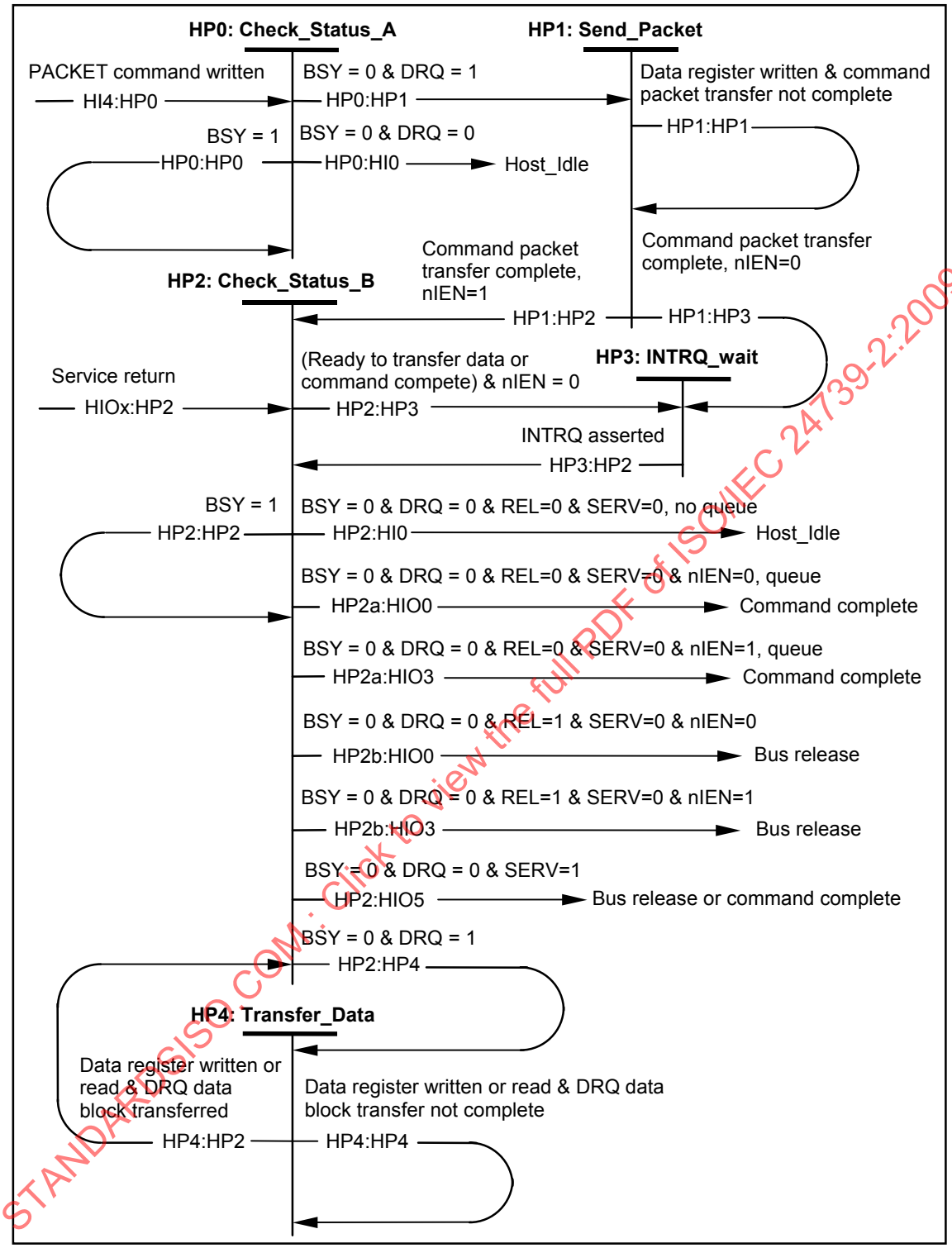


Figure 53 – Host PACKET non-data and PIO data command state diagram

HP0: Check_Status_A State: This state is entered when the host has written a PACKET command to the device.

When in this state, the host shall read the device Status register. When entering this state from the HI4 state, the host shall wait 400 ns before reading the Status register.

Transition HP0:HP0: When BSY is set to one, the host shall make a transition to the HP0: Check_Status_A state.

Transition HP0:HP1: When BSY is cleared to zero and DRQ is set to one, then the host shall make a transition to the HP1: Send_Packet state.

Transition HP0:HI0: When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero and SERV is cleared to zero, then the command is completed and the host shall make a transition to the HI0: Host_Idle state (see Figure 41). If an error is reported, the host shall perform appropriate error recovery.

HP1: Send_Packet State: This state is entered when BSY is cleared to zero and DRQ is set to one.

When in this state, the host shall write a byte of the command packet to the Data register.

Transition HP1:HP1: When the Data register has been written and the writing of the command packet is not completed, the host shall make a transition to the HP1: Send_Packet state.

Transition HP1:HP2: When the Data register has been written, the writing of the command packet is completed and nIEN is set to one, the host shall make a transition to the HP2: Check_Status_B state.

Transition HP1:HP3: When the Data register has been written, the writing of the command packet is completed and nIEN is cleared to zero, the host shall make a transition to the HP3: INTRQ wait state.

HP2: Check_Status_B State: This state is entered when the host has written the command packet to the device, when INTRQ has been asserted, when a DRQ data block has been transferred or from a service return.

When in this state, the host shall read the device Status register. When entering this state from the HP1 or HP4 state, the host shall wait one PIO transfer cycle time before reading the Status register. The wait may be accomplished by reading the Alternate Status register and ignoring the result.

Transition HP2:HP2: When BSY is set to one and DRQ is cleared to zero, the host shall make a transition to the HP2: Check_Status_B state.

Transition HP2:HP3: When the host is ready to transfer data or the command is complete and nIEN is cleared to zero, then the host shall make a transition to the HP3: INTRQ_Wait state.

Transition HP2:HP4: When BSY is cleared to zero and DRQ is set to one, then the host shall make a transition to the HP4: Transfer_Data state.

Transition HP2:HI0: When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero and the device queue is empty, then the command is completed and the host shall make a transition to the HI0: Host_Idle state (see Figure 41). If an error is reported, the host shall perform appropriate error recovery.

Transition HP2a:HIO0: When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, nIEN is cleared to zero and the device has a queue of released commands, then the command is completed and the host shall make a transition to the HIO0: Command completed state (see Figure 42). If an error is reported, the host shall perform appropriate error recovery.

Transition HP2a:HIO3: When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, nIEN is set to one and the device has a queue of released commands, then the command is completed and the host shall make a transition to the HIO3:

Command completed state (see Figure 42). If an error is reported, the host shall perform appropriate error recovery.

Transitions HP2b:HIO0: When BSY is cleared to zero, DRQ is cleared to zero, REL is set to one, SERV is cleared to zero and nIEN is cleared to zero, then the host shall make a transition to the HIO0: INTRQ_wait_A state (see Figure 42). The bus has been released.

Transitions HP2b:HIO3: When BSY is cleared to zero, DRQ is cleared to zero, REL is set to one, SERV is cleared to zero and nIEN is set to one, then the host shall make a transition to the HIO3: Check_status_A state (see Figure 42). The bus has been released.

Transitions HP2:HIO5: When BSY is cleared to zero, DRQ is cleared to zero and SERV is set to one, then the host shall make a transition to the HIO5: Write_SERVICE state (see Figure 42). The command is completed or the bus has been released and another queued command is ready for service. If an error is reported, the host shall perform appropriate error recovery.

HP3: INTRQ_Wait State: This state is entered when the command packet has been transmitted, the host is ready to transfer data or when the command has completed and nIEN is cleared to zero.

When in this state, the host shall wait for INTRQ to be asserted.

Transition HP3:HP2: When INTRQ is asserted, the host shall make a transition to the HP2: Check_Status_B state.

HP4: Transfer_Data State: This state is entered when BSY is cleared to zero, DRQ is set to one and C/D is cleared to zero.

When in this state, the host shall read the byte count then read or write the device Data register to transfer data. If the bus has been released, the host shall read the Sector Count register to determine the tag for the queued command to be executed.

Transition HP4:HP2: When the host has read or written the device Data register and the DRQ data block has been transferred, then the host shall make a transition to the HP2: Check_Status_B state.

Transition HP4:HP4: When the host has read or written the device status register and the DRQ data block transfer has not completed, then the host shall make a transition to the HP4: Transfer_Data state.

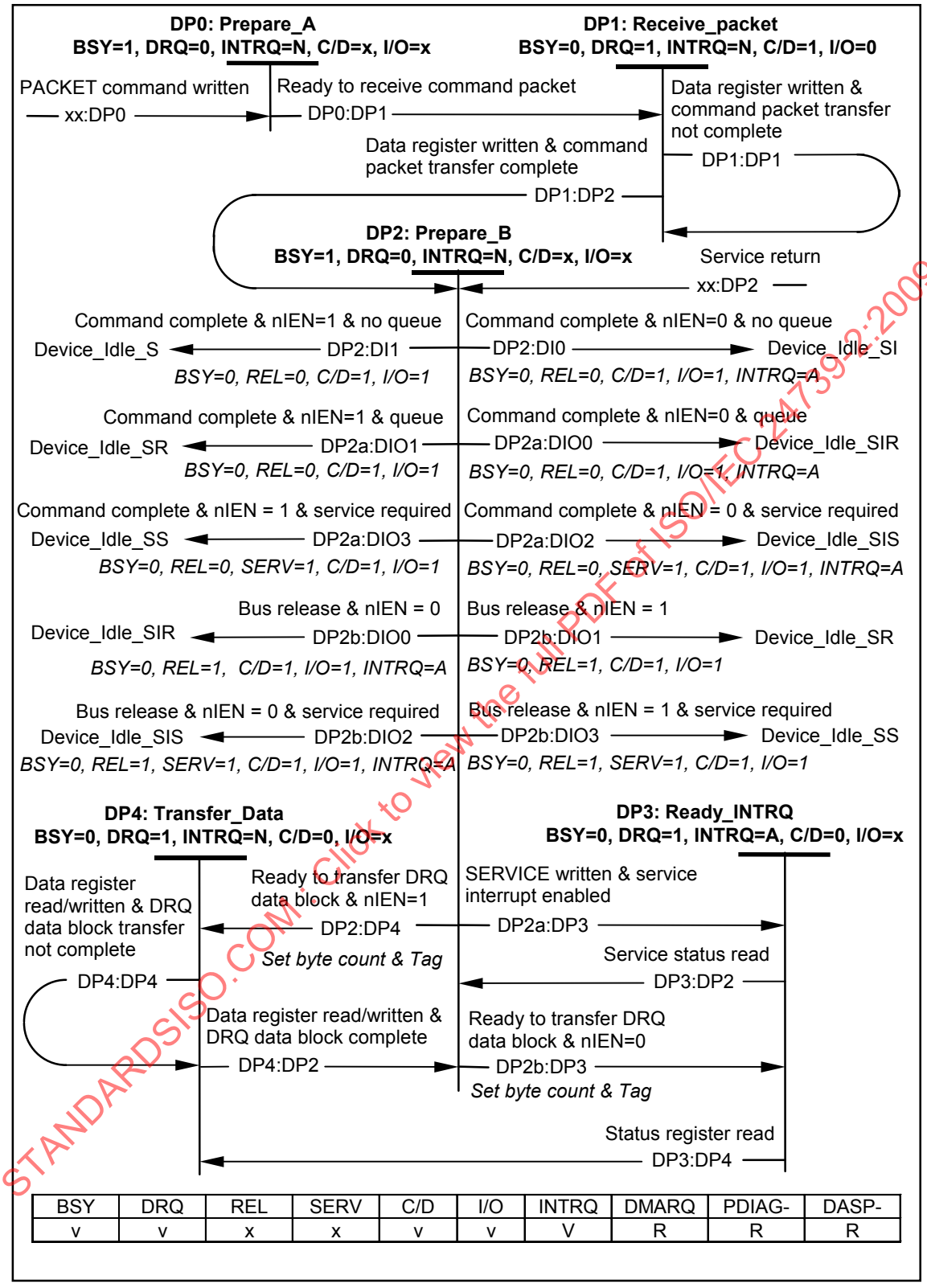


Figure 54 – Device PACKET non-data and PIO data command state diagram

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DP0: Prepare_A State: This state is entered when the device has a PACKET written to the Command register.

When in this state, device shall set BSY to one, clear DRQ to zero and negate INTRQ within 400 ns of the receipt of the command and shall prepare to receive a command packet. If the command is a queued command, the device shall verify that the tag is valid.

Transition DP0:DP1: When the device is ready to receive the command packet for a command, the device shall make a transition to the DP1: Receive_Packet state.

DP1: Receive_Packet State: This state is entered when the device is ready to receive the command packet.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is negated, C/D is set to one, I/O is cleared to zero and REL is cleared to zero. When in this state, the device Data register is written.

Transition DP1:DP1: If the Data register is written and the entire command packet has not been received, then the device shall make a transition to the DP1: Receive_Packet state.

Transition DP1:DP2: When the Data register is written and the entire command packet has been received, then the device shall make a transition to the DP2: Prepare_B state.

DP2: Prepare_B State: This state is entered when the command packet has been received or from a Service return.

When in this state, device shall set BSY to one, clear DRQ to zero and negate INTRQ. Non-data transfer commands shall be executed while in this state. For data transfer commands, the device shall check for errors, determine if the data transfer is complete and if not, prepare to transfer the next DRQ data block.

If the command is overlapped and the release interrupt is enabled, the device shall bus release as soon as the command packet has been received.

Transition DP2:DP4: When the device is ready to transfer a DRQ data block for a command and nIEN is set to one, then the device shall set the command Tag and byte count, set the Interrupt Pending and make a transition to the DP4: Transfer_Data state.

Transition DP2b:DP3: When the device is ready to transfer a DRQ data block for a command and nIEN is cleared to zero, then the device shall set the command Tag and byte count, set the Interrupt Pending and make a transition to the DP3: Ready_INTRQ state.

Transition DP2a:DP3: When the service interrupt is enabled and the device has SERVICE written to the Command register, then the device shall set the command Tag and byte count and make a transition to the DP3: Ready_INTRQ state.

Transition DP2:DI0: When the command has completed or an error occurs that causes the command to abort, the device has no other command released and nIEN is cleared to zero, then the device shall set the Interrupt Pending, set appropriate error bits, set C/D and I/O to one, clear BSY to zero and make a transition to the DI0: Device_Idle_SI state (see Figure 43).

Transition DP2:DI1: When the command has completed or an error occurs that causes the command to abort, the device has no other command released and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, clear BSY to zero and make a transition to the DI1: Device_Idle_S state (see Figure 43).

Transition DP2a:DIO0: When the command has completed or an error occurs that causes the command to abort, the device has another command released but not ready for service and nIEN is cleared to zero, then the device shall set the Interrupt Pending, set appropriate error bits, set C/D and I/O to one, clear BSY to zero and make a transition to the DIO0: Device_Idle_SIR state (see Figure 44).

Transition DP2a:DIO1: When the command has completed or an error occurs that causes the command to abort, the device has another command released but not ready for service and

nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, clear BSY to zero and make a transition to the DIO1: Device_Idle_SR state (see Figure 44).

Transition DP2a:DIO2: When the command has completed or an error occurs that causes the command to abort, the device has another command ready for service and nIEN is cleared to zero, then the device shall set the Interrupt Pending, set appropriate error bits, set C/D and I/O to one, set SERV to one, clear BSY to zero and make a transition to the DIO2: Device_Idle_SIS state (see Figure 44).

Transition DP2a:DIO3: When the command has completed or an error occurs that causes the command to abort, the device has another command ready for service and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, set SERV to one, clear BSY to zero and make a transition to the DIO3: Device_Idle_SS state (see Figure 44).

Transition DP2b:DIO0: When the command is released and nIEN is cleared to zero, then the device shall set the Interrupt Pending, set appropriate error bits, set C/D and I/O to one, set REL to one, clear BSY to zero and make a transition to the DIO0: Device_Idle_SIR state (see Figure 44).

Transition DP2b:DIO1: When the command is released and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, set REL to one, clear BSY to zero and make a transition to the DIO1: Device_Idle_SR state (see Figure 44).

Transition DP2b:DIO2: When the command is released, the device has another command ready for service and nIEN is cleared to zero, then the device shall set the Interrupt Pending, set appropriate error bits, set C/D and I/O to one, set REL to one, set SERV to one, clear BSY to zero and make a transition to the DIO2: Device_Idle_SIS state (see Figure 44).

Transition DP2b:DIO3: When the command is released, the device has another command ready for service and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, set REL to one, set SERV to one, clear BSY to zero and make a transition to the DIO3: Device_Idle_SS state (see Figure 44).

DP3: Ready_INTRQ State: This state is entered when the device is ready to transfer a DRQ data block and nIEN is cleared to zero. This state is entered to interrupt upon receipt of a SERVICE command when service interrupt is enabled.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is asserted, C/D is cleared to zero and I/O is set to one for PIO data-out or cleared to zero for PIO data-in.

Transition DP3:DP2: When the Status register is read to respond to a service interrupt, the device shall make a transition to the DP2: Prepare_B state.

Transition DP3:DP4: When the Status register is read when the device is ready to transfer data, then the device shall clear the Interrupt Pending, negate INTRQ and make a transition to the DP4: Data_Transfer state.

DP4: Data_Transfer State: This state is entered when the device is ready to transfer a DRQ data block.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is negated, C/D is cleared to zero, I/O is set to one for PIO data-out or cleared to zero for PIO data-in, and a data word is read/written in the Data register.

Transition DP4:DP4: When the Data register is read/written and transfer of the DRQ data block has not completed, then the device shall make a transition to the DP4: Data_Transfer state.

Transition DP4:DP2: When the Data register is read/written and the transfer of the current DRQ data block has completed, then the device shall make a transition to the DP2: Prepare_B state.

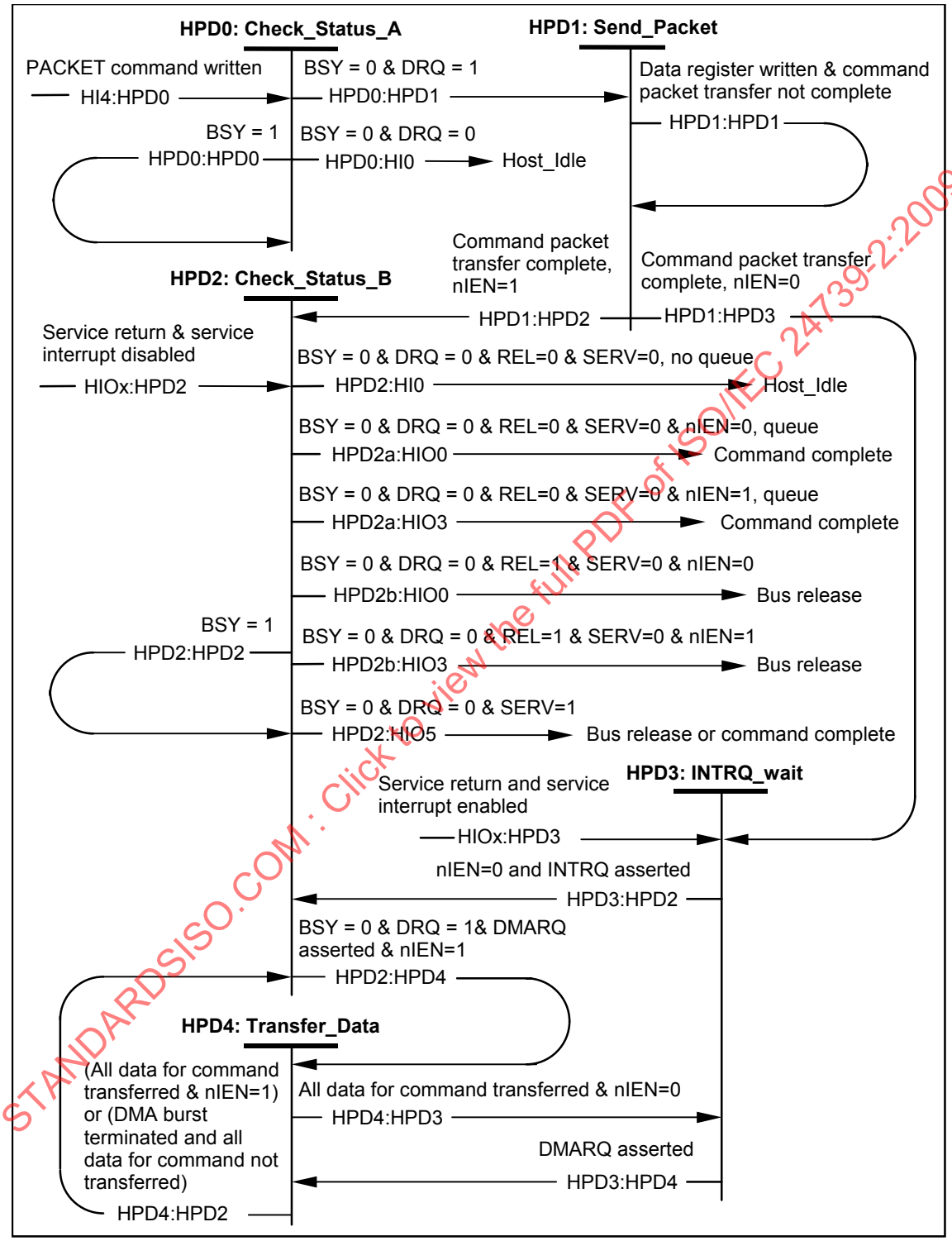


Figure 55 – Host PACKET DMA command state diagram

HPD0: Check_Status_A State: This state is entered when the host has written a PACKET command to the device.

When in this state, the host shall read the device Status register. When entering this state from the HI4 state, the host shall wait 400 ns before reading the Status register.

Transition HPD0:HPD0: When BSY is set to one, the host shall make a transition to the HPD0: Check_Status_A state.

Transition HPD0:HPD1: When BSY is cleared to zero and DRQ is set to one, then the host shall make a transition to the HPD1: Send_Packet state.

Transition HPD0:HI0: When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero and SERV is cleared to zero, then the command is completed and the host shall make a transition to the HI0: Host_Idle state (see Figure 41). If an error is reported, the host shall perform appropriate error recovery.

HPD1: Send_Packet State: This state is entered when BSY is cleared to zero, DRQ is set to one.

When in this state, the host shall write a byte of the command packet to the Data register.

Transition HPD1:HPD1: When the Data register has been written and the writing of the command packet is not completed, the host shall make a transition to the HPD1: Send_Packet state.

Transition HPD1:HPD2: When the Data register has been written, the writing of the command packet is completed and nIEN is set to one, the host shall make a transition to the HPD2: Check_Status_B state.

Transition HPD1:HPD3: When the Data register has been written, the writing of the command packet is completed and nIEN is cleared to zero, the host shall make a transition to the HPD3: INTRQ wait state.

HPD2: Check_Status_B State: This state is entered when the host has written the command packet to the device, when INTRQ has been asserted, when a DRQ data block has been transferred or from a service return when the service interrupt is disabled.

When in this state, the host shall read the device Status register. When entering this state from the HPD1 or HPD4 state, the host shall wait one PIO transfer cycle time before reading the Status register. The wait may be accomplished by reading the Alternate Status register and ignoring the result.

Transition HPD2:HPD2: When BSY is set to one and DRQ is cleared to zero, the host shall make a transition to the HPD2: Check_Status_B state.

Transition HPD2:HPD4: When BSY is cleared to zero, DRQ is set to one and DMARQ is asserted and nIEN=1, then the host shall make a transition to the HPD4: Transfer_Data state. The host shall have set up the DMA engine before this transition.

Transition HPD2:HI0: When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero and the device queue is empty, then the command is completed and the host shall make a transition to the HI0: Host_Idle state (see Figure 41). If an error is reported, the host shall perform appropriate error recovery.

Transition HPD2a:HIO0: When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, nIEN is cleared to zero and the device has a queue of released commands, then the command is completed and the host shall make a transition to the HIO0: Command completed state (see Figure 42). If an error is reported, the host shall perform appropriate error recovery.

Transition HPD2a:HIO3: When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, nIEN is set to one and the device has a queue of released

commands, then the command is completed and the host shall make a transition to the HIO3: Command completed state (see Figure 42). If an error is reported, the host shall perform appropriate error recovery.

Transition HPD2b:HIO0: When BSY is cleared to zero, DRQ is cleared to zero, REL is set to one, SERV is cleared to zero and nIEN is cleared to zero, then the host shall make a transition to the HIO0: INTRQ_wait_A state (see Figure 42). The bus has been released.

Transition HPD2b:HIO3: When BSY is cleared to zero, DRQ is cleared to zero, REL is set to one, SERV is cleared to zero and nIEN is set to one, then the host shall make a transition to the HIO3: Check_status_A state (see Figure 42). The bus has been released.

Transition HPD2:HIO5: When BSY is cleared to zero, DRQ is cleared to zero and SERV is set to one, then the host shall make a transition to the HIO5: Write_SERVICE state (see Figure 42). The command is completed or the bus has been released and another queued command is ready for service. If an error is reported, the host shall perform appropriate error recovery.

HPD3: INTRQ_Wait State: This state is entered when the command packet has been transmitted, when a service return is issued and the service interrupt is enabled or when the command has completed and nIEN is cleared to zero.

When in this state, the host shall wait for INTRQ to be asserted if nIEN=0 or DMARQ if nIEN=1.

Transition HPD3:HPD2: When INTRQ is asserted and nIEN=0, the host shall make a transition to the HPD2: Check_Status_B state.

Transition HPD3:HPD4: When DMARQ is asserted, the host shall make a transition to the HPD4: Transfer_Data state.

HPD4: Transfer_Data State: This state is entered when BSY is cleared to zero, DRQ is set to one and DMARQ is asserted.

When in this state, the host shall read or write the device Data port to transfer data. If the bus has been released, the host shall read the Sector Count register to determine the Tag for the queued command to be executed.

Transition HPD4:HPD2: The host shall make a transition to the HPD2: Check_Status_B state when (1) the host has transferred all data for the command and nIEN is set to one, or (2) the DMA burst has been terminated and all data for the command has not been transferred.

Transition HPD4:HPD3: When all data for the request has been transferred and nIEN is cleared to zero, then the host shall make a transition to the HPD3: INTRQ_wait state.

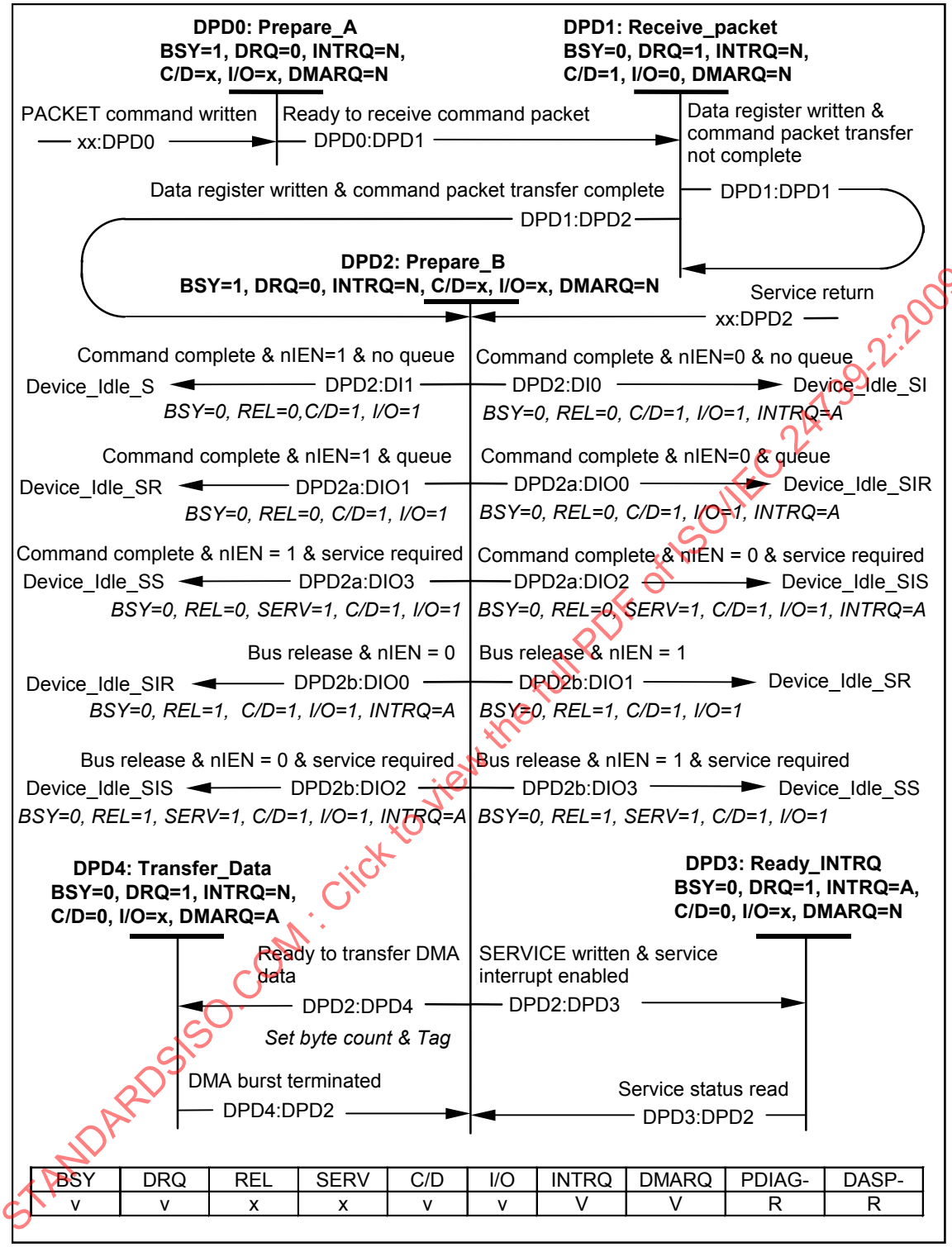


Figure 56 – Device PACKET DMA command state diagram

DPD0: Prepare_A State: This state is entered when the device has a PACKET written to the Command register.

When in this state, device shall set BSY to one, clear DRQ to zero and negate INTRQ within 400 ns of the receipt of the command and shall prepare to receive a command packet. If the command is a queued command, the device shall verify that the Tag is valid.

Transition DPD0:DPD1: When the device is ready to receive the command packet for a command, the device shall make a transition to the DPD1: Receive_Packet state.

DPD1: Receive_Packet State: This state is entered when the device is ready to receive the command packet.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is negated, C/D is set to one, I/O is cleared to zero and REL is cleared to zero. When in this state, the device Data register is written.

Transition DPD1:DPD1: If the Data register is written and the entire command packet has not been received, then the device shall make a transition to the DPD1: Receive_Packet state.

Transition DPD1:DPD2: When the Data register is written and the entire command packet has been received, then the device shall make a transition to the DPD2: Prepare_B state.

DPD2: Prepare_B State: This state is entered when the command packet has been received or from a Service return.

When in this state, device shall set BSY to one, clear DRQ to zero and negate INTRQ. The device shall check for errors, determine if the data transfer is complete, and if not, prepare to transfer the DMA data.

If the command is overlapped and the release interrupt is enabled, the device shall bus release as soon as the command packet has been received.

Transition DPD2:DPD4: When the device is ready to transfer DMA data for a command and nIEN is set to one, then the device shall set the command Tag and byte count, set the Interrupt Pending and make a transition to the DPD4: Transfer_Data state.

Transition DPD2:DPD3: When the service interrupt is enabled and the device has SERVICE written to the Command register, then the device shall set the command Tag and byte count and make a transition to the DPD3: Ready_INTRQ state.

Transition DPD2:DI0: When the command has completed or an error occurs that causes the command to abort, the device has no other command released and nIEN is cleared to zero, then the device shall set the Interrupt Pending, set appropriate error bits, set C/D and I/O to one, clear BSY to zero and make a transition to the DI0: Device_Idle_SI state (see Figure 43).

Transition DPD2:DI1: When the command has completed or an error occurs that causes the command to abort, the device has no other command released and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, clear BSY to zero and make a transition to the DI1: Device_Idle_S state (see Figure 43).

Transition DPD2a:DIO0: When the command has completed or an error occurs that causes the command to abort, the device has another command released but not ready for service and nIEN is cleared to zero, then the device shall set the Interrupt Pending, set appropriate error bits, set C/D and I/O to one, clear BSY to zero and make a transition to the DIO0: Device_Idle_SIR state (see Figure 44).

Transition DPD2a:DIO1: When the command has completed or an error occurs that causes the command to abort, the device has another command released but not ready for service and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, clear BSY to zero and make a transition to the DIO1: Device_Idle_SR state (see Figure 44).

Transition DPD2a:DIO2: When the command has completed or an error occurs that causes the command to abort, the device has another command ready for service and nIEN is cleared to zero, then the device shall set the Interrupt Pending, set appropriate error bits, set C/D and I/O to one, set SERV to one, clear BSY to zero and make a transition to the DIO2: Device_Idle_SIS state (see Figure 44).

Transition DPD2a:DIO3: When the command has completed or an error occurs that causes the command to abort, the device has another command ready for service and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, set SERV to one, clear BSY to zero and make a transition to the DIO3: Device_Idle_SS state (see Figure 44).

Transition DPD2b:DIO0: When the command is released and nIEN is cleared to zero, then the device shall set the Interrupt Pending, set appropriate error bits, set C/D and I/O to one, set REL to one, clear BSY to zero and make a transition to the DIO0: Device_Idle_SIR state (see Figure 44).

Transition DPD2b:DIO1: When the command is released and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, set REL to one, clear BSY to zero and make a transition to the DIO1: Device_Idle_SR state (see Figure 44).

Transition DPD2b:DIO2: When the command is released, the device has another command ready for service and nIEN is cleared to zero, then the device shall set the Interrupt Pending, set appropriate error bits, set C/D and I/O to one, set REL to one, set SERV to one, clear BSY to zero and make a transition to the DIO2: Device_Idle_SIS state (see Figure 44).

Transition DPD2b:DIO3: When the command is released, the device has another command ready for service and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, set REL to one, set SERV to one, clear BSY to zero and make a transition to the DIO3: Device_Idle_SS state (see Figure 44).

DPD3: Ready_INTRQ State: This state is entered upon receipt of a SERVICE command when service interrupt is enabled.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is asserted, C/D is cleared to zero and I/O is set to one for PIO data-out or cleared to zero for PIO data-in.

Transition DPD3:DPD2: When the Status register is read to respond to a service interrupt, the device shall make a transition to the DPD2: Prepare_B state.

DPD4: Data_Transfer State: This state is entered when the device is ready to transfer DMA data.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is negated, C/D is cleared to zero, I/O is set to one for data-out or cleared to zero for data-in, DMARQ is asserted and data is transferred as described in Multiword DMA timing or Ultra DMA protocol.

Transition DPD4:DPD2: When the DMA burst is terminated, the device shall make a transition to the DPD2: Prepare_B state. All of the data for the command may not have been transferred.

11.10 READ/WRITE DMA QUEUED command protocol

This class includes:

- READ DMA QUEUED
- READ DMA QUEUED EXT
- WRITE DMA QUEUED
- WRITE DMA QUEUED EXT
- WRITE DMA QUEUED FUA EXT

Execution of this class of command includes the transfer of one or more blocks of data from the host to the device or from the device to the host using DMA transfer. All data for the command may be transferred without a bus release between the command receipt and the data transfer. This command may bus release before transferring data. The host shall initialize the

DMA channel prior to transferring data. When data transfer has begun, all data for the request shall be transferred without a bus release. Figure 57 and the text following the figure describe the host states. Figure 58 and the text following the figure describe the device states.

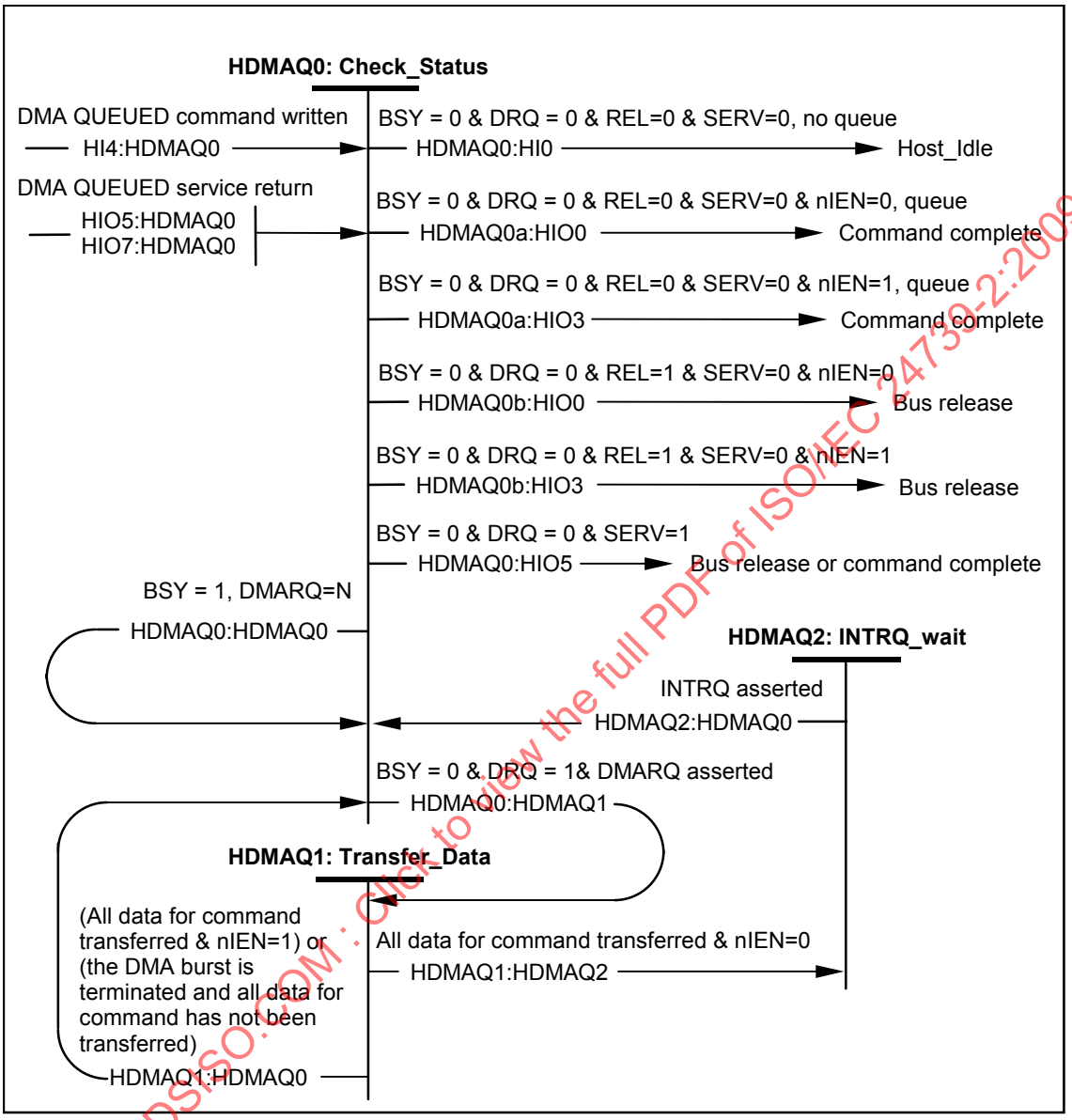


Figure 57 – Host DMA QUEUED state diagram

HDMAQ0: Check_Status State: This state is entered when the host has written a READ/WRITE DMA QUEUED command to the device, when all data for the command has been transferred and nIEN is set to one or when all data for the command has been transferred, nIEN is cleared to zero and INTRQ has been asserted. It is also entered when the SERVICE command has been written to continue execution of a bus released command.

When in this state, the host shall read the device Status register. When entering this state from the HI4, HIO5 or HIO7 state, the host shall wait 400 ns before reading the Status register. When entering this state from the HDMAQ1 state, the host shall wait one PIO transfer cycle time before reading the Status register. The wait may be accomplished by reading the Alternate Status register and ignoring the result. When entering this state from the DMA QUEUED service return, the host shall check the tag for the command to be serviced before making a transition to transfer data.

Transition HDMAQ0:HDMAQ0: When BSY is set to one and DMARQ is negated, the host shall make a transition to the HDMAQ0: Check_Status state.

Transition HDMAQ0:HDMAQ1: When BSY is cleared to zero, DRQ is set to one and DMARQ is asserted, then the host shall set up the DMA engine and then make a transition to the HDMAQ1: Transfer_Data state.

Transition HDMAQ0:HI0: When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero and the device queue is empty, then the command is completed and the host shall make a transition to the HI0: Host_Idle state (see Figure 41). If an error is reported, the host shall perform appropriate error recovery.

Transition HDMAQ0a:HIO0: When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, nIEN is cleared to zero and the device has a queue of released commands, then the command is completed and the host shall make a transition to the HIO0: Command completed state (see Figure 42). If an error is reported, the host shall perform appropriate error recovery.

Transition HDMAQ0a:HIO3: When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, nIEN is set to one and the device has a queue of released commands, then the command is completed and the host shall make a transition to the HIO3: Command completed state (see Figure 42). If an error is reported, the host shall perform appropriate error recovery.

Transition HDMAQ0b:HIO0: When BSY is cleared to zero, DRQ is cleared to zero, REL is set to one, SERV is cleared to zero and nIEN is cleared to zero, then the host shall make a transition to the HIO0: INTRQ_wait_A state (see Figure 42). The bus has been released.

Transition HDMAQ0b:HIO3: When BSY is cleared to zero, DRQ is cleared to zero, REL is set to one, SERV is cleared to zero and nIEN is set to one, then the host shall make a transition to the HIO3: Check_status_A state (see Figure 42). The bus has been released.

Transition HDMAQ0:HIO5: When BSY is cleared to zero, DRQ is cleared to zero and SERV is set to one, then the host shall make a transition to the HIO5: Write_SERVICE state (see Figure 42). The command is completed or the bus has been released and another queued command is ready for service. If an error is reported, the host shall perform appropriate error recovery.

HDMAQ1: Transfer_Data State: This state is entered when BSY is cleared to zero, DRQ is set to one and DMARQ is asserted.

When in this state, the host shall read or write the device Data port to transfer data. If the bus has been released, the host shall read the tag in the Sector Count register to determine the queued command to be executed and initialize the DMA channel.

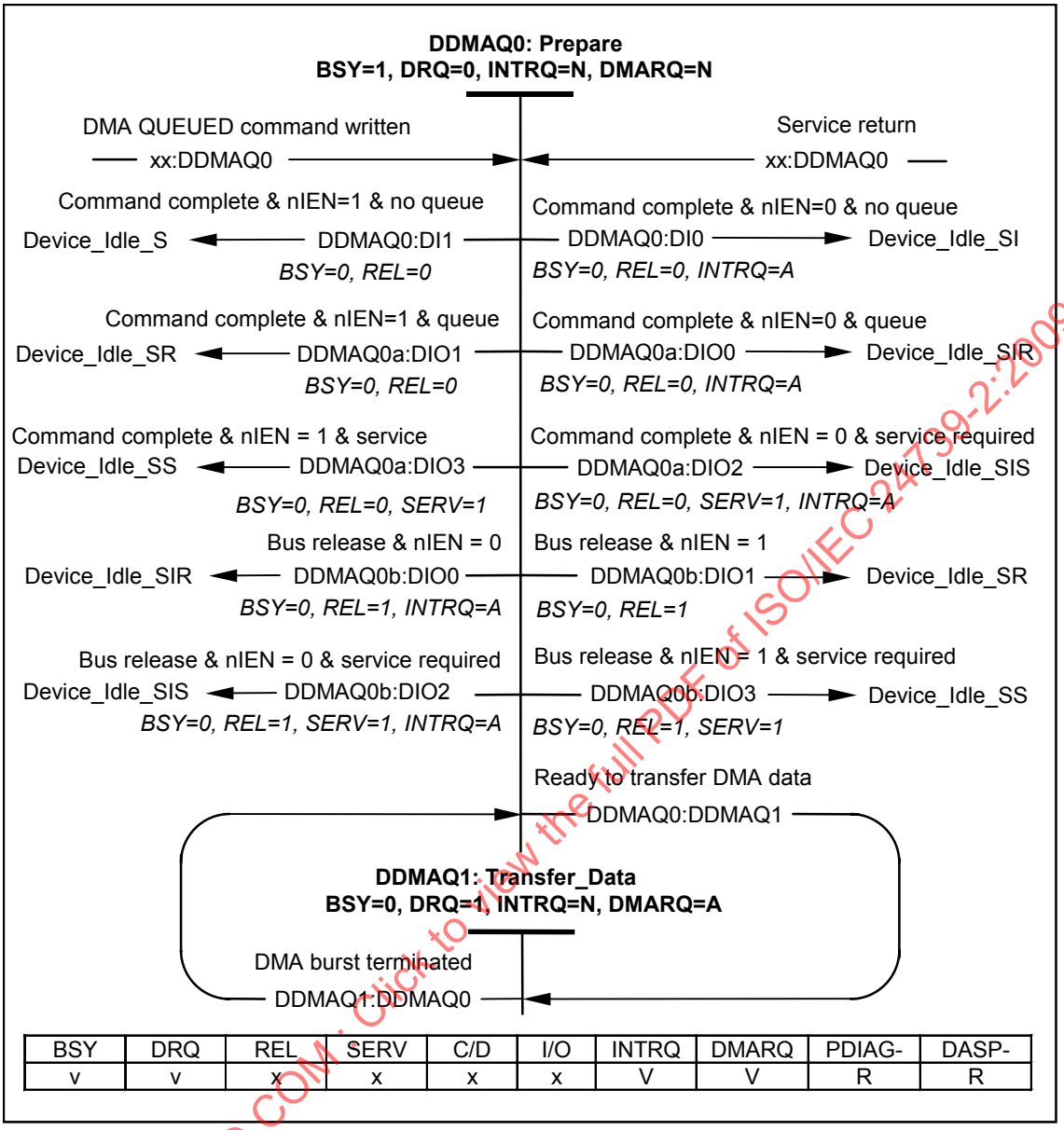
Transition HDMAQ1:HDMAQ0: The host shall make a transition to the HDMAQ0: Check_Status state when (1) all data for the request has been transferred and nIEN is set to one, or (2) the DMA burst is terminated and all data for the request has not been transferred.

Transition HDMAQ1:HDMAQ2: When all data for the request has been transferred and nIEN is cleared to zero, then the host shall make a transition to the HDMAQ2: INTRQ_wait state.

HDMAQ2: INTRQ_Wait State: This state is entered when the command has completed and nIEN is cleared to zero.

When in this state, the host shall wait for INTRQ to be asserted.

Transition HDMAQ2:HDMAQ0: When INTRQ is asserted, the host shall make a transition to the HDMAQ0: Check_Status state.



BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
v	v	x	x	x	x	V	V	R	R

Figure 58 – Device DMA QUEUED command state diagram

DDMAQ0: Prepare State: This state is entered when the device has a READ/WRITE DMA QUEUED or SERVICE command written to the Command register, when the data has been transferred or when the command has completed.

When in this state, device shall set BSY to one, clear DRQ to zero and negate INTRQ. If the command is a queued command, the device shall verify that the tag is valid. If commands are queued, the tag for the command to be serviced shall be placed into the Sector Count register.

Transition DDMAQ0:DDMAQ1: When the device is ready to transfer the data for a command, then the device shall make a transition to the DDMAQ1: Transfer_Data state.

Transition DDMAQ0:DI0: When the command has completed or an error occurs that causes the command to abort, the device has no other command released and nIEN is cleared to zero, then the device shall set the Interrupt Pending, set appropriate error bits, clear BSY to zero, assert INTRQ and make a transition to the DI0: Device_Idle_SI state (see Figure 43).

Transition DDMAQ0:DI1: When the command has completed or an error occurs that causes the command to abort, the device has no other command released and nIEN is set to one, then

the device shall set appropriate error bits, clear BSY to zero, assert INTRQ and make a transition to the DI1: Device_Idle_S state (see Figure 43).

Transition DDMAQ0a:DIO0: When the command has completed or an error occurs that causes the command to abort, the device has another command released but not ready for service and nIEN is cleared to zero, then the device shall set the Interrupt Pending, set appropriate error bits, clear BSY to zero, assert INTRQ and make a transition to the DIO0: Device_Idle_SIR state (see Figure 44).

Transition DDMAQ0a:DIO1: When the command has completed or an error occurs that causes the command to abort, the device has another command released but not ready for service and nIEN is set to one, then the device shall set appropriate error bits, clear BSY to zero and make a transition to the DIO1: Device_Idle_SR state (see Figure 44).

Transition DDMAQ0a:DIO2: When the command has completed or an error occurs that causes the command to abort, the device has another command ready for service and nIEN is cleared to zero, then the device shall set the Interrupt Pending, set appropriate error bits, set SERV to one, clear BSY to zero, assert INTRQ and make a transition to the DIO2: Device_Idle_SIS state (see Figure 44).

Transition DDMAQ0a:DIO3: When the command has completed or an error occurs that causes the command to abort, the device has another command ready for service and nIEN is set to one, then the device shall set appropriate error bits, set SERV to one, clear BSY to zero and make a transition to the DIO3: Device_Idle_SS state (see Figure 44).

Transition DDMAQ0b:DIO0: When the bus is released and nIEN is cleared to zero, then the device shall set the Interrupt Pending, set appropriate error bits, set REL to one, clear BSY to zero, assert INTRQ and make a transition to the DIO0: Device_Idle_SIR state (see Figure 44).

Transition DDMAQ0b:DIO1: When the bus is released and nIEN is set to one, then the device shall set appropriate error bits, set REL to one, clear BSY to zero and make a transition to the DIO1: Device_Idle_SR state (see Figure 44).

Transition DDMAQ0b:DIO2: When the bus is released, the device has another command ready for service and nIEN is cleared to zero, then the device shall set the Interrupt Pending, set appropriate error bits, set REL to one, set SERV to one, clear BSY to zero, assert INTRQ and make a transition to the DIO2: Device_Idle_SIS state (see Figure 44).

Transition DDMAQ0b:DIO3: When the bus is released, the device has another command ready for service and nIEN is set to one, then the device shall set appropriate error bits, set REL to one, set SERV to one, clear BSY to zero and make a transition to the DIO3: Device_Idle_SS state (see Figure 44).

DDMAQ1: Data_Transfer State: This state is entered when the device is ready to transfer DMA data.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is negated, DMARQ is asserted and data is transferred as described in Multiword DMA timing or Ultra DMA protocol.

Transition DDMAQ1:DDMAQ0: When the DMA burst has been terminated, then the device shall make a transition to the DDMAQ0: Prepare state. All of the data for the command may not have been transferred.

11.11 EXECUTE DEVICE DIAGNOSTIC command protocol

This class includes:

- EXECUTE DEVICE DIAGNOSTIC

If the host asserts RESET- before devices have completed executing their EXECUTE DEVICE DIAGNOSTIC protocol, then the devices shall start executing the power-on or hardware reset protocol from the beginning.

If the host sets SRST to one in the Device Control register before the devices have completed execution of their EXECUTE DEVICE DIAGNOSTIC protocol, then the devices shall start executing their software reset protocol from the beginning.

Figure 59 and the text following the figure describe the EXECUTE DEVICE DIAGNOSTIC protocol for the host. Figure 60 and the text following the figure describe the EXECUTE DEVICE DIAGNOSTIC protocol for Device 0. Figure 61 and the text following the figure describe the EXECUTE DEVICE DIAGNOSTIC protocol for Device 1.

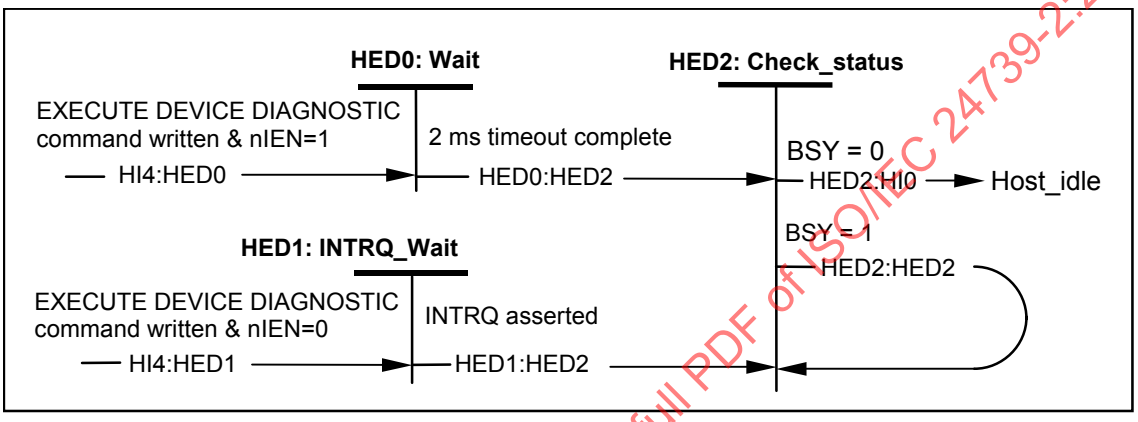


Figure 59 – Host EXECUTE DEVICE DIAGNOSTIC state diagram

HED0: Wait State: This state is entered when the host has written the EXECUTE DEVICE DIAGNOSTIC command to the devices and nIEN is set to one.

The host shall remain in this state for at least 2 ms.

Transition HED0:HED1: When at least 2 ms has elapsed since the command was written, the host shall make a transition to the HED1: Check_status state.

HED1: INTRQ_wait: This state is entered when the host has written the EXECUTE DEVICE DIAGNOSTIC command to the devices and nIEN is cleared to zero.

When in this state the host shall wait for INTRQ to be asserted.

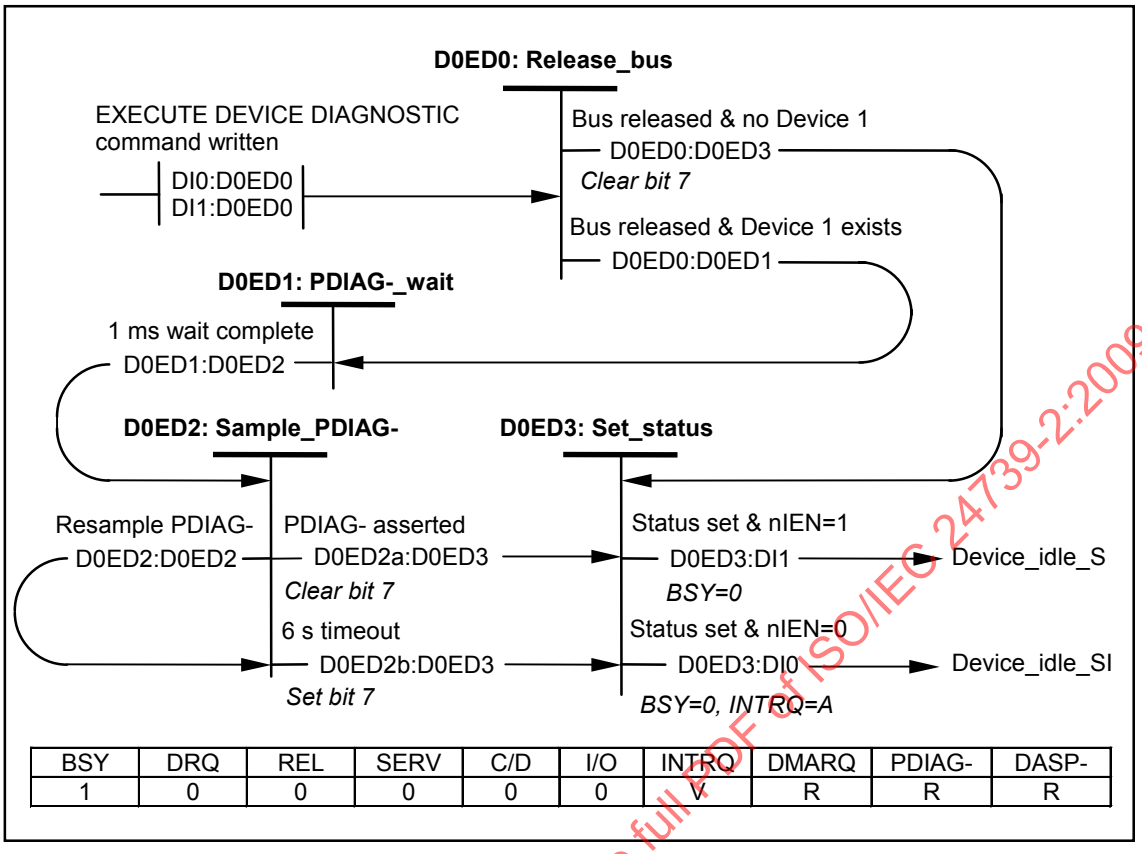
Transition HED1:HED2: When INTRQ is asserted, the host shall make a transition to the HED2: Check_status state.

HED2: Check_status State: This state is entered when at least 2 ms since the command was written or INTRQ has been asserted.

When in this state, the host shall read the Status or Alternate Status register.

Transition HED2:HED2: When BSY is set to one, the host shall make a transition to the HED1: Check_status state.

Transition HED2:HI0: When BSY is cleared to zero, the host shall check the results of the command (see ISO/IEC 24739-1:2008, Clause 5) and make a transition to the HI0: Host_idle state (see Figure 41).



BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
1	0	0	0	0	0	V	R	R	R

Figure 60 – Device 0 EXECUTE DEVICE DIAGNOSTIC state diagram

D0ED0: Release_bus State: This state is entered when the EXECUTE DEVICE DIAGNOSTIC command has been written.

When in this state, the device shall release PDIAG-, INTRQ, IORDY, DMARQ and DD(15:0) and shall set BSY to one within 400 ns after entering this state.

The device should begin performing the self-diagnostic testing.

Transition D0ED0:D0ED1: When the bus has been released, BSY set to one and the assertion of DASP- by Device 1 was detected during the most recent power-on or hardware reset, then the device shall make a transition to the D0ED1: PDIAG-_wait state.

Transition D0ED0:D0ED3: When the bus has been released, BSY set to one and the assertion of DASP- by Device 1 was not detected during the most recent power-on or hardware reset, then the device shall clear bit 7 in the Error register and make a transition to the D0ED3: Set_status state.

D0ED1: PDIAG-_wait State: This state is entered when the bus has been released, BSY set to one, and Device 1 exists.

The device shall remain in this state until least 1 ms has elapsed since the command was written and shall clear the DEV bit in the Device register to zero within 1 ms.

Transition D0ED1:D0ED2: When at least 1 ms has elapsed since the command was written, the device shall make a transition to the D0ED2: Sample_PDIAG- state.

D0ED2: Sample_PDIAG- State: This state is entered when at least 1 ms has elapsed since the command was written.

When in this state, the device shall sample the PDIAG- signal.

Transition D0ED2:D0ED3: When the sample indicates that PDIAG- is asserted, the device shall clear bit 7 in the Error register and make a transition to the D0ED3: Set_status state.

Transition D0ED2:D0ED2: When the sample indicates that PDIAG- is not asserted and less than 6 s have elapsed since the command was written, then the device shall make a transition to the D0ED2: Sample_PDIAG- state.

Transition D0ED2:D0ED3: When the sample indicates that DASP- is not asserted and 6 s have elapsed since the command was written, then the device shall set bit 7 in the Error register and make a transition to the D0ED3: Set_status state.

D0ED3: Set_status State: This state is entered when bit 7 in the Error register has been set or cleared.

When in this state, the device shall clear the DEV bit in the Device register to zero within 1 ms. The device shall complete the self-diagnostic testing begun in the Release bus state if not already completed.

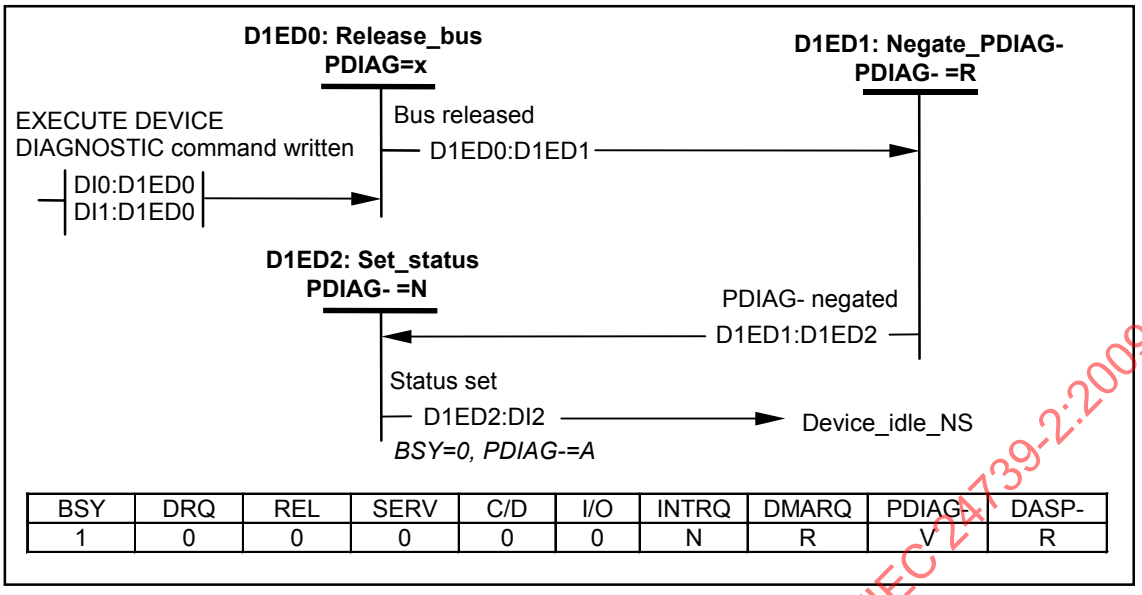
Results of the EXECUTE DEVICE DIAGNOSTICS self-diagnostic testing shall be placed in bits (6:0) of the Error register (see ISO/IEC 24739-1:2008, Clause 6). The device shall set the signature values (see ISO/IEC 24739-1:2008, Clause 5). The contents of the Features register is undefined.

If the device does not implement the PACKET command feature set, the device shall clear bits 3, 2 and 0 in the Status register to zero.

If the device implements the PACKET command feature set, the device shall clear bits 6, 5, 4, 3, 2 and 0 in the Status register to zero. The device shall return the operating modes to their specified initial conditions. MODE SELECT conditions shall be restored to their last saved values if saved values have been established. MODE SELECT conditions for which no values have been saved shall be returned to their default values.

Transition D0ED3:DI1: When hardware initialization and self-diagnostic testing is completed, the status has been set and nIEN is set to one, then the device shall clear BSY to zero and make a transition to the DI1: Device_idle_S state (see Figure 43).

Transition D0ED3:DI0: When hardware initialization and self-diagnostic testing is completed, the status has been set and nIEN is cleared to zero, then the device shall clear BSY to zero, assert INTRQ and make a transition to the DI0: Device_idle_SI state (see Figure 43).



BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	DASP-
1	0	0	0	0	0	N	R	V	R

Figure 61 – Device 1 EXECUTE DEVICE DIAGNOSTIC command state diagram

D1ED0: Release_bus State: This state is entered when the EXECUTE DEVICE DIAGNOSTIC command is written.

When in this state, the device shall release INTRQ, IORDY, DMARQ and DD(15:0) within 400 ns after entering this state. The device shall set BSY to one within 400 ns after entering this state.

The device should begin performing the self-diagnostic testing.

Transition D1ED0:D1ED1: When the bus has been released and BSY set to one, then the device shall make a transition to the D1ED1: Negate_PDIAG- state.

D1ED1: Negate_PDIAG- State: This state is entered when the bus has been released and BSY set to one.

When in this state, the device shall negate PDIAG- and clear the DEV bit in the Device register within less than 1 ms of the receipt of the EXECUTE DEVICE DIAGNOSTIC command.

Transition D1ED1:D1ED2: When PDIAG- has been negated, the device shall make a transition to the D1ED2: Set_status state.

D1ED2: Set_status State: This state is entered when the device has negated PDIAG-.

When in this state the device shall complete the hardware initialization and self-diagnostic testing begun in the Release bus state if not already completed. Results of the EXECUTE DEVICE DIAGNOSTICS shall be placed in the Error register (see ISO/IEC 24739-1:2008, Clause 6). If the device passed the self-diagnostics, the device shall assert PDIAG-.

The device shall set the signature values (see ISO/IEC 24739-1:2008, Clause 5). The effect on the Features register is undefined.

If the device does not implement the PACKET command feature set, the device shall clear bits 3, 2 and 0 in the Status register to zero.

If the device implements the PACKET command feature set, the device shall clear bits 6, 5, 4, 3, 2 and 0 in the Status register to zero. The device shall return the operating modes to their specified initial conditions. MODE SELECT conditions shall be restored to their last saved

values if saved values have been established. MODE SELECT conditions for which no values have been saved shall be returned to their default values.

All requirements for this state shall be completed within 5 s from the writing of the command.

Transition D1ED2:DI2: When hardware initialization and self-diagnostic testing is completed and the status has been set, then the device shall clear BSY to zero, assert PDIAG- if diagnostics were passed and make a transition to the DI2: Device_idle_NS state (see Figure 43).

11.12 DEVICE RESET command protocol

This class includes:

- DEVICE RESET

If the host asserts RESET- before the device has completed executing a DEVICE RESET command, then the device shall start executing the hardware reset protocol from the begining. If the host sets the SRST bit to one in the Device Control register before the device has completed executing a DEVICE RESET command, the device shall start executing the software reset protocol from the beginning.

The host should not issue a DEVICE RESET command while a DEVICE RESET command is in progress. If the host issues a DEVICE RESET command while a DEVICE RESET command is in progress, the results are indeterminate.

Figure 62 and the text following the figure describe the DEVICE RESET command protocol for the host. Figure 63 and the text following the figure describe the DEVICE RESET command protocol for the device.

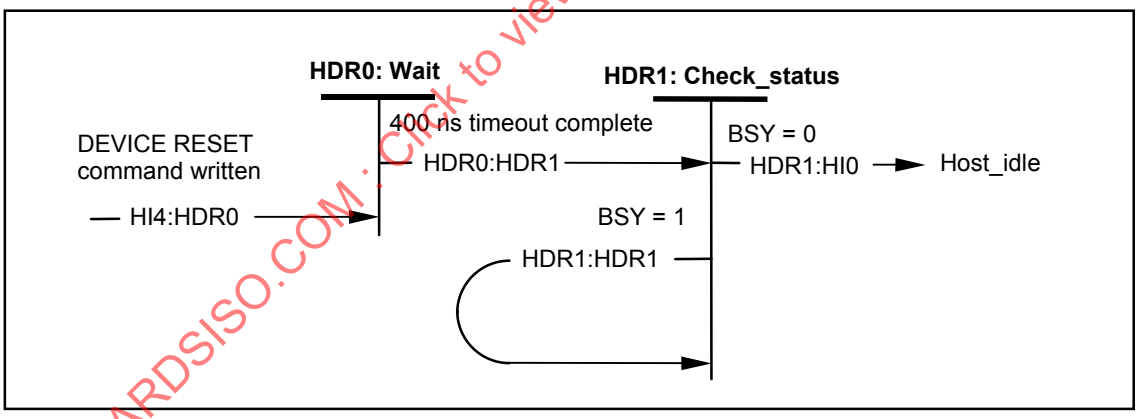


Figure 62 – Host DEVICE RESET command state diagram

HDR0: Wait State: This state is entered when the host has written the DEVICE RESET command to the device.

The host shall remain in this state for at least 400 ns.

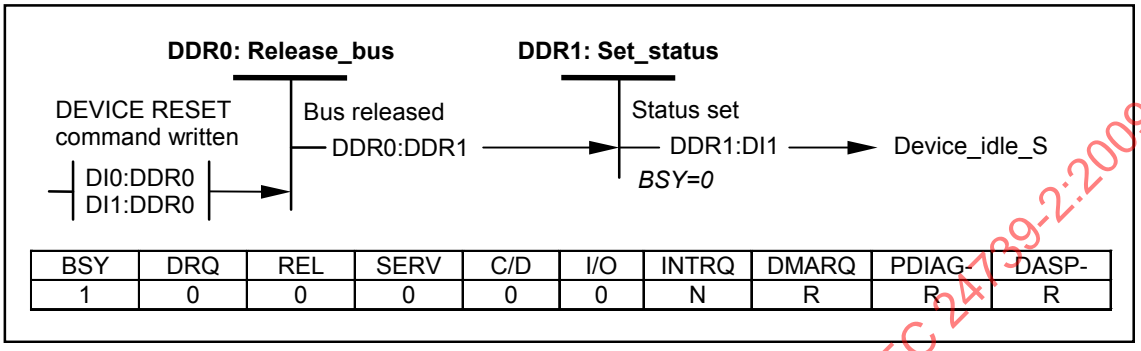
Transition HDR0:HDR1: When at least 400 ns has elapsed since the command was written, the host shall make a transition to the HDR1: Check_status state.

HDR1: Check_status State: This state is entered when at least 400 ns has elapsed since the command was written.

When in this state the host shall read the Status register.

Transition HDR1:HDR1: When BSY is set to one, the host shall make a transition to the HDR1: Check_status state.

Transition HDR1:HI0: When BSY is cleared to zero, the host shall make a transition to the HI0: Host_idle state (see Figure 41). If status indicates that an error has occurred, the host shall take appropriate action.



BSY	DRQ	REL	SERV	C/D	I/O	INTRQ	DMARQ	PDIAG-	-DASP-
1	0	0	0	0	0	N	R	R	R

Figure 63 – Device DEVICE RESET command state diagram

DDR0: Release_bus State: This state is entered when the DEVICE RESET command is written.

When in this state, the device shall release INTRQ, IORDY, DMARQ and DD(15:0) within 400 ns after entering this state. The device shall set BSY to one within 400 ns after entering this state.

Transition DDR0:DDR1: When the bus has been released and BSY set to one, the device shall make a transition to the DDR1: Set_status state.

DDR1: Set_status State: This state is entered when the device has released the bus and set BSY to one.

When in this state the device should stop execution of any uncompleted command. The device should end background activity (e.g., immediate commands, see MMC-2).

The device should not revert to the default condition. If the device reverts to the default condition, the device shall report an exception condition by setting CHK to one in the Status register. MODE SELECT conditions shall not be altered.

The device shall set the signature values (see ISO/IEC 24739-1:2008, Clause 5). The content of the Features register is undefined.

The device shall clear bit 7 in the ERROR register to zero. The device shall clear bits 6, 5, 4, 3, 2 and 0 in the Status register to zero.

Transition DDR1:DI1: When the status has been set, the device shall clear BSY to zero and make a transition to the DI1: Device_idle_S state (see Figure 43).

11.13 Ultra DMA data-in commands

11.13.1 Initiating an Ultra DMA data-in burst

The following steps shall occur in the order they are listed unless otherwise specified. Timing requirements are listed in 12.2.5 and shown in 12.2.5.2.

a) The host shall keep DMACK- in the negated state before an Ultra DMA burst is initiated.

b) The device shall assert DMARQ to initiate an Ultra DMA burst when DMACK- is negated. After assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE.

NOTE Steps c), d) and e) may occur in any order or at the same time.

c) The host shall assert STOP.

d) The host shall negate HDMARDY-.

e) The host shall negate CS0-, CS1-, DA2, DA1 and DA0. The host shall keep CS0-, CS1-, DA2, DA1 and DA0 negated until after negating DMACK- at the end of the burst.

NOTE For steps c), d) and e) shall have occurred at least t_{ACK} before the host asserts DMACK-.

f) The host shall keep DMACK- asserted until the end of an Ultra DMA burst.

g) The host shall release DD(15:0) within tAZ after asserting DMACK-.

h) The device may assert DSTROBE tZIORDY after the host has asserted DMACK-. Once the device has driven DSTROBE the device shall not release DSTROBE until after the host has negated DMACK- at the end of an Ultra DMA burst.

i) The host shall negate STOP and assert HDMARDY- within tENV after asserting DMACK-. After negating STOP and asserting HDMARDY-, the host shall not change the state of either signal until after receiving the first negation of DSTROBE from the device (i.e., after the first data word has been received).

j) The device shall drive DD(15:0) no sooner than t_{ZAD} has occurred and after the host has asserted DMACK-, negated STOP and asserted HDMARDY-.

k) The device shall drive the first word of the data transfer onto DD(15:0). This step may occur when the device first drives DD(15:0) in step (j).

l) To transfer the first word of data the device shall negate DSTROBE within tFS after the host has negated STOP and asserted HDMARDY-. The device shall negate DSTROBE no sooner than t_{DVS} has occurred and after driving the first word of data onto DD(15:0).

11.13.2 The data-in transfer

The following steps shall occur in the order they are listed unless otherwise specified. Timing requirements are listed in 12.2.5 and shown in 12.2.5.2.

a) The device shall drive a data word onto DD(15:0).

b) The device shall generate a DSTROBE edge to latch the new word no sooner than t_{DVS} has occurred and after changing the state of DD(15:0). The device shall generate a DSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA mode. The device shall not generate two rising or two falling DSTROBE edges more frequently than t_{2cyc} for the selected Ultra DMA mode.

c) The device shall not change the state of DD(15:0) until at least t_{DVH} after generating a DSTROBE edge to latch the data.

d) The device shall repeat steps a), b) and c) until the Ultra DMA burst is paused or terminated by the device or host.

11.13.3 Pausing an Ultra DMA data-in burst

11.13.3.1 General

The following steps shall occur in the order they are listed unless otherwise specified. Timing requirements are listed in 12.2.5 and shown in 12.2.5.3.

11.13.3.2 Device pausing an Ultra DMA data-in burst

The following steps for device pausing apply.

a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
b) The device shall pause an Ultra DMA burst by not generating additional DSTROBE edges. If the host is ready to terminate the Ultra DMA burst, see 11.13.3.4.2.
c) The device shall resume an Ultra DMA burst by generating a DSTROBE edge.

11.13.3.3 Host pausing an Ultra DMA data-in burst

The following steps for host pausing apply.

a) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
b) The host shall pause an Ultra DMA burst by negating HDMARDY-.
c) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating HDMARDY-.
d) When operating in Ultra DMA modes 2, 1 or 0 the host shall be prepared to receive zero, one or two additional data words after negating HDMARDY-. While operating in Ultra DMA modes 6, 5, 4 or 3 the host shall be prepared to receive zero, one, two or three additional data words after negating HDMARDY-. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.
e) The host shall resume an Ultra DMA burst by asserting HDMARDY-.

11.13.3.4 Terminating an Ultra DMA data-in burst

11.13.3.4.1 Device terminating an Ultra DMA data-in burst

Burst termination is completed when the termination protocol has been executed and DMACK- negated.

The device shall terminate an Ultra DMA burst before command completion.

The following steps shall occur in the order they are listed unless otherwise specified. Timing requirements are listed in 12.2.5 and shown in 12.2.5.5.

a) The device shall initiate termination of an Ultra DMA burst by not generating additional DSTROBE edges.
b) The device shall negate DMARQ no sooner than t_{SS} has occurred and after generating the last DSTROBE edge. The device shall not assert DMARQ again until after DMACK- has been negated.
c) The device shall release DD(15:0) no later than t_{AZ} after negating DMARQ.
d) The host shall assert STOP within t_{LI} after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
e) The host shall negate HDMARDY- within t_{LI} after the device has negated DMARQ. The host shall continue to negate HDMARDY- until the Ultra DMA burst is terminated. Steps d) and e) may occur simultaneously.
f) The host shall drive DD(15:0) no sooner than t_{ZAH} has occurred and after the device has negated DMARQ. For this step, the host may first drive DD(15:0) with the result of the host CRC calculation (see 11.15).
g) If DSTROBE is negated, the device shall assert DSTROBE within t_{LI} after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.
h) If the host has not placed the result of the host CRC calculation on DD(15:0) since first driving DD(15:0) during f), the host shall place the result of the host CRC calculation on DD(15:0) (see 11.15).
i) The host shall negate DMACK- no sooner than t_{MLI} has occurred and after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated

HDMARDY- and no sooner than t_{DVS} has occurred and after the host places the result of the host CRC calculation on DD(15:0).

j) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.

k) The device shall compare the CRC data received from the host with the results of the device CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command the device shall report the first error that occurred (see 11.15).

l) The device shall release DSTROBE within t_{IORDYZ} after the host negates DMACK-.

m) The host shall not negate STOP nor assert HDMARDY- until at least t_{ACK} after negating DMACK-.

n) The host shall not assert DIOR-, CS0-, CS1-, DA2, DA1 or DA0 until at least t_{ACK} after negating DMACK.

11.13.3.4.2 Host terminating an Ultra DMA data-in burst

The following steps shall occur in the order they are listed unless otherwise specified. Timing requirements are listed in 12.2.5 and shown in 12.2.5.6.

a) The host shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.

b) The host shall initiate Ultra DMA burst termination by negating HDMARDY-. The host shall continue to negate HDMARDY- until the Ultra DMA burst is terminated.

c) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating HDMARDY-.

d) When operating in Ultra DMA modes 2, 1 or 0 the host shall be prepared to receive zero, one or two additional data words after negating HDMARDY-. While operating in Ultra DMA modes 6, 5, 4 or 3 the host shall be prepared to receive zero, one, two or three additional data words after negating HDMARDY-. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.

e) The host shall assert STOP no sooner than t_{RP} has occurred and after negating HDMARDY-. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

f) The device shall negate DMARQ within t_{LI} after the host has asserted STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.

g) If DSTROBE is negated, the device shall assert DSTROBE within t_{LI} after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.

h) The device shall release DD(15:0) no later than t_{AZ} after negating DMARQ.

i) The host shall drive DD(15:0) no sooner than t_{ZAH} has occurred and after the device has negated DMARQ. For this step, the host may first drive DD(15:0) with the result of the host CRC calculation (see 11.15).

j) If the host has not placed the result of the host CRC calculation on DD(15:0) since first driving DD(15:0) during (i), the host shall place the result of the host CRC calculation on DD(15:0) (see 11.15).

k) The host shall negate DMACK- no sooner than t_{MLI} has occurred and after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated HDMARDY- and no sooner than t_{DVS} has occurred and after the host places the result of the host CRC calculation on DD(15:0).

l) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.

m) The device shall compare the CRC data received from the host with the results of the device CRC calculation. If a miscompare error occurs during one or more Ultra DMA burst for any one command, at the end of the command, the device shall report the first error that occurred (see 11.15).

n) The device shall release DSTROBE within t_{IORDYZ} after the host negates DMACK-.

o) The host shall neither negate STOP nor assert HDMARDY- until at least t_{ACK} after the host has negated DMACK-.

p) The host shall not assert DIOR-, CS0-, CS1-, DA2, DA1 or DA0 until at least t_{ACK} after negating DMACK.

11.14 Ultra DMA data-out commands

11.14.1 Initiating an Ultra DMA data-out burst

The following steps shall occur in the order they are listed unless otherwise specified. Timing requirements are listed in 12.2.5 and shown in 12.2.5.7.

a) The host shall keep DMACK- in the negated state before an Ultra DMA burst is initiated.
b) The device shall assert DMARQ to initiate an Ultra DMA burst when DMACK- is negated.

NOTE Steps c), d) and e) may occur in any order or at the same time.

c) The host shall assert STOP.
d) The host shall assert HSTROBE.
e) The host shall negate CS0-, CS1-, DA2, DA1 and DA0. The host shall keep CS0-, CS1-, DA2, DA1 and DA0 negated until after negating DMACK- at the end of the burst.

NOTE For steps c), d) and e) shall have occurred at least t_{ACK} before the host asserts DMACK-.

f) The host shall keep DMACK- asserted until the end of an Ultra DMA burst.
g) The device may negate DDMARDY- t_{ZIORDY} after the host has asserted DMACK-. Once the device has negated DDMARDY-, the device shall not release DDMARDY- until after the host has negated DMACK- at the end of an Ultra DMA burst.
h) The host shall negate STOP within t_{ENV} after asserting DMACK-. The host shall not assert STOP until after the first negation of HSTROBE.
i) The device shall assert DDMARDY- within t_{LI} after the host has negated STOP. After asserting DMARQ and DDMARDY- the device shall not negate either signal until after the first negation of HSTROBE by the host.
j) The host shall drive the first word of the data transfer onto DD(15:0). This step may occur any time during Ultra DMA burst initiation.
k) To transfer the first word of data: the host shall negate HSTROBE no sooner than t_{UI} has occurred and after the device has asserted DDMARDY-. The host shall negate HSTROBE no sooner than t_{DVS} after the driving the first word of data onto DD(15:0).

11.14.2 Data-out transfer

The following steps shall occur in the order they are listed unless otherwise specified. Timing requirements are listed in 12.2.5 and shown in 12.2.5.8.

a) The host shall drive a data word onto DD(15:0).
b) The host shall generate an HSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of DD(15:0). The host shall generate an HSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA mode. The host shall not generate two rising or falling HSTROBE edges more frequently than t_{2CYC} for the selected Ultra DMA mode.
c) The host shall not change the state of DD(15:0) until at least t_{DVH} after generating an HSTROBE edge to latch the data.
d) The host shall repeat steps a), b) and c) until the Ultra DMA burst is paused or terminated by the device or host.

11.14.3 Pausing an Ultra DMA data-out burst

11.14.3.1 General

The following steps shall occur in the order they are listed unless otherwise specified. Timing requirements are listed in 12.2.5 and shown in 12.2.5.9.

11.14.3.2 Host pausing an Ultra DMA data-out burst

The following steps for host pausing apply.

a) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
b) The host shall pause an Ultra DMA burst by not generating an HSTROBE edge. If the host is ready to terminate the Ultra DMA burst (see 11.14.4.1).
c) The host shall resume an Ultra DMA burst by generating an HSTROBE edge.

11.14.3.3 Device pausing an Ultra DMA data-out burst

The following steps for device pausing apply.

a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
b) The device shall pause an Ultra DMA burst by negating DDMARDY-.
c) The host shall stop generating HSTROBE edges within t_{RFS} of the device negating DDMARDY-.
d) When operating in Ultra DMA modes 2, 1 or 0 the device shall be prepared to receive zero, one or two additional data words after negating DDMARDY-. While operating in Ultra DMA modes 6, 5, 4 or 3 the device shall be prepared to receive zero, one, two or three additional data words after negating DDMARDY-. The additional data words are a result of cable round trip delay and t_{RFS} timing for the host.
e) The device shall resume an Ultra DMA burst by asserting DDMARDY-.

11.14.4 Terminating an Ultra DMA data-out burst

11.14.4.1 Host terminating an Ultra DMA data-out burst

The following steps shall occur in the order they are listed unless otherwise specified. Timing requirements are listed in 12.2.5 and shown in 12.2.5.10.

a) The host shall initiate termination of an Ultra DMA burst by not generating additional HSTROBE edges.
b) The host shall assert STOP no sooner than t_{SS} has occurred and after the last generated an HSTROBE edge. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
c) The device shall negate DMARQ within t_{LI} after the host asserts STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
d) The device shall negate DDMARDY- within t_{LI} after the host has negated STOP. The device shall not assert DDMARDY- again until after the Ultra DMA burst termination is complete.
e) If HSTROBE is negated, the host shall assert HSTROBE within t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.
f) The host shall place the result of the host CRC calculation on DD(15:0) (see 11.15).
g) The host shall negate DMACK- no sooner than t_{MLI} has occurred and after the host has asserted HSTROBE and STOP and the device has negated DMARQ and DDMARDY- and no sooner than t_{DVS} has occurred and after placing the result of the host CRC calculation on DD(15:0).
h) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.
i) The device shall compare the CRC data received from the host with the results of the device CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred (see 11.15).
j) The device shall release DDMARDY- within t_{IORDYZ} after the host has negated DMACK-.
k) The host shall neither negate STOP nor negate HSTROBE until at least t_{ACK} after negating DMACK-.
l) The host shall not assert DIOW-, CS0-, CS1-, DA2, DA1 or DA0 until at least t_{ACK} after negating DMACK.

11.14.4.2 Device terminating an Ultra DMA data-out burst

Burst termination is completed when the termination protocol has been executed and DMACK- negated.

The device shall terminate an Ultra DMA burst before command completion.

The following steps shall occur in the order they are listed unless otherwise specified. Timing requirements are listed in 12.2.5 and shown in 12.2.5.11.

a) The device shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.
b) The device shall initiate Ultra DMA burst termination by negating DDMARDY-.
c) The host shall stop generating an HSTROBE edges within t_{RFS} of the device negating DDMARDY-.
d) When operating in Ultra DMA modes 2, 1 or 0 the device shall be prepared to receive zero, one or two additional data words after negating DDMARDY-. While operating in Ultra DMA modes 6, 5, 4 or 3 the device shall be prepared to receive zero, one, two or three additional data words after negating DDMARDY-. The additional data words are a result of cable round trip delay and t_{RFS} timing for the host.
e) The device shall negate DMARQ no sooner than t_{RP} after negating DDMARDY-. The device shall not assert DMARQ again until after DMACK- is negated.
f) The host shall assert STOP within t_{LI} after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
g) If HSTROBE is negated, the host shall assert HSTROBE within t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.
h) The host shall place the result of the host CRC calculation on DD(15:0) (see 11.15).
i) The host shall negate DMACK- no sooner than t_{MLI} has occurred and after the host has asserted HSTROBE and STOP and the device has negated DMARQ and DDMARDY- and no sooner than t_{DVS} has occurred and after placing the result of the host CRC calculation on DD(15:0).
j) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.
k) The device shall compare the CRC data received from the host with the results of the device CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred (see 11.15).
l) The device shall release DDMARDY- within t_{IORDYZ} after the host has negated DMACK-.
m) The host shall neither negate STOP nor HSTROBE until at least t_{ACK} after negating DMACK-.
n) The host shall not assert DIOW-, CS0-, CS1-, DA2, DA1 or DA0 until at least t_{ACK} has occurred and after negating DMACK.

11.15 Ultra DMA CRC rules

The following is a list of rules for calculating CRC, determining if a CRC error has occurred during an Ultra DMA burst and reporting any error that occurs at the end of a command.

1) Both the host and the device shall have a 16-bit CRC calculation function.
2) Both the host and the device shall calculate a CRC value for each Ultra DMA burst.
3) The CRC function in the host and the device shall be initialized with a seed of 4ABAh at the beginning of an Ultra DMA burst before any data is transferred.
4) For each STROBE transition used for data transfer, both the host and the device shall calculate a new CRC value by applying the CRC polynomial to the current value of their individual CRC functions and the word being transferred. CRC is not calculated for the return of STROBE to the asserted state after the Ultra DMA burst termination request has been acknowledged.
5) At the end of any Ultra DMA burst the host shall send the results of the host CRC calculation function to the device on DD(15:0) with the negation of DMACK-.
6) The device shall then compare the CRC data from the host with the calculated value in its own CRC calculation function. If the two values do not match, the device shall save the error. A subsequent Ultra DMA burst for the same command that does not have a CRC error shall not clear an error saved from a previous Ultra DMA burst in the same command. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, the device shall report the first error that occurred. If the device detects that a CRC error has occurred before data transfer for the command is complete, the device may complete the transfer and report the error or abort the command and report the error.
7) For READ DMA, WRITE DMA, READ DMA QUEUED or WRITE DMA QUEUED commands: When a CRC error is detected, the error shall be reported by setting both ICRC and ABRT

(bit 7 and bit 2 in the Error register) to one. ICRC is defined as the interface CRC error bit. The host shall respond to this error by re-issuing the command.

8) For a REQUEST SENSE PACKET command (see SPC, INCITS 301:1997, for the definition of the REQUEST SENSE command): When a CRC error is detected during transmission of sense data the device shall complete the command and set CHK to one. The device shall report a Sense key of 0Bh (ABORTED COMMAND). The device shall preserve the original sense data that was being returned when the CRC error occurred. The device shall not report any additional sense data specific to the CRC error. The host device driver may retry the REQUEST SENSE command or may consider this an unrecoverable error and retry the command that caused the Check Condition.
9) For any PACKET command except a REQUEST SENSE command: If a CRC error is detected, the device shall complete the command with CHK set to one. The device shall report a Sense key of 04h (HARDWARE ERROR). The sense data supplied via a subsequent REQUEST SENSE command shall report an ASC/ASCQ value of 08h/03h (LOGICAL UNIT COMMUNICATION CRC ERROR). Host drivers should retry the command that resulted in a HARDWARE ERROR.
10) A host may send extra data words on the last Ulotra DMA burst of a data out command. If a device determines that all data has been transferred for a command, the device shall terminate the burst. A devide may have already received more data words that were required for the command. These extra words are used by both the host and the devive to calculate the CRC, but, on an Ultr DMA data-out burst, the extra words shall be discarded by the device.
11) The CRC generator polynomial is: G(X) = X16 + X12 + X5 + 1. Table 49 describes the equations for 16-bit parallel generation of the resulting polynomial (based on a word boundary).

NOTE 1 Since no bit clock is available, the recommended approach for calculating CRC is to use a word clock derived from the bus strobe. The combinational logic is then equivalent to shifting sixteen bits serially through the generator polynomial where DD0 is shifted in first and DD15 is shifted in last.

NOTE 2 If excessive CRC errors are encountered while operating in an Ultra mode, the host should select a slower Ultra mode. CAUTION: CRC errors are detected and reported only while operating in an Ultra mode.

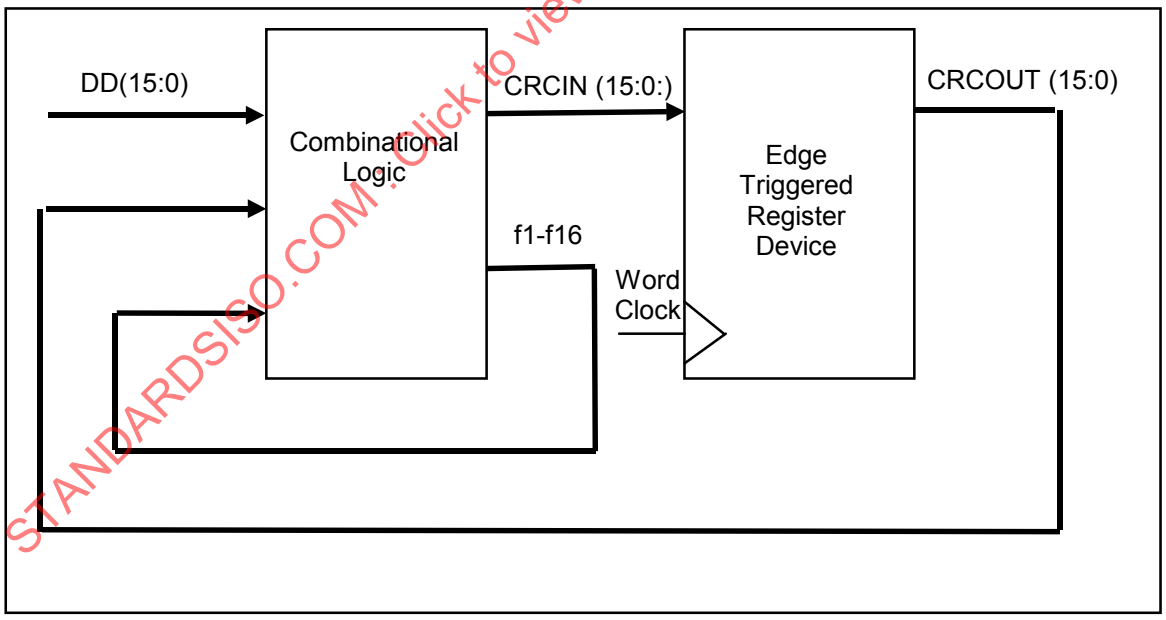


Figure 64 – Example parallel CRC generator

Table 49 – Equations for parallel generation of a CRC polynomial

CRCIN0 = f16	CRCIN8 = f8 XOR f13
CRCIN1 = f15	CRCIN9 = f7 XOR f12
CRCIN2 = f14	CRCIN10 = f6 XOR f11
CRCIN3 = f13	CRCIN11 = f5 XOR f10
CRCIN4 = f12	CRCIN12 = f4 XOR f9 XOR f16
CRCIN5 = f11 XOR f16	CRCIN13 = f3 XOR f8 XOR f15
CRCIN6 = f10 XOR f15	CRCIN14 = f2 XOR f7 XOR f14
CRCIN7 = f9 XOR f14	CRCIN15 = f1 XOR f6 XOR f13
f1 = DD0 XOR CRCOUT15	f9 = DD8 XOR CRCOUT7 XOR f5
f2 = DD1 XOR CRCOUT14	f10 = DD9 XOR CRCOUT6 XOR f6
f3 = DD2 XOR CRCOUT13	f11 = DD10 XOR CRCOUT5 XOR f7
f4 = DD3 XOR CRCOUT12	f12 = DD11 XOR CRCOUT4 XOR f1 XOR f8
f5 = DD4 XOR CRCOUT11 XOR f1	f13 = DD12 XOR CRCOUT3 XOR f2 XOR f9
f6 = DD5 XOR CRCOUT10 XOR f2	f14 = DD13 XOR CRCOUT2 XOR f3 XOR f10
f7 = DD6 XOR CRCOUT9 XOR f3	f15 = DD14 XOR CRCOUT1 XOR f4 XOR f11
f8 = DD7 XOR CRCOUT8 XOR f4	f16 = DD15 XOR CRCOUT0 XOR f5 XOR f12
Key	
f = feedback	
DD = Data to or from the bus	
CRCOUT = 16-bit edge triggered result (current CRC)	
CRCOUT(15:0) are sent on matching order bits of DD(15:0)	
CRCIN = Output of combinatorial logic (next CRC)	

12 Parallel interface timing

12.1 Deskewing

For PIO and Multiword DMA modes all timing values shall be measured at the connector of the selected device. The host shall account for cable skew.

For Ultra DMA modes unless otherwise specified, timing parameters shall be measured at the connector of the host or device to which the parameter applies.

12.2 Transfer timing

12.2.1 General

The minimum cycle time supported by the device in PIO mode 3, 4 and Multiword DMA mode 1, 2, respectively, shall always be greater than or equal to the minimum cycle time defined by the associated mode e.g., a device supporting PIO mode 4 timing shall not report a value less than 120 ns, the minimum cycle time defined for PIO mode 4 timings.

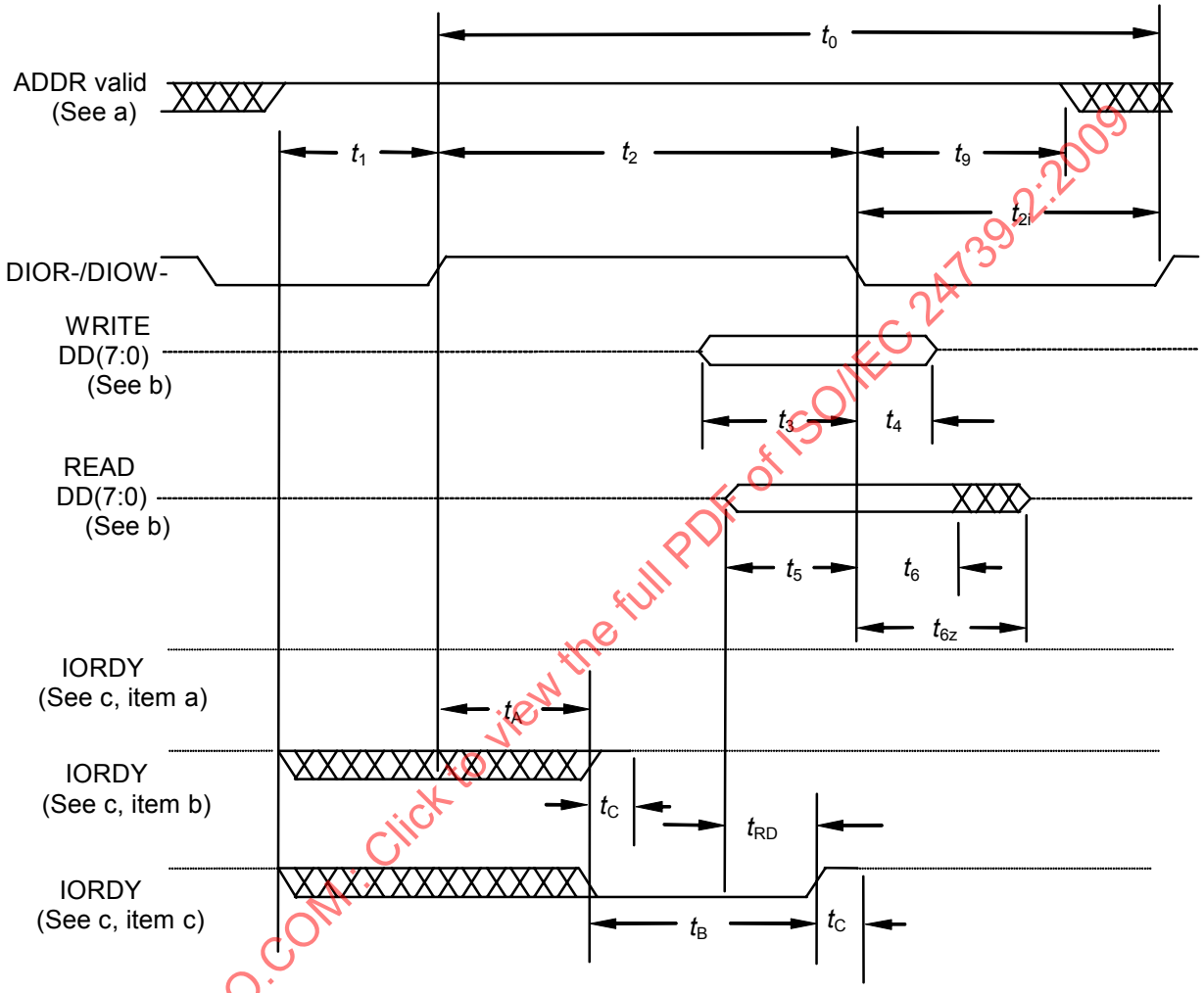
See 3.3.9 for timing diagram conventions.

12.2.2 Register transfers

Figure 65 defines the relationships between the interface signals for register transfers. Peripherals reporting support for PIO mode 3 or 4 shall power-up in a PIO mode 0, 1, or 2.

For PIO modes 3 and above, the minimum value of t_0 is specified by word 68 in the IDENTIFY DEVICE parameter list. Table 50 defines the minimum value that shall be placed in word 68.

Both hosts and devices shall support IORDY when PIO mode 3 or 4 are the currently selected mode of operation.



DMACK- shall remain negated during a register transfer.

a Device address consists of signals CS0-, CS1-, and DA(2:0)

b Data consists of DD(7:0).

c The negation of IORDY by the device is used to extend the register transfer cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:

- a Device never negates IORDY, devices keeps IORDY released: no wait is generated.
- b Device negates IORDY before t_A, but causes IORDY to be asserted before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: no wait generated.
- c Device negates IORDY before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(7:0) for t_{RD} before asserting IORDY.

Figure 65 – Register transfer to/from device

Table 50 – Register transfer to/from device

Register transfer timing parameters			Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Mode 4 ns	Foot-notes to table
t_0	Cycle time	min.	600	383	330	180	120	a, d, e
t_1	Address valid to DIOR-/DIOW- setup	min.	70	50	30	30	25	
t_2	DIOR-/DIOW- pulse width 8-bit	min.	290	290	290	80	70	a
t_{2i}	DIOR-/DIOW- recovery time	min.	-	-	-	70	25	a
t_3	DIOW- data setup	min.	60	45	30	30	20	
t_4	DIOW- data hold	min.	30	20	15	10	10	
t_5	DIOR- data setup	min.	50	35	20	20	20	
t_6	DIOR- data hold	min.	5	5	5	5	5	
t_{6Z}	DIOR- data tristate	max.	30	30	30	30	30	b
t_9	DIOR-/DIOW- to address valid hold	min.	20	15	10	10	10	
t_{RD}	Read Data Valid to IORDY active (if IORDY initially low after t_A)	min.	0	0	0	0	0	
t_A	IORDY Setup time		35	35	35	35	35	c
t_B	IORDY Pulse Width	max.	1 250	1 250	1 250	1 250	1 250	
t_C	IORDY assertion to release	max.	5	5	5	5	5	

a t_0 is the minimum total cycle time, t_2 is the minimum DIOR-/DIOW- assertion time and t_{2i} is the minimum DIOR-/DIOW- negation time. A host implementation shall lengthen t_2 and/or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

b This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is released by the device.

c The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the register transfer cycle is completed. If the device is not driving IORDY negated at the t_A after the activation of DIOR- or DIOW-, then $t5$ shall be met and t_{RD} is not applicable. If the device is driving IORDY negated at the time t_A after the activation of DIOR- or DIOW-, then t_{RD} shall be met and $t5$ is not applicable.

d ATA/ATAPI standards prior to ATA/ATAPI-5 inadvertently specified an incorrect value for mode 2 time t_0 by utilizing the 16-bit PIO value.

e Mode shall be selected no higher than the highest mode supported by the slowest device.

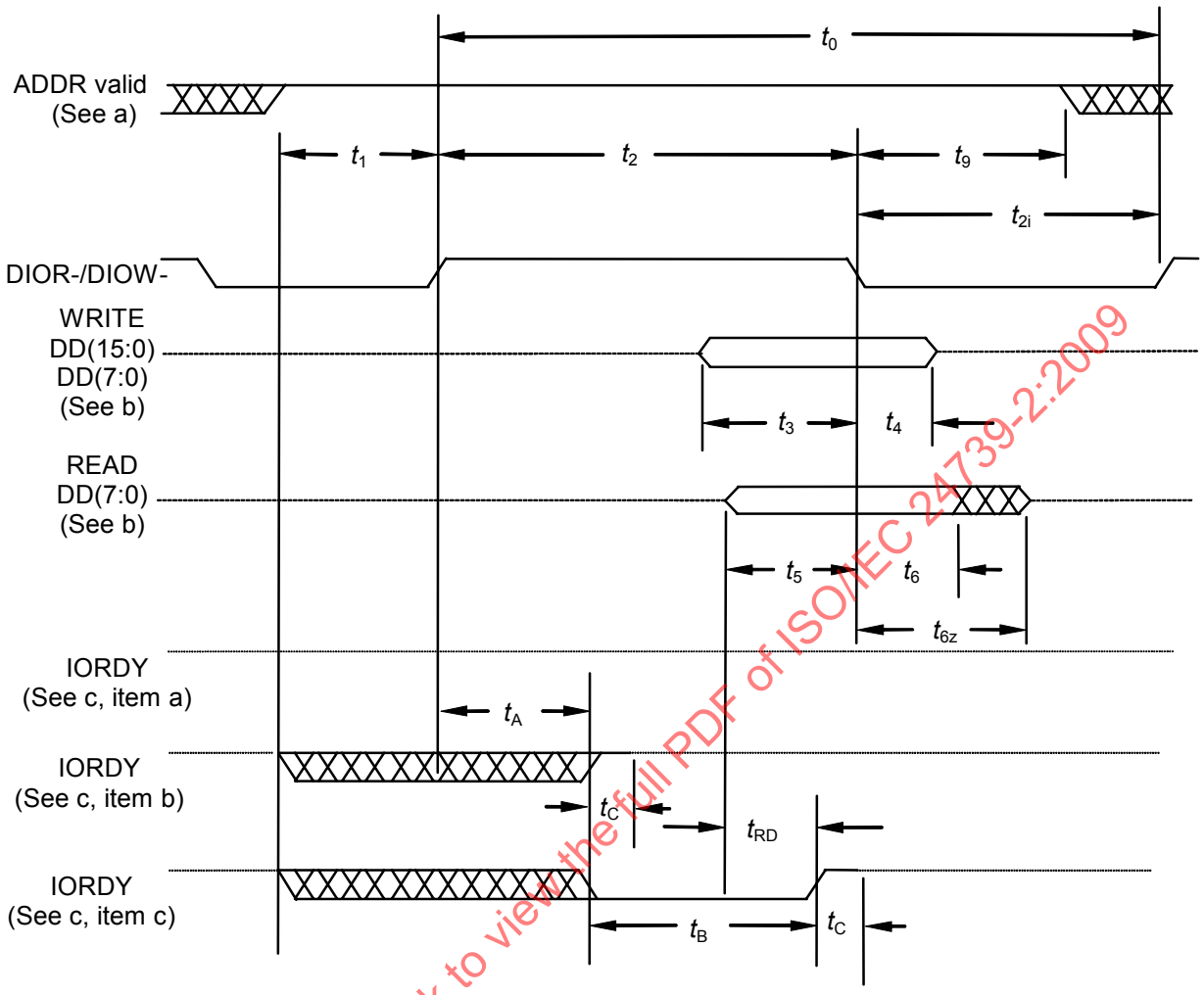
12.2.3 PIO data transfers

Figure 66 defines the relationships between the interface signals for PIO data transfers. Peripherals reporting support for PIO mode 3 or 4 shall power-up in a PIO mode 0, 1 or 2.

For PIO modes 3 and above, the minimum value of t_0 is specified by word 68 in the IDENTIFY DEVICE parameter list. Table 51 defines the minimum value that shall be placed in word 68.

IORDY shall be supported when PIO mode 3 or 4 are the current mode of operation.

NOTE Some devices implementing the PACKET Command feature set prior to ATA/ATAPI-4 power-up in PIO mode 3 and enable IORDY as the default.



DMACK- shall remain negated during a register transfer.

a Device address consists of signals CS0-, CS1-, and DA(2:0)

b Data consists of DD(7:0).

c The negation of IORDY by the device is used to extend the register transfer cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:

- a Device never negates IORDY, devices keeps IORDY released: no wait is generated.
- b Device negates IORDY before t_A, but causes IORDY to be asserted before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: no wait generated.
- c Device negates IORDY before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(7:0) for t_{RD} before asserting IORDY.

Figure 66 – PIO data transfer to/from device

Table 51 – PIO data transfer to/from device

PIO timing parameters			Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Mode 4 ns	Foot-notes to table
t_0	Cycle time	min.	600	383	240	180	120	a, d
t_1	Address valid to DIOR-/DIOW- setup	min.	70	50	30	30	25	
t_2	DIOR-/DIOW-	min.	165	125	100	80	70	a
t_{2i}	DIOR-/DIOW- recovery time	min.	-	-	-	70	25	a
t_3	DIOW- data setup	min.	60	45	30	30	20	
t_4	DIOW- data hold	min.	30	20	15	10	10	
t_5	DIOR- data setup	min.	50	35	20	20	20	
t_6	DIOR- data hold	min.	5	5	5	5	5	
t_{6Z}	DIOR- data tristate	max.	30	30	30	30	30	b
t_9	DIOR-/DIOW- to address valid hold	min.	20	15	10	10	10	
t_{RD}	Read Data Valid to IORDY active (if IORDY initially low after t_A)	min.	0	0	0	0	0	
t_A	IORDY Setup time		35	35	35	35	35	c
t_B	IORDY Pulse Width	max.	1 250	1 250	1 250	1 250	1 250	
t_C	IORDY assertion to release	max.	5	5	5	5	5	

a t_0 is the minimum total cycle time, t_2 is the minimum DIOR-/DIOW- assertion time and t_{2i} is the minimum DIOR-/DIOW- negation time. A host implementation shall lengthen t_2 and/or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

b This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is released by the device.

c The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle is completed. If the device is not driving IORDY negated at the t_A after the activation of DIOR- or DIOW-, then t_5 shall be met and t_{RD} is not applicable. If the device is driving IORDY negated at the time t_A after the activation of DIOR- or DIOW-, then t_{RD} shall be met and t_5 is not applicable.

d Mode may be selected at the highest mode for the device if CS(1:0) and DA(2:0) do not change between read or write cycles or selected at the highest mode supported by the slowest device if CS(1:0) or DA(2:0) do change between read or write cycles.

12.2.4 Multiword DMA data transfer

12.2.4.1 General

Figure 67 through Figure 70 define the timing associated with Multiword DMA transfers.

For Multiword DMA modes 1 and above, the minimum value of t_0 is specified by word 65 in the IDENTIFY DEVICE parameter list. Table 52 defines the minimum value that shall be placed in word 65.

Devices shall power-up with mode 0 as the default Multiword DMA mode.

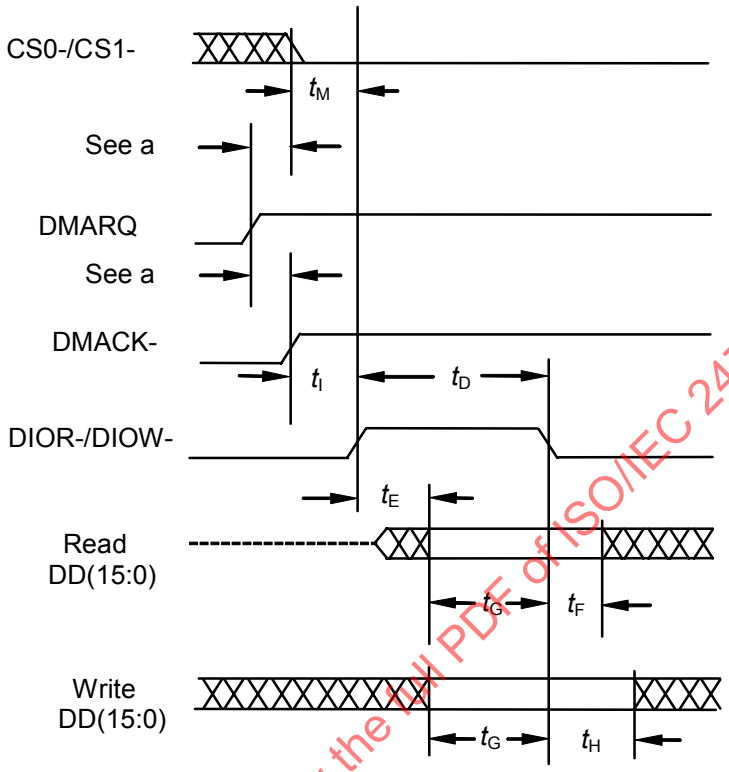
Table 52 – Multiword DMA data transfer

Multiword DMA timing parameters			Mode 0 ns	Mode 1 ns	Mode 2 ns	Foot-notes to table
t_0	Cycle time	min.	480	150	120	a
t_D	DIOR-/DIOW- asserted pulse width	min.	215	80	70	a
t_E	DIOR- data access	max.	150	60	50	
t_F	DIOR- data hold	min.	5	5	5	
t_G	DIOR-/DIOW- data setup	min.	100	30	20	
t_H	DIOW- data hold	min.	20	15	10	
t_I	DMACK to DIOR-/DIOW- setup	min.	0	0	0	
t_J	DIOR-/DIOW- to DMACK hold	min.	20	5	5	
t_{KR}	DIOR- negated pulse width	min.	50	50	25	a
t_{KW}	DIOW- negated pulse width	min.	215	50	25	a
t_{LR}	DIOR- to DMARQ delay	max.	120	40	35	
t_{LW}	DIOW- to DMARQ delay	max.	40	40	35	
t_M	CS(1:0) valid to DIOR-/DIOW-	min.	50	30	25	
t_N	CS(1:0) hold	min.	15	10	10	
t_Z	DMACK- to read data released	max.	20	25	25	

a t_0 is the minimum total cycle time, t_D is the minimum DIOR-/DIOW- assertion time and t_K (t_{KR} or t_{KW}, as appropriate) is the minimum DIOR-/DIOW- negation time. A host shall lengthen t_D and/or t_K to ensure that t_0 is equal to the value reported in the devices IDENTIFY DEVICE data.

12.2.4.2 Initiating a Multiword DMA data burst

The values for the timings for each of the Multiword DMA modes are contained in Table 52.



a The host shall not assert DMACK- or negate both CS0 and CS1 until the assertion of DMARQ is detected. The maximum time from the assertion of DMARQ to the assertion of DMACK- or the negation of both CS0 and CS1 is not defined.

Figure 67 – Initiating a multiword DMA data burst

12.2.4.3 Sustaining a multiword DMA data burst

The values for the timings for each of the multiword DMA modes are contained in Table 52.

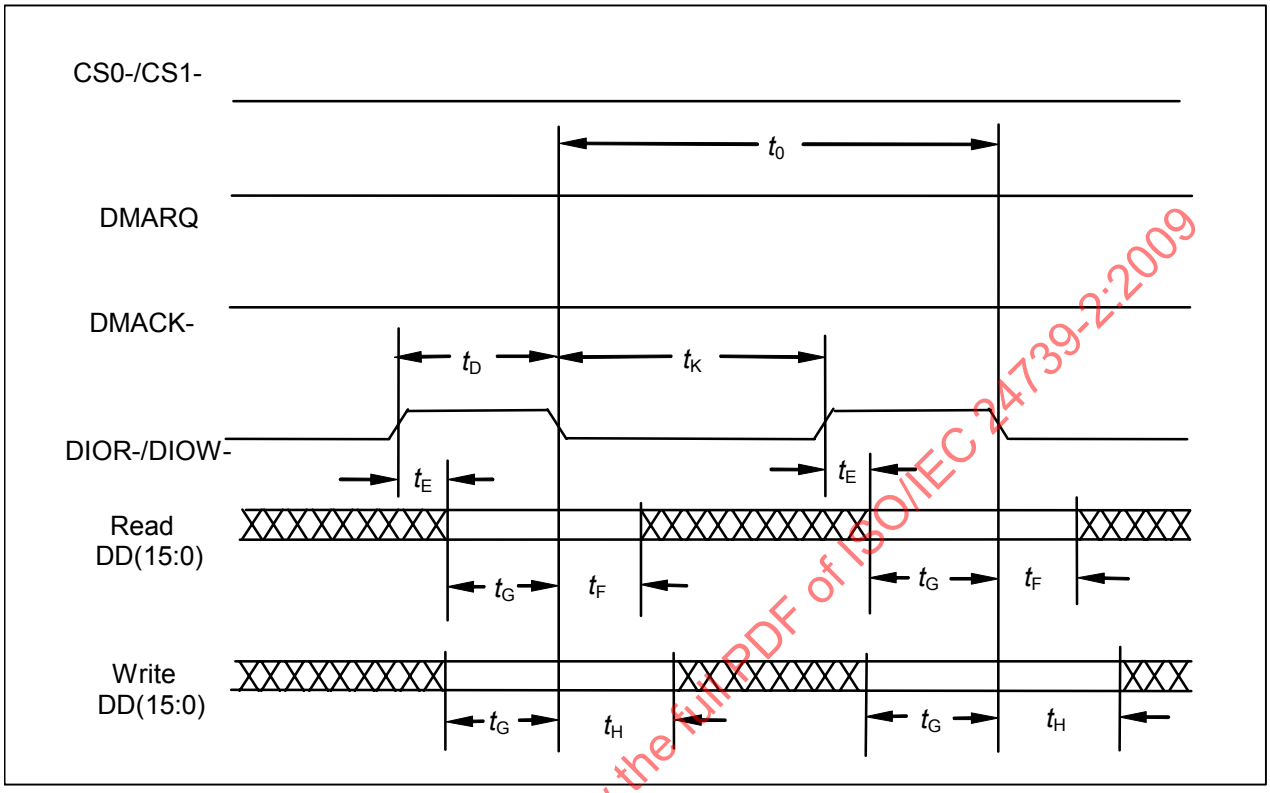
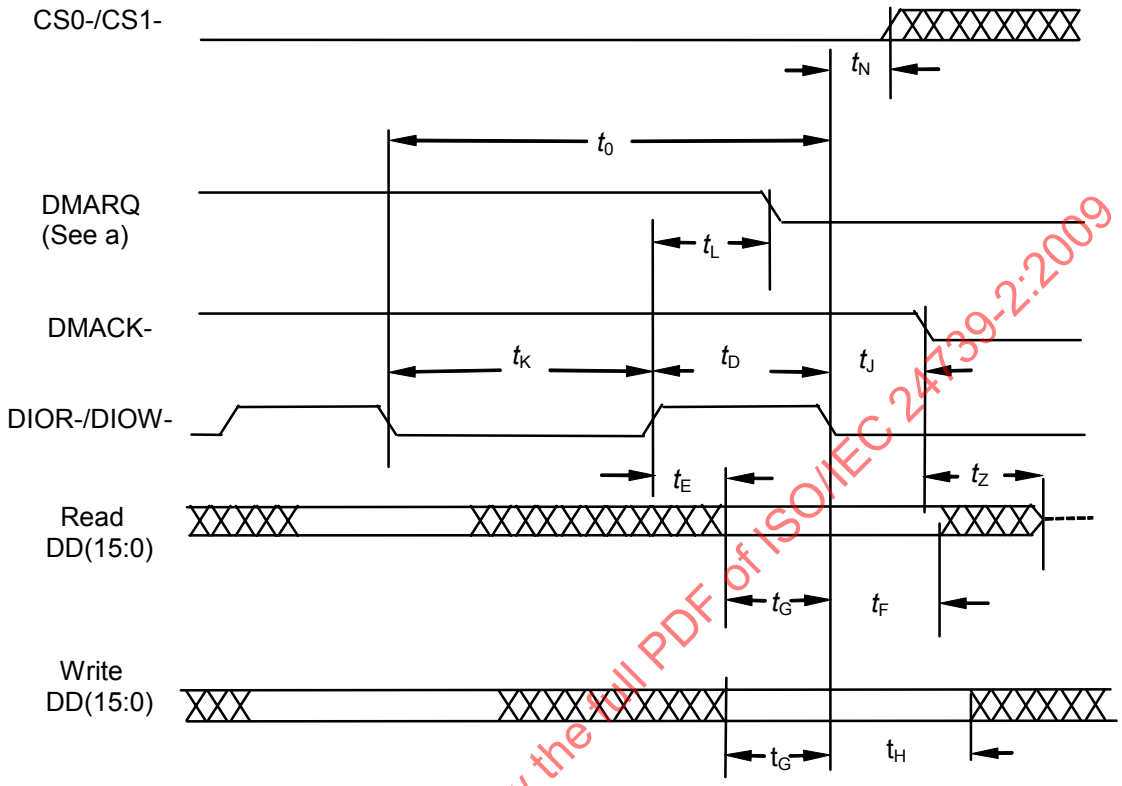


Figure 68 – Sustaining a multiword DMA data burst

12.2.4.4 Device terminating a multiword DMA data burst

The values for the timings for each of the multiword DMA modes are contained in Table 52.

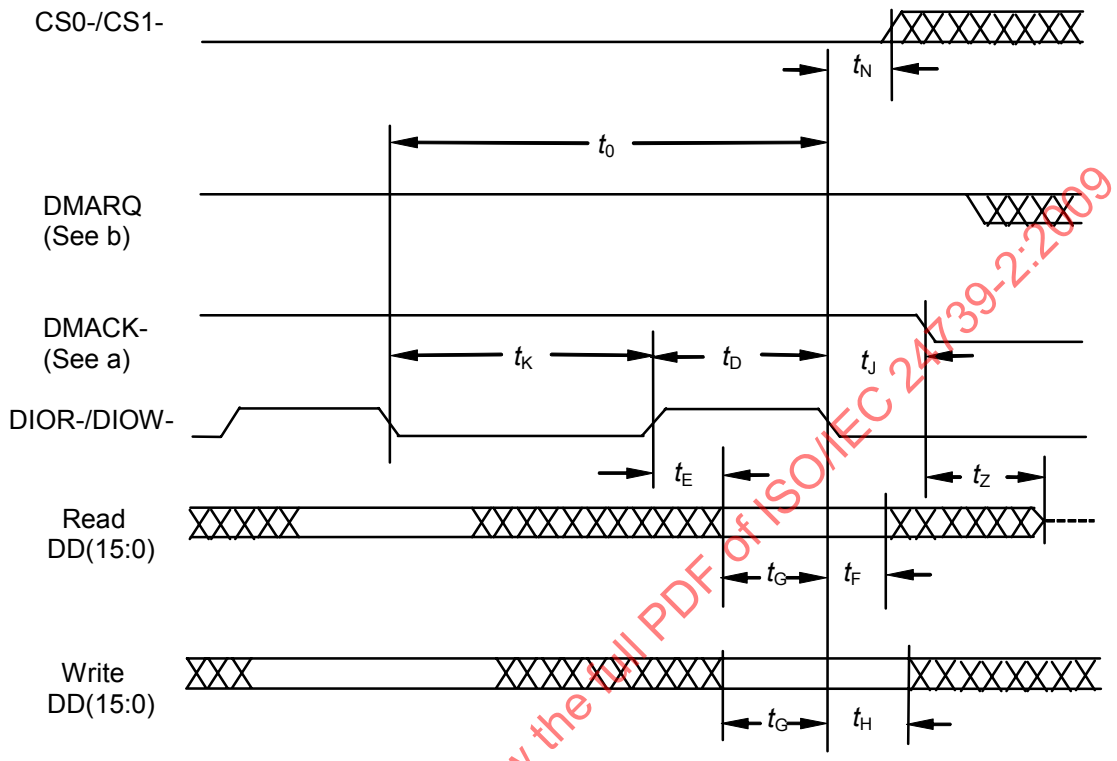


a To terminate the data burst, the Device shall negate DMARQ within t_L of the assertion of the current DIOR- or DIOW- pulse. The last data word for the burst shall then be transferred by the negation of the current DIOR- or DIOW- pulse. If all data for the command has not been transferred, the device shall reassert DMARQ again at any later time to resume the DMA operation, as shown in Figure 66.

Figure 69 – Device terminating a Multiword DMA data burst

12.2.4.5 Host terminating a multiword DMA data burst

The values for the timings for each of the multiword DMA modes are contained in Table 52.



a To terminate the transmission of a data burst, the host shall negate DMACK- within t_J after a DIOR- or DIOW- pulse. No further DIOR- or DIOW- pulses shall be asserted for this burst.

b If the device is able to continue the transfer of data, the device may leave DMARQ asserted and wait for the host to reassert DMACK- or may negate DMARQ at any time after detecting that DMACK- has been negated.

Figure 70 – Host terminating a multiword DMA data burst

12.2.5 Ultra DMA data transfer

12.2.5.1 General

Figure 71 through Figure 80 define the timings associated with all phases of Ultra DMA bursts.

Table 53 contains the values for the timings for each of the Ultra DMA modes. Table 54 contains descriptions and comments for each of the timing values in Table 53, Table 55 contains timings specified for the IC alone.

All timings are worst case across functional voltage, process, temperature and system configuration variances.

Table 53 – Ultra DMA data burst timing requirements

Name	Mode 0 ns		Mode 1 ns		Mode 2 ns		Mode 3 ns		Mode 4 ns		Mode 5 ns		Mode 6 ns		Measurement location
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{2CYCTYP}$	240		160		120		90		60		40		30		Sender
t_{CYC}	112		73		54		39		25		16.8		13.0		(See [a])
t_{2CYC}	230		153		115		86		57		38		29		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		4.0		2.6		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		4.6		3.5		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		4.8		4.0		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8		4.0		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		5.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		10.0		10.0		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10.0		10.0		Host
t_{ZFS}	0		0		0		0		0		35		25		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		25		17.5		Sender
t_{FS}		230		200		170		130		120		90		80	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	0	60	(See [b])
t_{MLI}	20		20		20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10		10		10	(See [c])
t_{ZAH}	20		20		20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	20	50	20	50	Host
t_{RFS}		75		70		60		60		60		50		50	Sender
t_{RP}	160		125		100		100		100		85		85		Recipient
tIORDYZ		20		20		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		50		50		Sender

All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of t_{RFS}, both STROBE and DMARDY- transitions are measured at the sender connector.

[a] The parameter t_{CYC} shall be measured at the recipient's connector farthest from the sender.

[b] The parameter t_{LI} shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

[c] The parameter t_{AZ} shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus the allow for a bus turnaround.

Table 54 – Ultra DMA data burst timing descriptions

Name	Comment
$t_{2CYCTYP}$	Typical sustained average two cycle time
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
t_{DS}	Data setup time at recipient (from data valid until strobe edge) (see [b] and [e])
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid) (see [b] and [e])
t_{DVS}	Data valid setup time at sender (from data valid until strobe edge) (see [c])
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid) (see [c])
t_{CS}	CRC word setup time at device (see [b])
t_{CH}	CRC word hold time device (see [b])
t_{CVS}	CRC word valid setup time at host (from CRC valid until DMACK- negation) (see [c])
t_{CVH}	CRC word valid hold time at sender (from DMACK- negation until CRC may become invalid) (see [c])
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)
t_{LI}	Limited interlock time (see [a])
t_{MLI}	Interlock time with minimum (see [a])
t_{UI}	Unlimited interlock time (see [a])
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)
t_{ZAH}	Minimum delay time required for output
t_{ZAD}	Drivers to assert or negate (from released)
t_{ENV}	Envelope time (from DMACK- to STOP and HDMARDY- during data in burst initiation and from DMACK- to STOP during data out burst initiation)
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating DMARDY-)
t_{IORDYZ}	Maximum time before releasing IORDY
t_{ZIORDY}	Minimum time before driving IORDY (see [d])
t_{ACK}	Setup and hold times for DMACK- (before assertion or negation)
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)

[a] The parameters t_{UI}, t_{MLI} (in Figure 74 and Figure 75) and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.

[b] 80-conductor cabling (see 7.3) shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes greater than 2.

[c] Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 pF and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

[d] For all modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY- giving it a known state when released.

[e] The parameters t_{DS} and t_{DH} for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for t_{DS} and t_{DH} for mode 5 at the middle connector being 3.0 ns and 3.9 ns, respectively.

Table 55 – Ultra DMA sender and recipient IC timing requirements

Name	Mode 0 ns		Mode 1 ns		Mode 2 ns		Mode 3 ns		Mode 4 ns		Mode 5 ns		Mode 6 ns	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
t_{DSIC}	14.7		9.7		6.8		6.8		4.8		2.3		2.3	
t_{DHIC}	4.8		4.8		4.8		4.8		4.8		2.8		2.8	
t_{DVSIC}	72.9		50.9		33.9		22.6		9.5		6.0		5.2	
t_{DVHIC}	9.0		9.0		9.0		9.0		9.0		6.0		5.2	

Comment	
t_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge) (see [a])
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid) (see [a])
t_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge) (see [b])
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see [b])

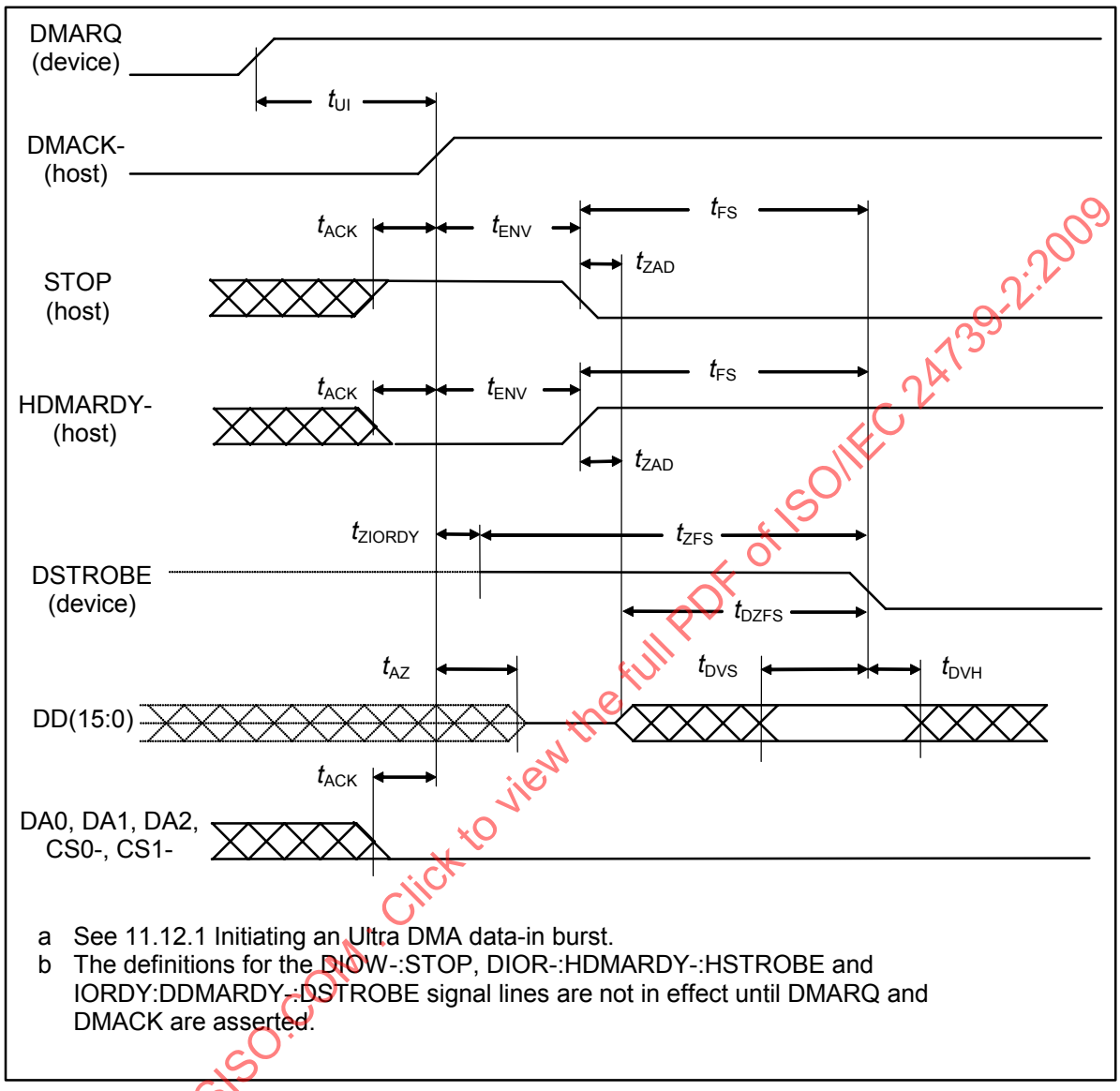
All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

[a] The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at t_{DSIC} and t_{DHIC} timing (as measured through 1.5 V).

[b] The parameters t_{DVSIC} and t_{DVHIC} shall be met for lumped capacitive loads of 15 pF and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

12.2.5.2 Initiating an Ultra DMA data-in burst

The values for the timings for each of the Ultra DMA modes are contained in 12.2.5.

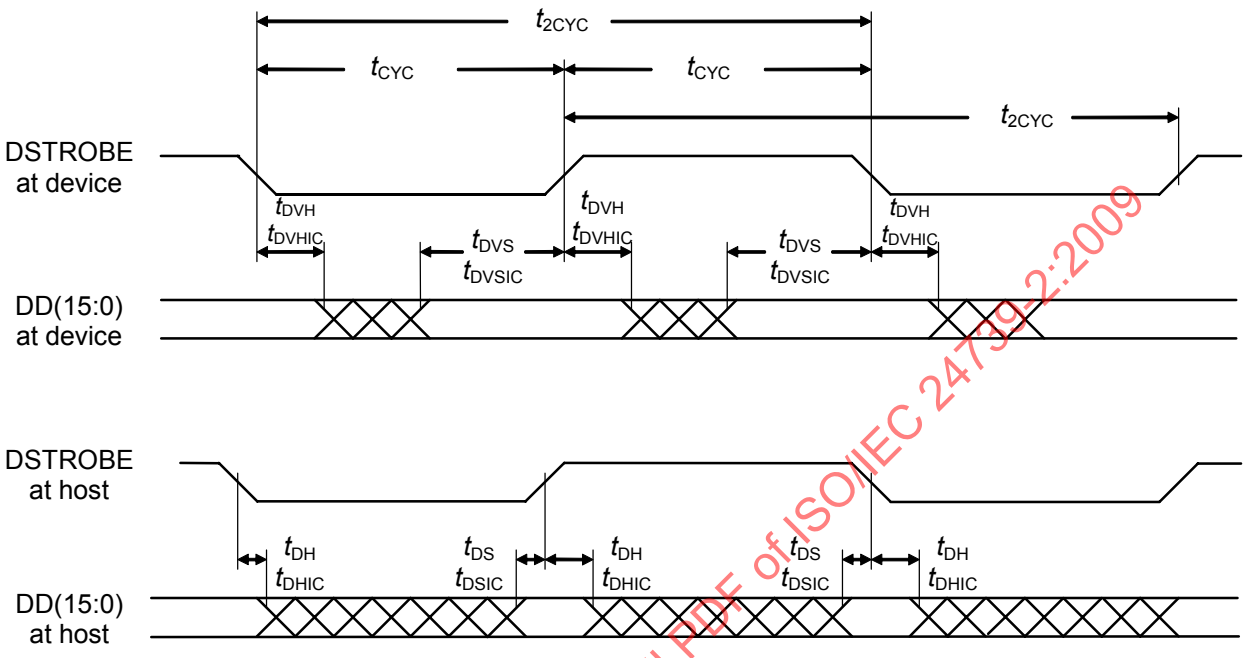


a See 11.12.1 Initiating an Ultra DMA data-in burst.
b The definitions for the DIOW-:STOP, DIOR-:HDMARDY-:HSTROBE and IORDY:DDMARDY-:DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

Figure 71 – Initiating an Ultra DMA data-in burst

12.2.5.3 Sustained Ultra DMA data-in burst

The values for the timings for each of the Ultra DMA modes are contained in 12.2.5.

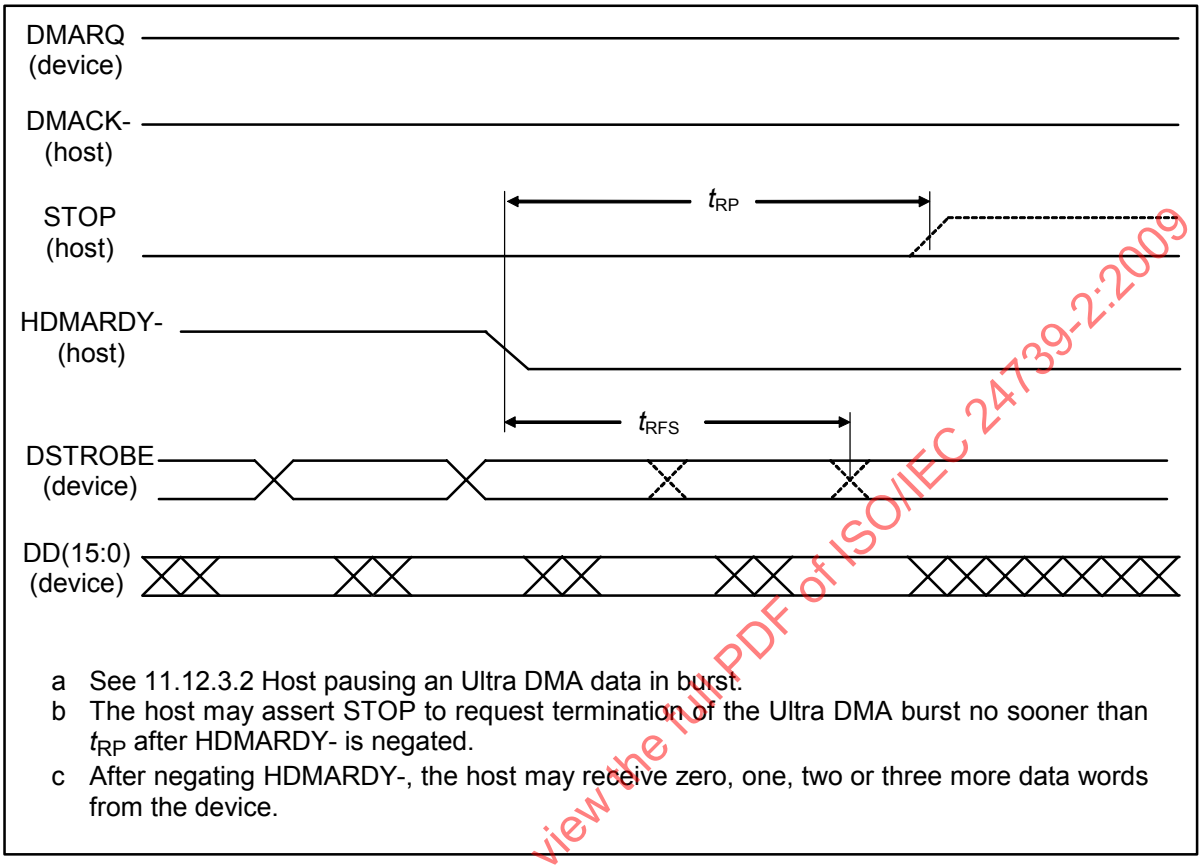


a See 11.12.2, The data in transfer.
b DD(15:0) and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

Figure 72 – Sustained Ultra DMA data-in burst

12.2.5.4 Host pausing an Ultra DMA data-in burst

The values for the timings for each of the Ultra DMA modes are contained in 12.2.5.

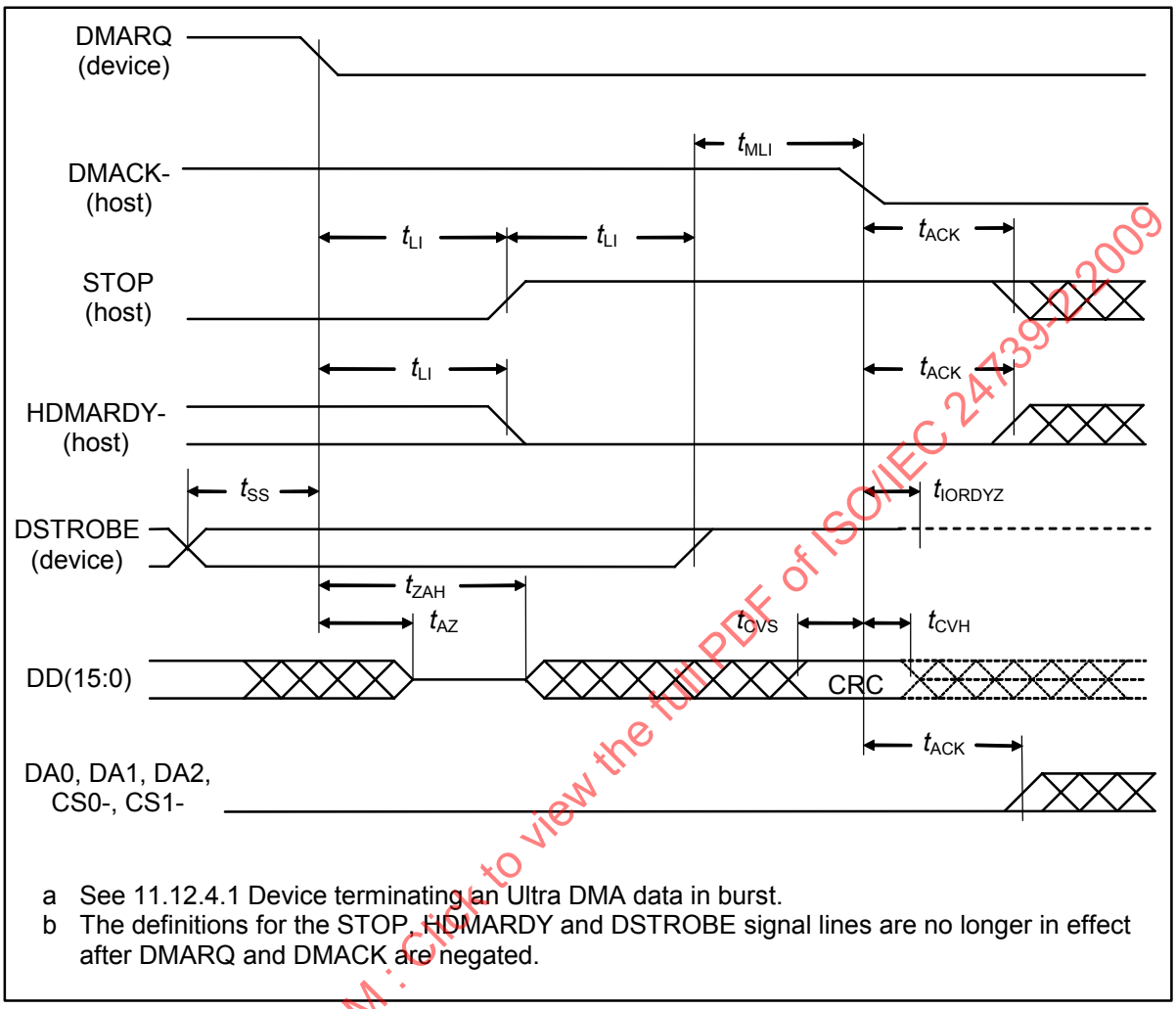


a See 11.12.3.2 Host pausing an Ultra DMA data in burst.
b The host may assert STOP to request termination of the Ultra DMA burst no sooner than t_{RP} after HDMARDY- is negated.
c After negating HDMARDY-, the host may receive zero, one, two or three more data words from the device.

Figure 73 – Host pausing an Ultra DMA data-in burst

12.2.5.5 Device terminating an Ultra DMA data-in burst

The values for the timings for each of the Ultra DMA modes are contained in 12.2.5.

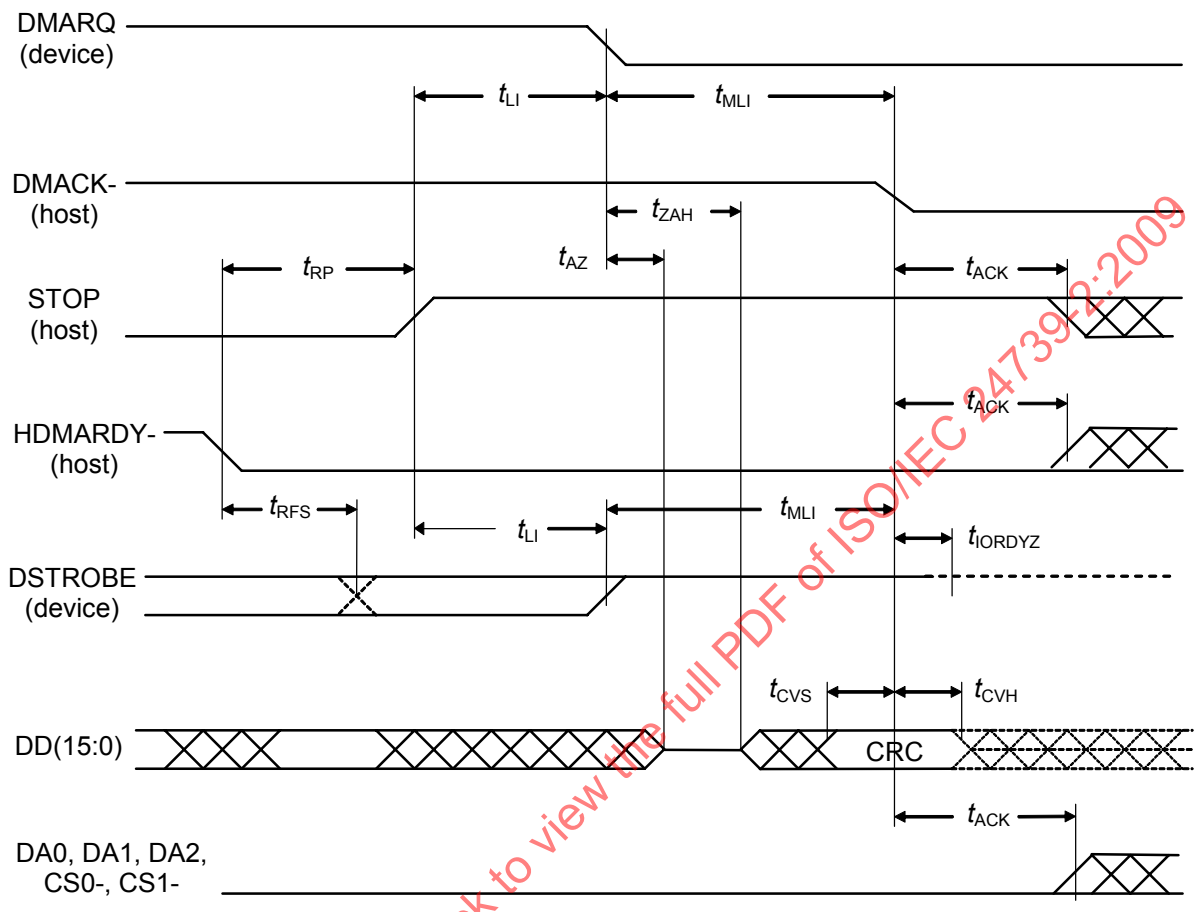


a See 11.12.4.1 Device terminating an Ultra DMA data in burst.
b The definitions for the STOP, HDMARDY and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 74 – Device terminating an Ultra DMA data-in burst

12.2.5.6 Host terminating an Ultra DMA data-in burst

The values for the timings for each of the Ultra DMA modes are contained in 12.2.5.

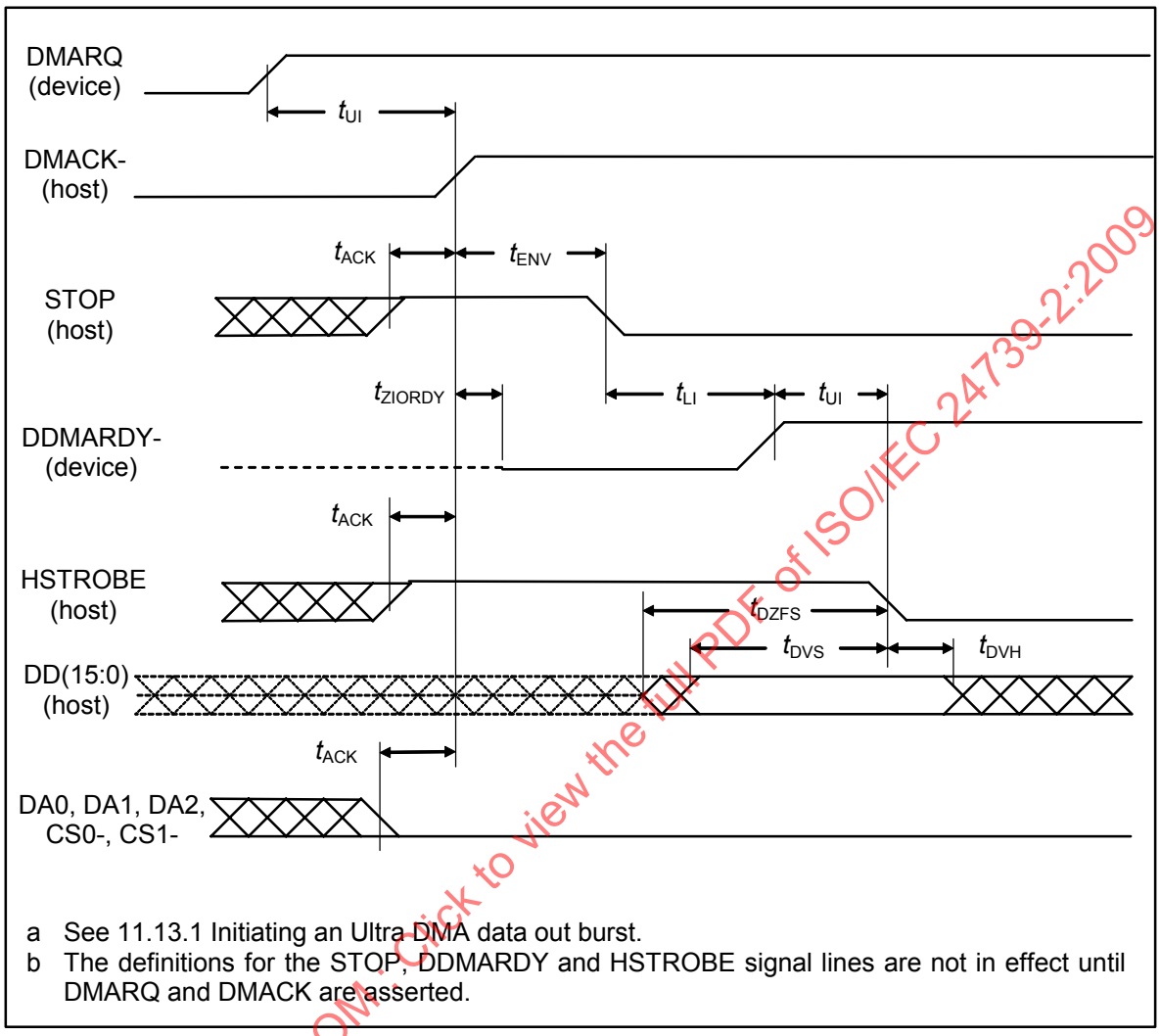


a See 11.12.4.2 Host pausing an Ultra DMA data in burst.
b The definitions for the STOP, HDMARDY and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 75 – Host terminating an Ultra DMA data-in burst

12.2.5.7 Initiating an Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in 12.2.5.

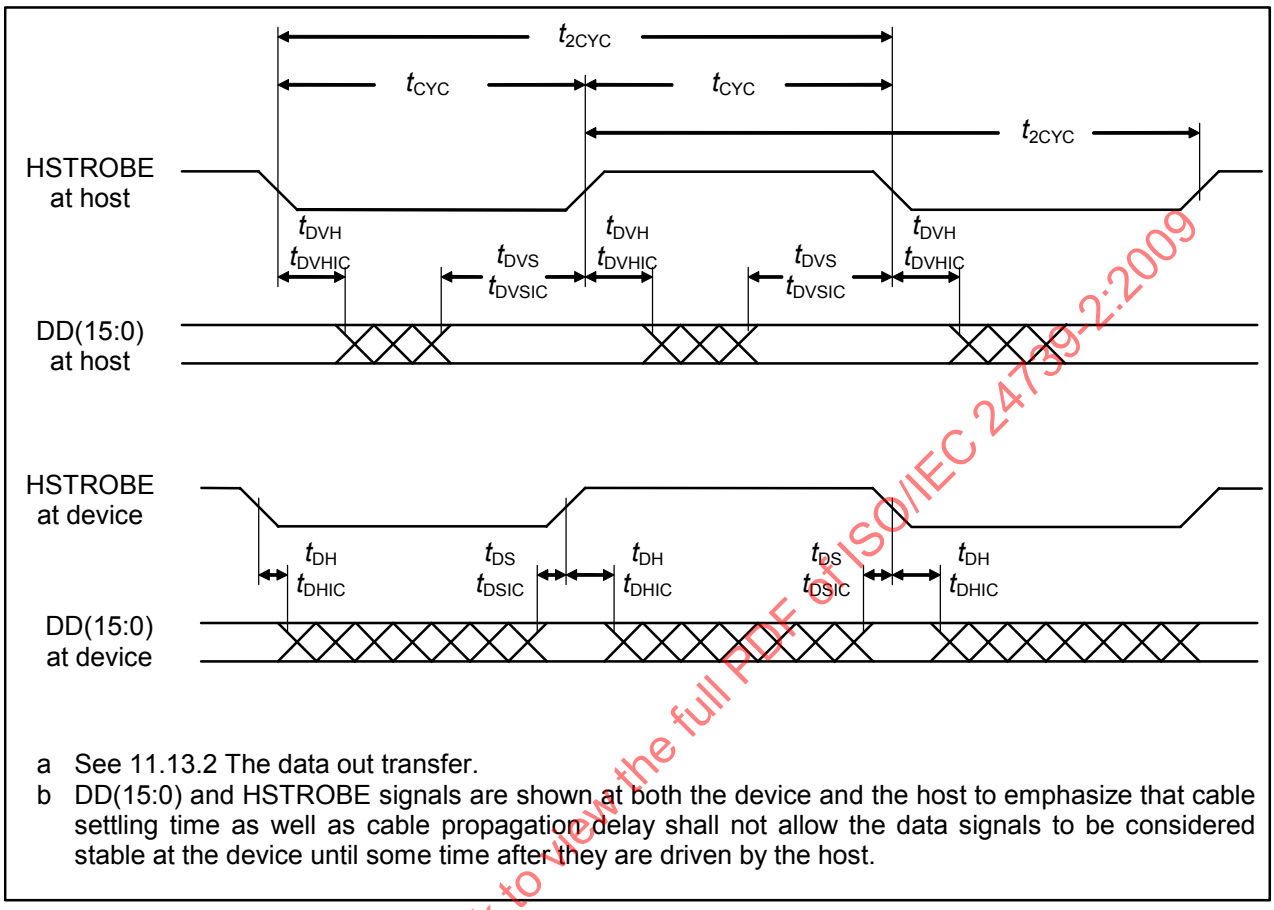


a See 11.13.1 Initiating an Ultra DMA data out burst.
b The definitions for the STOP, DDMARDY and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

Figure 76 – Initiating an Ultra DMA data-out burst

12.2.5.8 Sustained Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in 12.2.5.

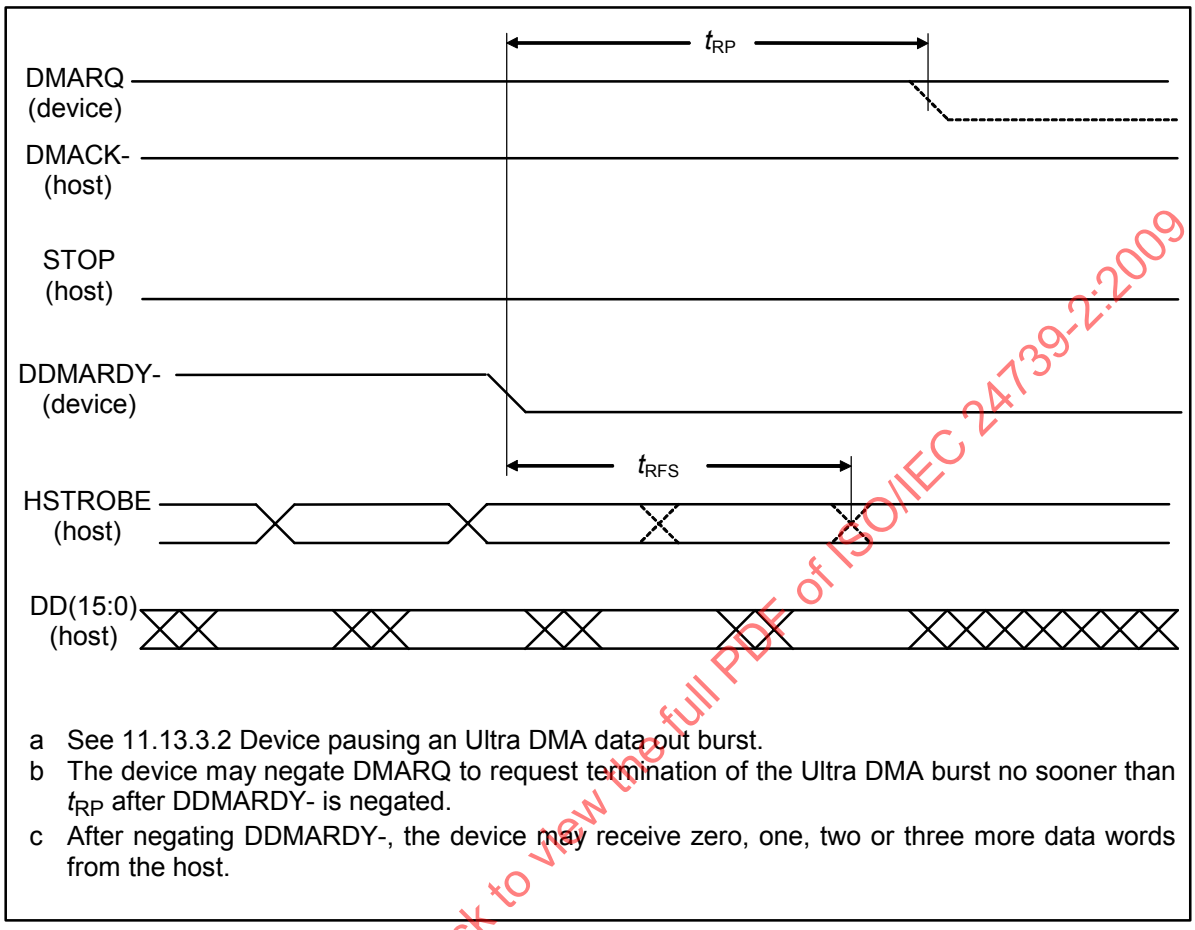


a See 11.13.2 The data out transfer.
b DD(15:0) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

Figure 77 – Sustained Ultra DMA data-out burst

12.2.5.9 Device pausing an Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in 12.2.5.

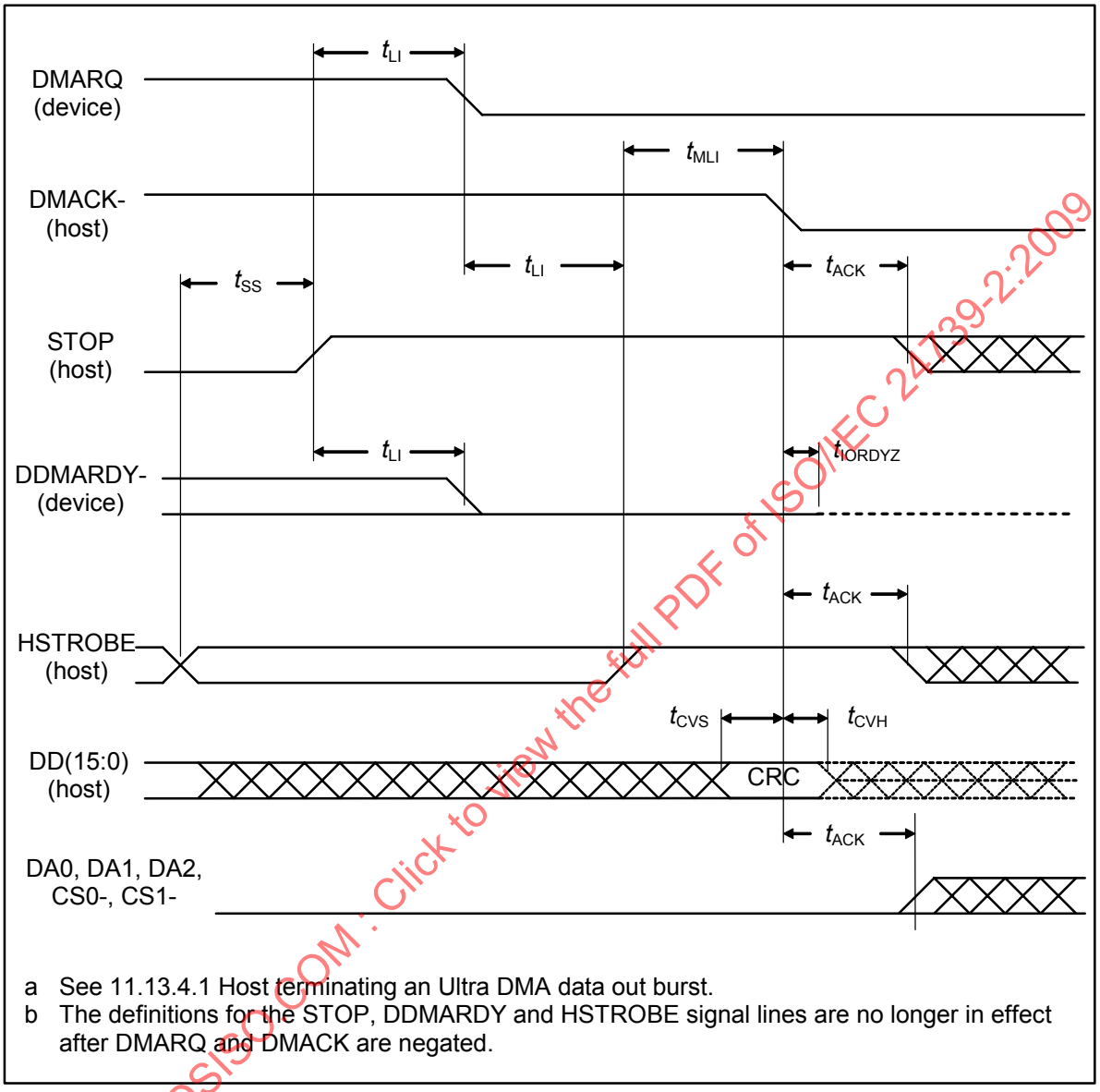


a See 11.13.3.2 Device pausing an Ultra DMA data out burst.
b The device may negate DMARQ to request termination of the Ultra DMA burst no sooner than t_{RP} after DDMARDY- is negated.
c After negating DDMARDY-, the device may receive zero, one, two or three more data words from the host.

Figure 78 – Device pausing an Ultra DMA data-out burst

12.2.5.10 Host terminating an Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in 12.2.5.

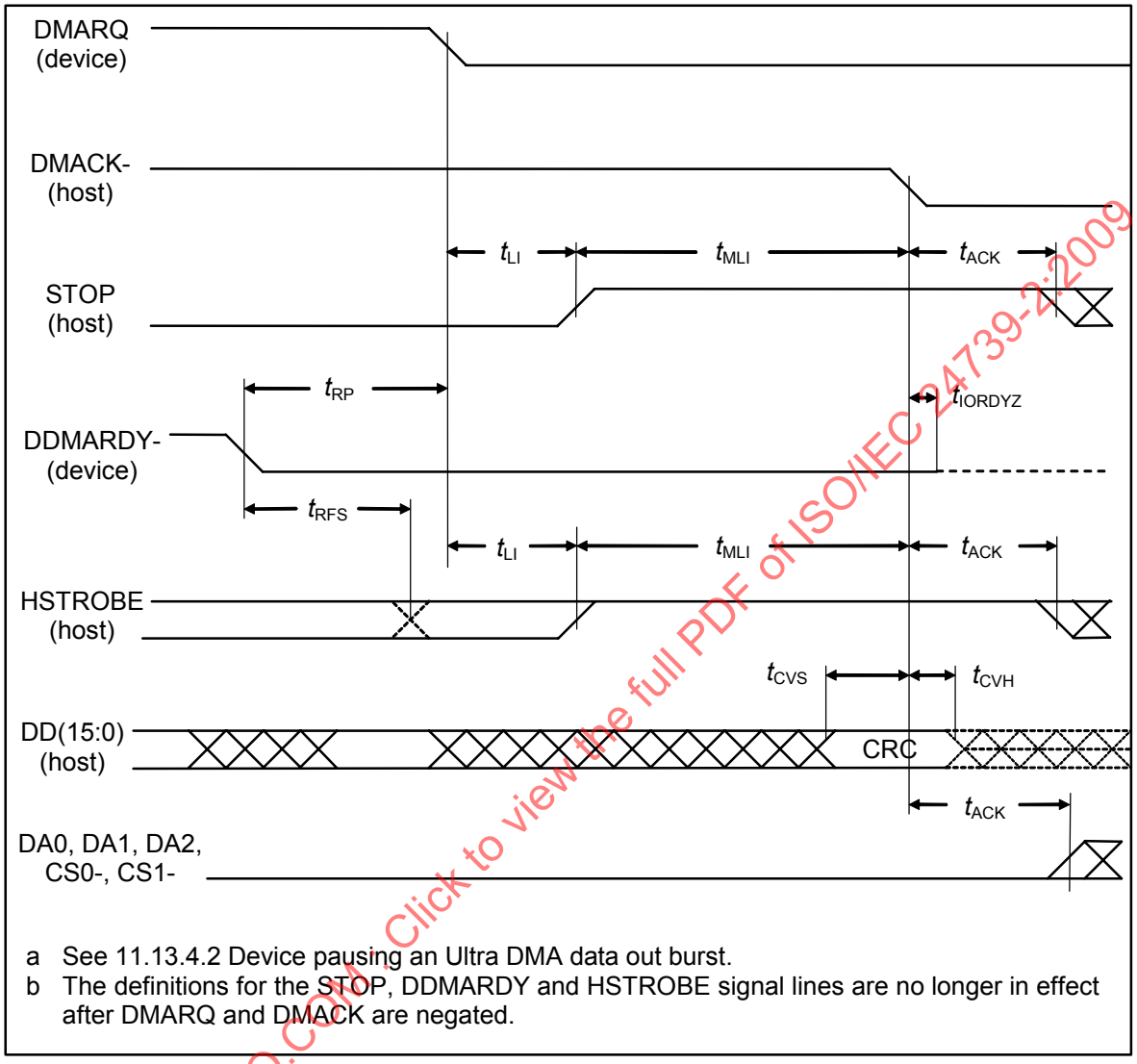


a See 11.13.4.1 Host terminating an Ultra DMA data out burst.
b The definitions for the STOP, DDMARDY and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 79 – Host terminating an Ultra DMA data-out burst

12.2.5.11 Device terminating an Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in 12.2.5.



a See 11.13.4.2 Device pausing an Ultra DMA data out burst.
b The definitions for the STOP, DDMARDY and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 80 – Device terminating an Ultra DMA data-out burst

For Clauses 13 to 20 as well as Annex A and Annex B, refer to 3.4.

13 Serial interface overview

See ISO/IEC 24739-3:2010.

14 Serial interface physical layer

See ISO/IEC 24739-3:2010.

15 Serial interface link layer

See ISO/IEC 24739-3:2010.

16 Serial interface transport layer

See ISO/IEC 24739-3:2010.

17 Serial interface device command layer

See ISO/IEC 24739-3:2010.

18 Host command layer

See ISO/IEC 24739-3:2010.

19 Serial interface host adapter register interface

See ISO/IEC 24739-3:2010.

20 Serial interface error handling

See ISO/IEC 24739-3:2010.

Annex A
(informative)

Command Set summary

Void, see 3.4.

(See ISO/IEC 24739-1:2009)

Annex B
(informative)

Design and programming considertions for large physical sector sizes

Void, see 3.4.

(See ISO/IEC 24739-1:2009)

Annex C
(informative)

Device determination of cable type

C.1 Overview

This standard requires that, for systems using a cable assembly, an 80-conductor cable assembly shall be installed before a system may operate with Ultra DMA modes greater than 2. However, some hosts have not implemented circuitry to determine the installed cable type by detecting whether PDIAG-:CBLID- is connected to ground as mandated by this standard. The following describes an alternate method for using IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data from the device to determine the cable type. It is not recommended that a host use the method described in this annex.

If a host uses IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data from the device to determine the cable type, then a 0.047 µF capacitor shall be installed from CBLID- to ground at the host connector. The tolerance on this capacitor is ±20 % or less. After receiving an IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command the device detects the presence or absence of the capacitor by asserting PDIAG-:CBLID- to discharge the capacitor, releasing PDIAG- and sampling PDIAG-:CBLID- before the installed capacitor could recharge through the 10 kΩ pull-up resistor(s) on PDIAG-:CBLID- at the device(s).

If the host system has a capacitor on PDIAG-:CBLID- and a 40-conductor cable is installed, the rise time of the signal will be slow enough that the device will sample PDIAG-:CBLID- while the signal is still below V_{IL}. Otherwise, if PDIAG-:CBLID- is not connected from the host connector to the devices in an 80-conductor cable assembly, the device will detect that the signal is pulled above V_{IH} through the resistor(s) on the device(s). The capacitor test results will then be reported to the host in the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data. The host will use the data to determine the maximum transfer rate of which the system is capable and use this information when setting the transfer rate using the SET FEATURES command.

C.2 Sequence for device detection of installed capacitor

The following is the sequence for a host using IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data from the device to determine the cable type:

a) the host issues an IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command (according to device type) first to Device 1 and then to Device 0 after every power-on or hardware reset sequence (the command is issued to Device 1 first to ensure that Device 1 releases PDIAG-:CBLID- before Device 0 is selected. Device 0 will be unable to distinguish a discharged capacitor if Device 1 is driving the line to its electrically low state. Issuing the command to Device 1 forces it to release PDIAG-:CBLID-);

b) the selected device asserts PDIAG-:CBLID- for at least 30 µs after receipt of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command but before transferring data for the command;

c) the device releases PDIAG-:CBLID- and samples it between two and thirteen µs after release;

d) if the device detects that PDIAG-:CBLID- is below V_{IL}, then the device returns a value of zero in bit 13 of word 93 in its IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data (if the host system has a capacitor on that signal and a 40-conductor cable is installed, the rise time of the signal will be slow enough that it will be sampled by the device while it is still below V_{IL});

e) if the device detects that the signal is above V_{IH}, then the device returns a value of one in bit 13 of word 93 in its IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data. This signal

is not connected between the host and the devices in an 80-conductor cable assembly, thus, the sampling device will see this signal pulled above V_{IH} through the 10 kΩ resistor(s) installed on the device(s);

f) the host then uses its knowledge of its own capabilities and the content of word 88 and word 93 to determine the Ultra DMA modes of which the system is capable;

g) the host then uses the SET FEATURES command to set the transfer mode.

Figure C.1 Illustrates an example configuration of a system where the device detects a 40-conductor cable. Table C.1 describes the result of device detection when a capacitor is installed. Table C.2 describes the result of device based cable detection when a capacitor is not installed.

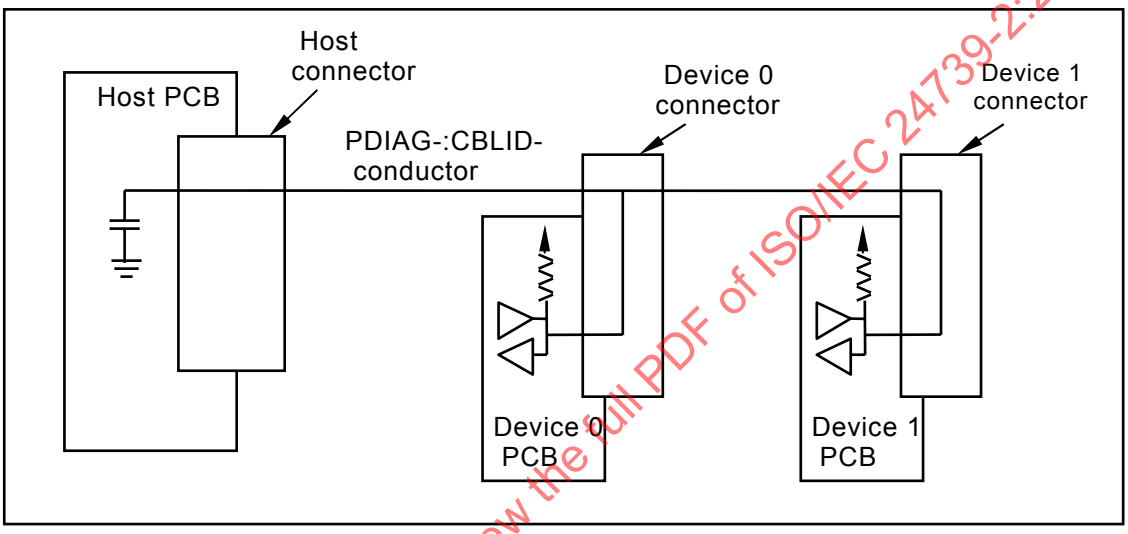


Figure C.1 – Example configuration of a system where the device detects a 40-conductor cable

Table C.1 – Device detection of installed capacitor

Cable assembly type	Device 1 releases PDIAG-	Value reported in ID data by device	Device-determined cable type	Determination correct?
40-conductor	Yes	0	40-conductor	Yes
80-conductor	Yes	1	80-conductor	Yes
40-conductor	No	0	40-conductor	Yes
80-conductor	No	0	40-conductor	No (see [a])
[a] Ultra DMA modes greater than 2 will not be set even though the system supports them.				

Table C.2 – Results of device based cable detection if the host does not have the capacitor installed

Cable assembly type	Device 1 releases PDIAG-	Value reported in ID data by device	Device-determined cable type	Determination correct?
40-conductor	Yes	1	80-conductor	No (see [a])
80-conductor	Yes	1	80-conductor	Yes
40-conductor	No	0	40-conductor	Yes
80-conductor	No	0	40-conductor	No (see [b])
[a] Ultra DMA modes greater than 2 may be set incorrectly resulting in ICRC errors.				
[b] Ultra DMA modes greater than 2 will not be set even though the system supports them.				

C.3 Using the combination of methods for detecting cable type

Determining the cable assembly type may be done either by the host sensing the condition of the PDIAG-:CBLID- signal, by relying on information from the device or a combination of both methods. Table C.3 describes the results of using both host and device cable detection methods.

Table C.3 – Results from using both host and device cable detection methods

Cable assembly type	Device 1 Releases PDIAG-	Electrical state of CBLID- at host	Value reported in ID data by device	Determined cable type	Determination correct?
40-conductor	Yes	1	0	40	Yes
80-conductor	Yes	0	1	80	Yes
40-conductor	No	0	0	40	Yes (see [a])
80-conductor	No	0	0	40	No (see [a])

[a] The 0,0 result is independent of cable type and indicates that Device 1 is incorrectly asserting PDIAG-. When the host determines this result, it shall not operate with Ultra DMA modes greater than 2 and it may respond in several ways:

1) 1 report that Device 1 is incompatible with Ultra DMA modes higher than 2 and should be used on a different port in order to use those modes on the port being detected;

2) 2 report that Device 1 is not allowing the cable type to be properly detected;

3) 3 do not notify the user of any problem but detect the cable as a 40-conductor.

Table C.4 illustrates intermediate results for all combinations of cable, device and host, for hosts that support Ultra DMA modes greater than 2.

Table C.4 – Results for all combinations of device and host cable detection methods

Design options			Intermediate actions and results						Results
80-conductor cable installed	Device supports UDMA modes >2	Host senses PDIAG-: CBLID-	Host uses ID data, capacitor installed	Host capacitor connected to device	Device tests for capacitor	Capacitor detected	ID word 93 bit 13 value	Host checks ID word 93 bit 13	Host may set UDMA mode >2
No	No	Yes	No	No	No	No	0	No	No
No	Yes	Yes	No	No	Yes	No	1	No	No
Yes	No	Yes	No	No	No	No	0	No	No
Yes	Yes	Yes	No	No	Yes	No	1	No	Yes
No	No	No	Yes	Yes	No	No	0	Yes	No
No	Yes	No	Yes	Yes	Yes	Yes	0	Yes	No
Yes	No	No	Yes	No	No	No	0	Yes	No
Yes	Yes	No	Yes	No	Yes	No	1	Yes	Yes

Annex D
(informative)

Signal integrity and UDMA guide

D.1 General

This annex is intended as an aid to the implementation of Ultra DMA in host systems, ATA controllers and peripherals. Clarifications of some aspects of the protocol and details not specifically stated in the normative clauses of this standard have been included for the benefit of component, PCB and device driver engineers. This annex is not intended to be comprehensive but rather informative on subjects that have caused design questions. Included are warnings about proper interpretation of protocol where interpretation errors seem possible. The information provided is relevant to implementation of all Ultra DMA modes 0 through 6, as well as earlier protocols.

This annex uses the term data-out to indicate a transfer from the host to a device and data-in to indicate a transfer from the device to the host.

The ATA bus is a storage interface originally designed for the ISA Bus of the IBM PC/AT™. With the advent of faster host systems and devices, the definition of the bus has been expanded to include new operating modes. Each of the PIO modes, numbered zero through four, is faster than the one before (higher numbers translate to faster transfer rates). PIO modes 0, 1 and 2 correspond to transfer rates for the interface as was originally defined with maximum transfer rates of (3.3, 5.2 and 8.3) MB/s, respectively. PIO mode 3 defines a maximum transfer rate of 11.1 MB/s and PIO mode 4 defines a maximum rate of 16.7 MB/s. Additionally, Multiword DMA and Ultra DMA modes have been defined. Multiword DMA mode 0, 1 and 2 have maximum transfer rates of (4.2, 13.3 and 16.7) MB/s, respectively. Ultra DMA modes 0, 1, 2, 3, 4 and 5 have maximum transfer rates of (16.7, 25, 33.3, 44.4, 66.7, 100 and 133) MB/s, respectively.

Ultra DMA features such as increased frequencies, double-edge clocking and non-interlocked signalling require improved signal integrity on the bus relative to that required by PIO and Multiword DMA modes. For Ultra DMA modes 0, 1 and 2 this is achieved by the use of partial series termination and controlled slew rates. For modes 3 and above an 80-conductor cable assembly is required in addition to partial series termination and controlled slew rates. This cable assembly has ground lines between all signal lines on the bus in order to control impedance and reduce crosstalk, eliminating many of the signal integrity problems inherent to the 40-conductor cable assembly. However, many of the design considerations and measurement techniques required for the 80-conductor cable assembly are different from those used for the 40-conductor assembly. Hosts and devices capable of Ultra DMA modes greater than 2 should be designed to meet all requirements for operation with both cable types. Unless otherwise stated, 40- and 80-conductor cables are assumed to be 46 cm (18 in) long, the maximum allowed by this standard. Timing and signal integrity issues, as discussed, apply to this length cable.

D.2 Issues

D.2.1 General

The following subclauses describe the issues and design challenges while providing suggestions for implementation with respect to timing, crosstalk, ground bounce and ringing.

D.2.2 Timing

D.2.2.1 Overview

Two of the features Ultra DMA introduced to the bus are double-edge clocking and non-interlocked (also known as source-synchronous) signalling. Double-edge clocking allows a word of data to be transferred on each edge of STROBE (this is HSTROBE for an Ultra DMA data-out transfer and DSTROBE for a data-in transfer), resulting in doubling the data rate without increasing the fundamental frequency of signalling on the bus. Non-interlocked signalling means that DATA and STROBE are both generated by the sender during a data transfer. In addition, to signal integrity issues such as clocking the same data twice due to ringing on the STROBE signal and delay-limited interlock timings on the bus, non-interlocked signalling makes settling time and skew between different signals on the bus critical for proper Ultra DMA operation.

D.2.2.2 Cabling

The 80-conductor cable assembly adds 40 ground lines to the cable between the 40 signal lines defined for the 40-conductor cable assembly. These added ground lines are connected inside each connector on the cable assembly to the seven ground pins defined for the 40-conductor cable assembly. These additional ground lines allow the return current for each signal line to follow a closer path to the outgoing current than was allowed by the grounding scheme in the 40-conductor cable assembly. This results in a lower impedance and greatly reduced crosstalk for signals on the data bus. The controlled impedance and reduced crosstalk of the 80-conductor cable assembly results in much improved behavior of electrical signals on the bus and reduces the data settling time to effectively zero regardless of switching conditions. Thus, the signal at the recipient is monotonic, such that the first crossing of the input threshold is considered final. Reducing the time allowed for data settling time (DST) from greater than 25 ns in Ultra DMA mode 2, to 0 ns with the 80-conductor cable assembly allows nominal cycle time to be reduced from 60 ns for mode 2, to 15 ns for mode 6.

D.2.2.3 Skew

Skew is the difference in total propagation delay between two signals as they transit the bus. Propagation delay is the amount of time required for a single input signal at one part of the system to cause a disturbance to be observed at another part of the system in a system containing continuously distributed capacitance and inductance. Propagation delay is determined by the velocity of light within the dielectric materials containing the electric fields in the system. For systems with uniform properties along their length, propagation delay is often specified as seconds per foot or seconds per meter.

Skew will be positive or negative depending on which signal is chosen as the reference. All skews in the Ultra DMA timing derivations are defined as STROBE delay minus data delay. A positive skew is a STROBE that is delayed more than the data.

Skew corresponds to the reduction in setup and hold times that occurs between the sender and the recipient. If the bus contributes skew that exceeds the difference between the setup time produced by the sender and that required by the recipient, data will be stored incorrectly. The same is true for hold time. Skew between signals is caused by differences in the electrical characteristics of the paths followed by each signal.

Ultra DMA modes higher than 4 require less skew within the physical cable system than lower modes. In order to reduce the amount of skew created as signals transit the system, modes higher than 4 place a number of new requirements on the analog electrical aspects of system design. The primary requirement is that all devices and hosts supporting modes higher than 4 use 3.3 V signalling. This eliminates the contribution to skew from the asymmetry of the input thresholds with the previous 5 V V_{oH}. A second requirement is that hosts use a 4.7 kΩ pull-up resistor on IORDY/DSTROBE instead of the 1 kΩ resistor used for previous modes. The pull-up shall be to the host's 3.3 V internal supply. Third, the total output impedance consisting of driver resistance plus series termination resistor shall match the typical cable impedance of 75 Ω to 85 Ω.

D.2.2.4 Source-terminated bus

The bus operates as a source-terminated bus, meaning that the only low-impedance connection to ground is via the source impedance of the drivers in the sender.

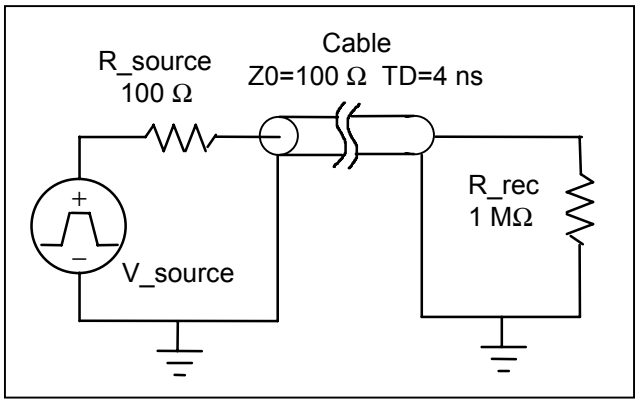


Figure D.1 – A transmission line with perfect source termination

On a source-terminated transmission line, the initial voltage level produced at the source propagates through the system until it reaches the receiving end that, by definition, is an open circuit or at least has high impedance relative to the characteristic impedance of the transmission line. This open circuit produces a reflection of the original step with the same polarity and amplitude as the original step but travelling in the opposite direction. The reflected step adds to the first step to raise the voltage throughout the system to two times the original step voltage. In a perfectly terminated system (see Figure D.1), R_source matches the cable impedance resulting in an initial step voltage on the transmission line equal to fifty percent of V_source and the entire system has reached a steady state at V_source once the reflection returns to the source.

The waveforms that are measured on the bus as a result of this behavior depend on the ratio of the signal rise time to the propagation delay of the system. If the rise time is shorter than the one-way propagation delay, the initial voltage step will be visible at the sender. At the recipient the incoming voltage step is instantaneously doubled as it reflects back to the sender and no step is observed (see Figure D.2).

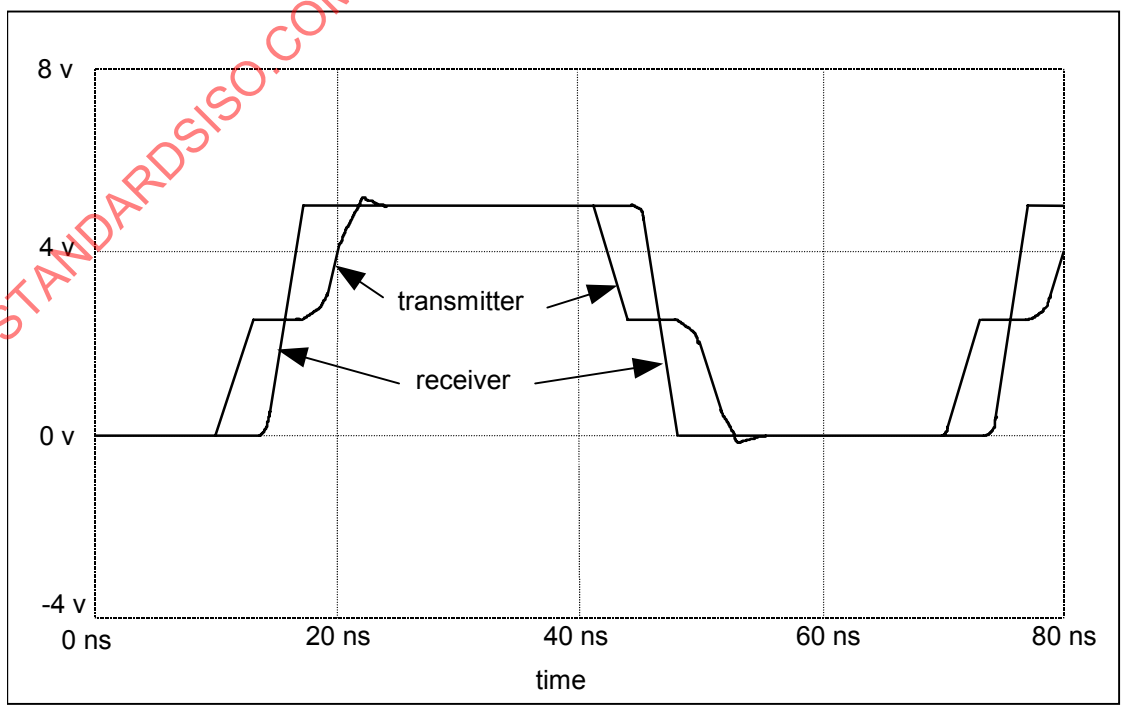


Figure D.2 – Waveforms on a source-terminated bus with rise time less than T_{prop}

If the rise time is longer than the propagation delay, the sender waveform changes, but the same behavior still occurs: the reflected step adds to the initial step at the sender while a delayed doubling of the initial step is observed at the recipient. Because the rising edges of the two steps overlap when measured at the sender, there is a temporary increase in slew rate instead of a step seen at the sender while the rising edge of the reflection adds to the edge still being generated by the sender (see Figure D.3).

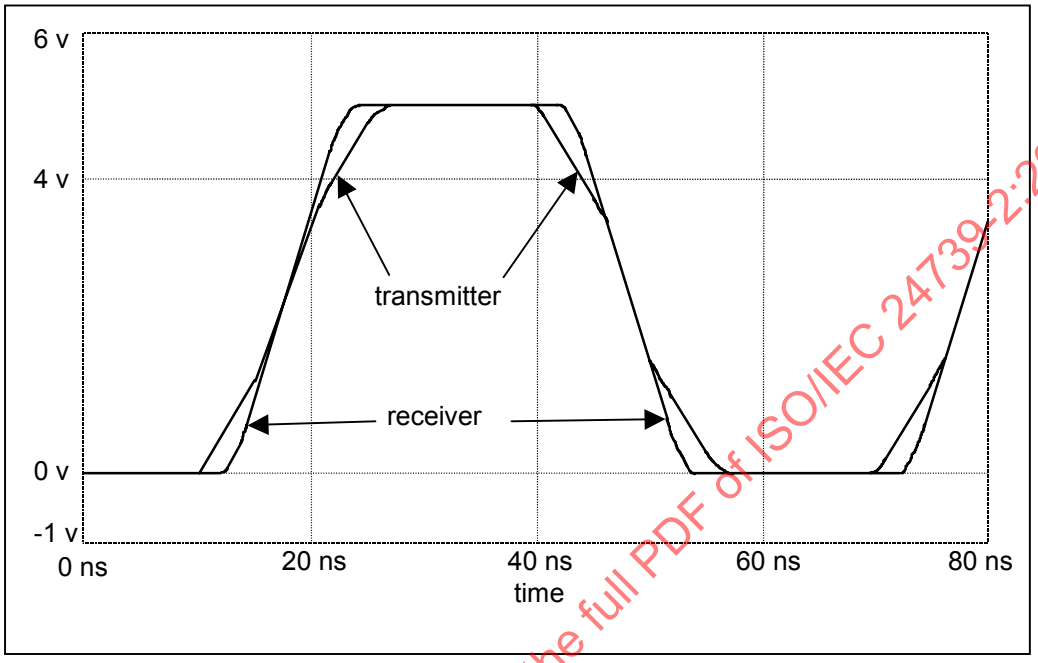


Figure D.3 – Waveforms on a source-terminated bus with rise time greater than T_{prop}

In Figure D.2 and Figure D.3, the source impedance is perfectly matched to the cable impedance with the result that, after the first reflection returns to the source, there are no further reflections and the system is at a steady state. In a system that is not perfectly terminated, there are two possibilities. The first possibility is when the source impedance is less than the characteristic impedance of the transmission line, the initial step is greater than fifty percent of V_{oH} and the system is at a voltage higher than V_{oH} when the first reflection returns to the recipient (see Figure D.4). In this case another reflection occurs at the source to reduce the system to a voltage below V_{oH} but closer to V_{oH} than the initial peak. Reflections continue but are further reduced in amplitude each time they reflect from the termination at the source.

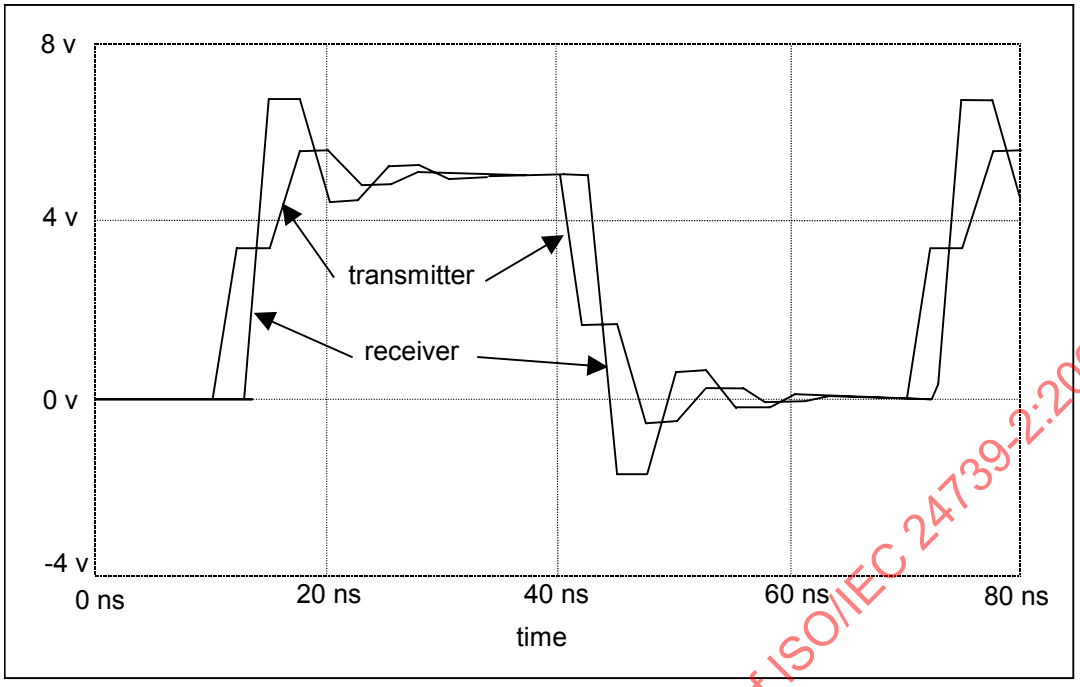


Figure D.4 – Waveforms on a source-terminated bus with R_source less than cable Z_0

The second possibility is when the source impedance is higher than the characteristic impedance, the initial step is less than fifty percent of V_{oH}, and multiple reflections back and forth on the bus will be required to bring the whole system up to a steady state at V_{oH} (see Figure D.5).

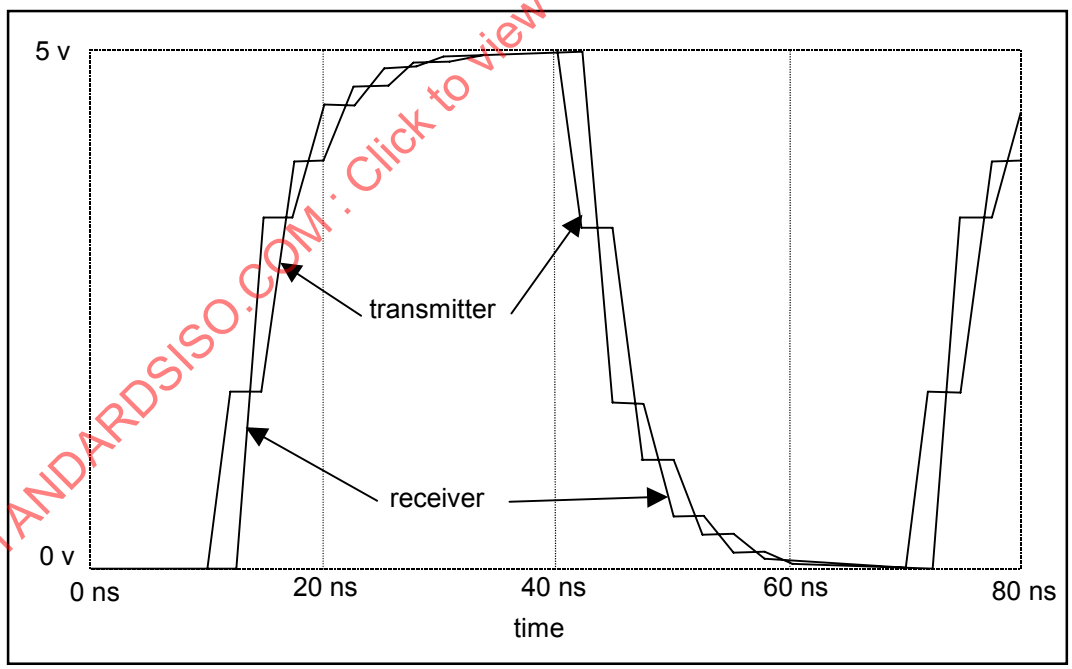


Figure D.5 – Waveforms on a source-terminated bus with R_source greater than cable Z_0

Note that falling edges exhibit the same transmission line behavior as rising edges. The only difference between the edges is that V_{oH} and V_{oL} are reversed. In actual systems output impedance and slew rate of the drivers are often different between rising and falling edges, resulting in different step voltages and waveform shapes.

For typical implementations using a 33 Ω series termination, the effective driving impedance of a sender's component I/O viewed from the cable connector ranges from 50 Ω to 90 Ω. The

component I/O is the combined input and/or output circuitry, bond wire and pin on an IC that is responsible for receiving and/or sending data on a particular conductor within the bus. The initial voltage step produced when an edge is driven onto the cable will be equal to the driver's open-circuit V_{oH} divided by the effective output impedance and the input impedance of the cable (typically 82 Ω) or a 50 Ω to 60 Ω printed circuit board trace in the case of hosts. This step voltage will fall in the range from 50 % to 70 % of V_{oH}. For example, for a theoretical source with zero output impedance using 33 Ω termination driving an 82 Ω cable the resulting step voltage is not greater than 100 × (82 / (33 + 82)) = 71.3 % of V_{oH}. Because the thresholds of an input are not centered with respect to the high and low voltages, the initial voltage step produced by a driver will often cross the recipient's input threshold on a rising edge but not on a falling edge. However, since the signal received at the end of the bus is a doubled version of the initial output from the sender, it will cross the switching thresholds for any reasonably low output impedance. Because of this the main voltage step only affects skew and delay for signals received at devices that are not at the end of the cable. The greater the distance a device is from the device end of the cable (i.e., closer to the host), the longer the duration of the step observed (see Figure D.6 and Figure D.7).

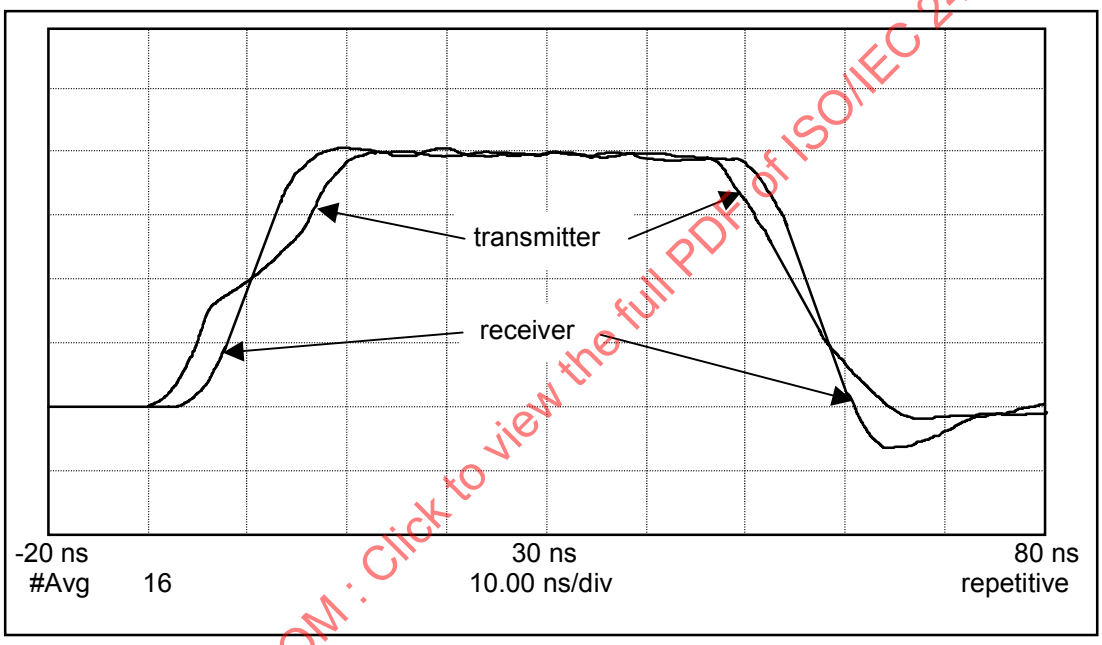


Figure D.6 – Typical step voltage seen in ATA systems using an 80-conductor cable (measured at drive and host connectors during read)

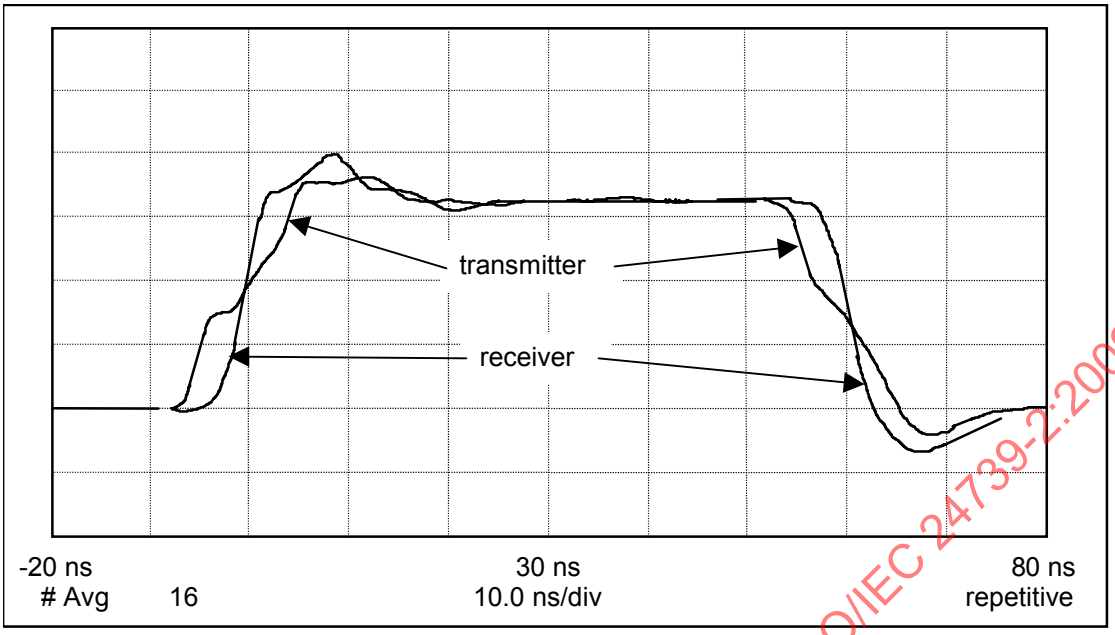


Figure D.7 – Typical step voltage seen in ATA systems using an 80-conductor cable (measured at host and drive connectors during write)

In addition to the step produced by the initial voltage driven onto the bus and the subsequent reflection, smaller steps are produced each time the propagating signal encounters a change in the bus impedance. The major impedance changes that occur in a system are

1) at the connections between the cable and the printed circuit boards (PCBs) of the hosts and devices,
2) along the traces of the PCBs as the result of changing layers and
3) at the connection between a motherboard and a backplane.

The transmission line behavior of the 80-conductor cable assembly adds skew to the received signal in two ways. First, impedance differences along one line versus another will result in different amounts of delay and attenuation on each line due to reflections on the bus. This produces a time difference between the two signals' threshold crossings at the recipient. Secondly, signals received at the device that is not at the end of the cable may cross the threshold during the initial voltage step or after the reflection from the end of the cable is received, depending on the supply voltage, series termination, output impedance, V_{oH} and PCB trace characteristics of the host.

Factors other than cable characteristics also contribute to skew. Differences in the capacitive loading between the STROBE and DATA lines on devices attached to the bus will delay propagating signals by differing amounts. Differences in slew rate or output impedance between drivers when driving the 82 Ω load will result in skew being generated as the signal is sent at the sender. Differences between the input RC delays on STROBE and DATA lines will add skew at the recipient.

The fundamental requirement for minimizing skew in the entire system is to make the STROBE and DATA lines as uniform as possible throughout the system.

D.2.2.5 Timing measurements for the 80-conductor cable assembly

The reflections that are present in a system make it difficult to measure skew and delays accurately. For the received signal at a device, the propagation delay from the device connector to the device integrated circuit (IC) connector pin is about 300 ps for typical device PCBs and trace lengths. The IC is the entire component (die and package) that contains the ATA bus interface circuitry.

This delay introduces an error of plus or minus 300 ps in timing measurements made at the device connector since rising edges and falling edges will be measured before and after the step respectively. When comparing two signals, this results in an error in measured skew of plus or minus 600 ps due to the measurement position. This error is small enough relative to the total timing margin of an Ultra DMA system that it may be ignored in most cases.

Since the trace length on host PCBs are often much longer than those on devices, the propagation time for a signal from the host connector to the host IC may be as high as 2 ns. This results in a plus or minus 2 ns accuracy in the measurement of a single signal and a plus or minus 4 ns accuracy for skew between two signals. These errors are not removed by adding or subtracting an allowance for PCB propagation delay depending on rising or falling edges because characteristics of the PCB and termination will affect the step levels and skew that occur at the component I/Os. As a result of this, accurate measurements of skew in signals received at the host are made either at pins of the host IC or at points on the PCB traces as close to the IC pins as possible. Test pads, headers or unconnected vias in PCB layouts may be designed allowing connection to DATA, STROBE and ground for this purpose.

It is important to note that the timing specifications for Ultra DMA in the standard are based on measuring signals at the interface connector.

D.2.2.6 Simulations for the 80-conductor cable assembly

The difficult nature of measuring skew in actual systems makes simulations a more important tool in determining the effect on skew of design decisions regarding component I/Os, PCB layout, cable lengths and other aspects of system design. Because of the well-controlled impedance of the 80-conductor cable assembly, single line transmission line models provide accurate predictions of the delay through the bus based on a given design choice for a given set of conditions on the bus. To be certain of the system-wide consequences of particular design choices, a large number of simulations encompassing many different combinations of parameters were used to determine the timing specifications for Ultra DMA mode 5. Results of these simulations are also the basis of the guidelines that follow.

Output skew is measured at the connector of the sender into capacitive loads to ground of 15 pF and 40 pF. An alternate loading arrangement is to measure the signal produced at the end of an 18-inch, 80-conductor cable assembly into typical device and host loads of 20 pF or 25 pF that are held uniform across STROBE and DATA lines. Skew is measured at the crossing of the 1.5 V threshold. All combinations of rising and falling edges on the signals involved are used when skew is measured.

Minimizing output skew is the best assurance of reliable signalling across the full range of cable loading and recipient termination conditions that will occur in systems.

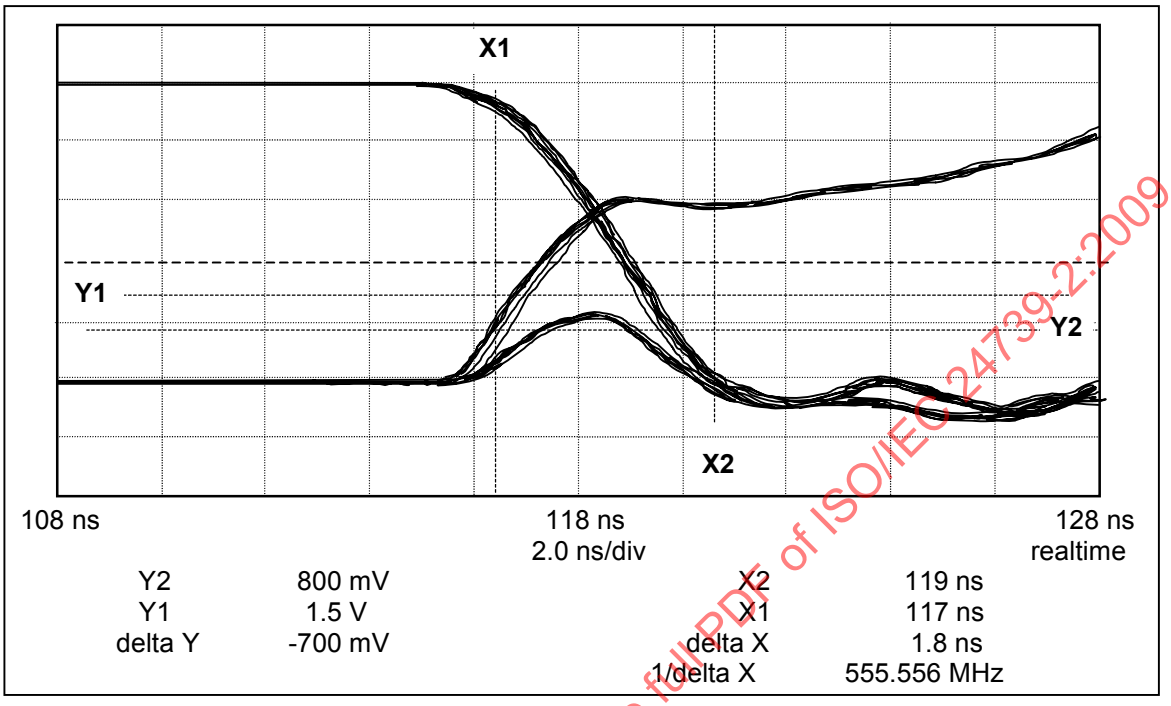
D.2.3 Crosstalk

D.2.3.1 General

Although the ground-signal-ground configuration of the 80-conductor cable assembly greatly reduces coupling between wires on the cable, the host and device connectors generate a large amount of crosstalk because they still use the original ground configuration with no ground lines separating the 16 signals of the data bus. In addition, crosstalk between traces on the PCB may reach high levels in systems with long traces or with tight spacing between traces. Cumulative crosstalk plus ground bounce measured at the connector of the recipient in typical systems using the 80-conductor cable ranges from 400 mV to 1 V peak, in short, pulses with a frequency content equivalent to the frequency content of the edge rates of the drivers being used. Although this level of total crosstalk may seem like a hazard to reliable signaling, crosstalk exceeding 800 mV detected at the recipient does not affect the setup or hold times when it occurs during the interval when other signals are switching (see Figure D.8).

This figure was generated using the first falling STROBE edge for a trigger and showing a middle data signal staying low while all other lines switch high to low. With infinite persistence,

the pattern was then changed to all lines switching low to high for the same STROBE edge. The crosstalk that occurs on the line staying low while all others switch high to low is in excess of 800 mV but has more hold and setup time margin than data lines that are switching and therefore it does not reduce the setup or hold time margin.



NOTE Posivite crosstalk does not affect data setup or hold time.

Figure D.8 – Positive crosstalk pulse during a falling edge

A larger signal integrity hazard exists when crosstalk extends into the middle of the cycle when data could be clocked. This may result from a high level of reverse crosstalk detected at the recipient as the reflected signal propagates from the recipient input back to the sender output in the switching lines, see Figure D.9.

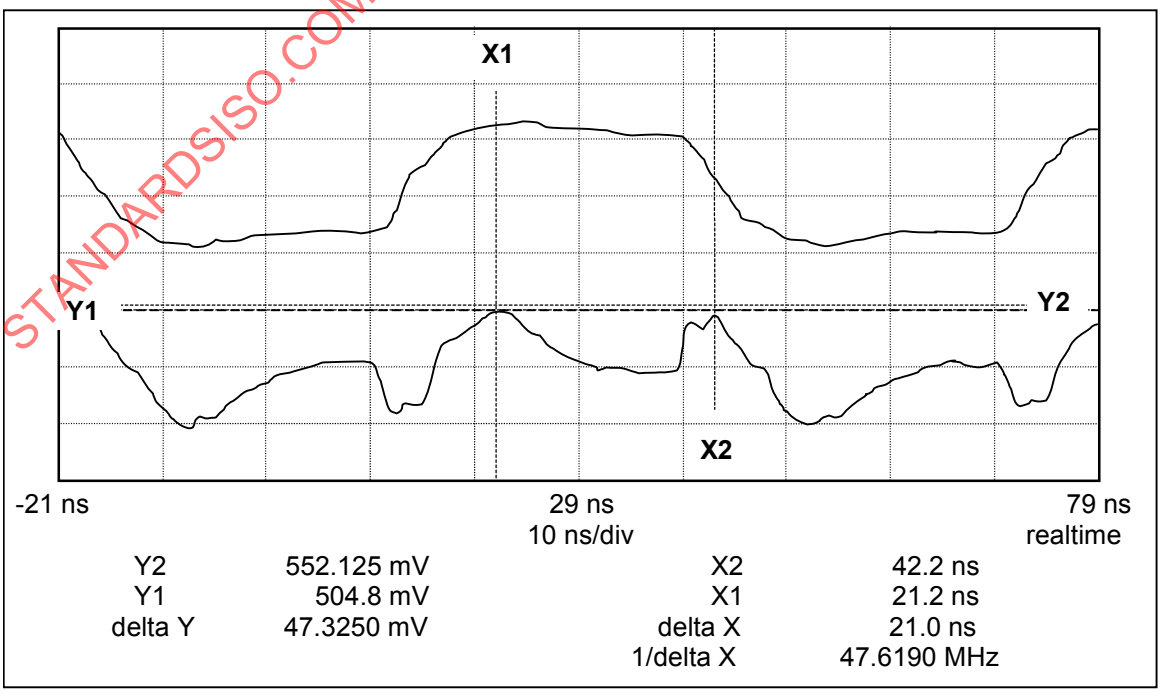


Figure D.9 – Reverse crosstalk waveform from reflected edge

Reducing a system's creation of and susceptibility to forward and reverse crosstalk requires an understanding of how crosstalk is generated and propagates through the system. Crosstalk results from coupling between signals in the form of either a capacitance from one signal conductor to another or inductors in the path of each signal with overlapping magnetic fields. The capacitive and inductive coupling are easiest to understand if treated as separate effects.

D.2.3.2 Capacitive coupling

Capacitive coupling in its simplest form consists of a capacitor connecting together two transmission lines somewhere along their length. When a change in voltage occurs on one line (called the aggressor line), a pulse on the non-switching signal (called the victim line) is produced with a peak amplitude proportional to the rate of change of voltage (d*V*/d*t*) on the aggressor line. The pulse on the victim line propagates both forward and backward from the point of coupling and has the same sign in both directions. Forward and backward are defined relative to the direction that the aggressor signal was propagating. Forward means that the propagation is in the same direction as the aggressor signal. Backward means that propagation is in the opposite direction of the aggressor signal. Figure D.10 is a schematic of a model for capacitive coupling. Figure D.11 shows waveforms resulting from capacitive coupling at the sender and recipient component I/Os of the aggressor and victim lines.

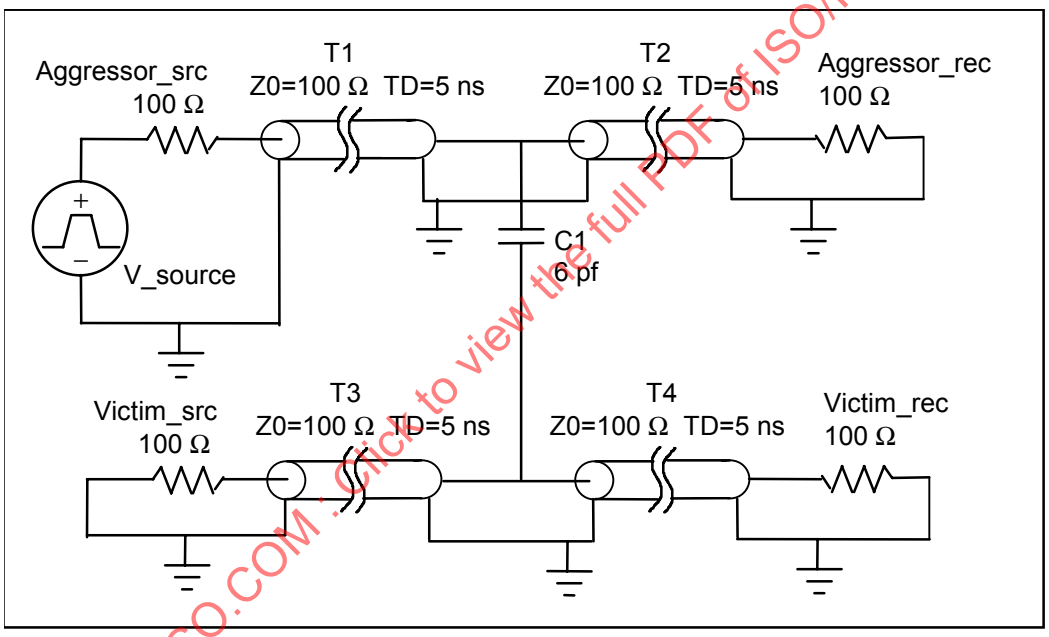


Figure D.10 – Model of capacitive coupling

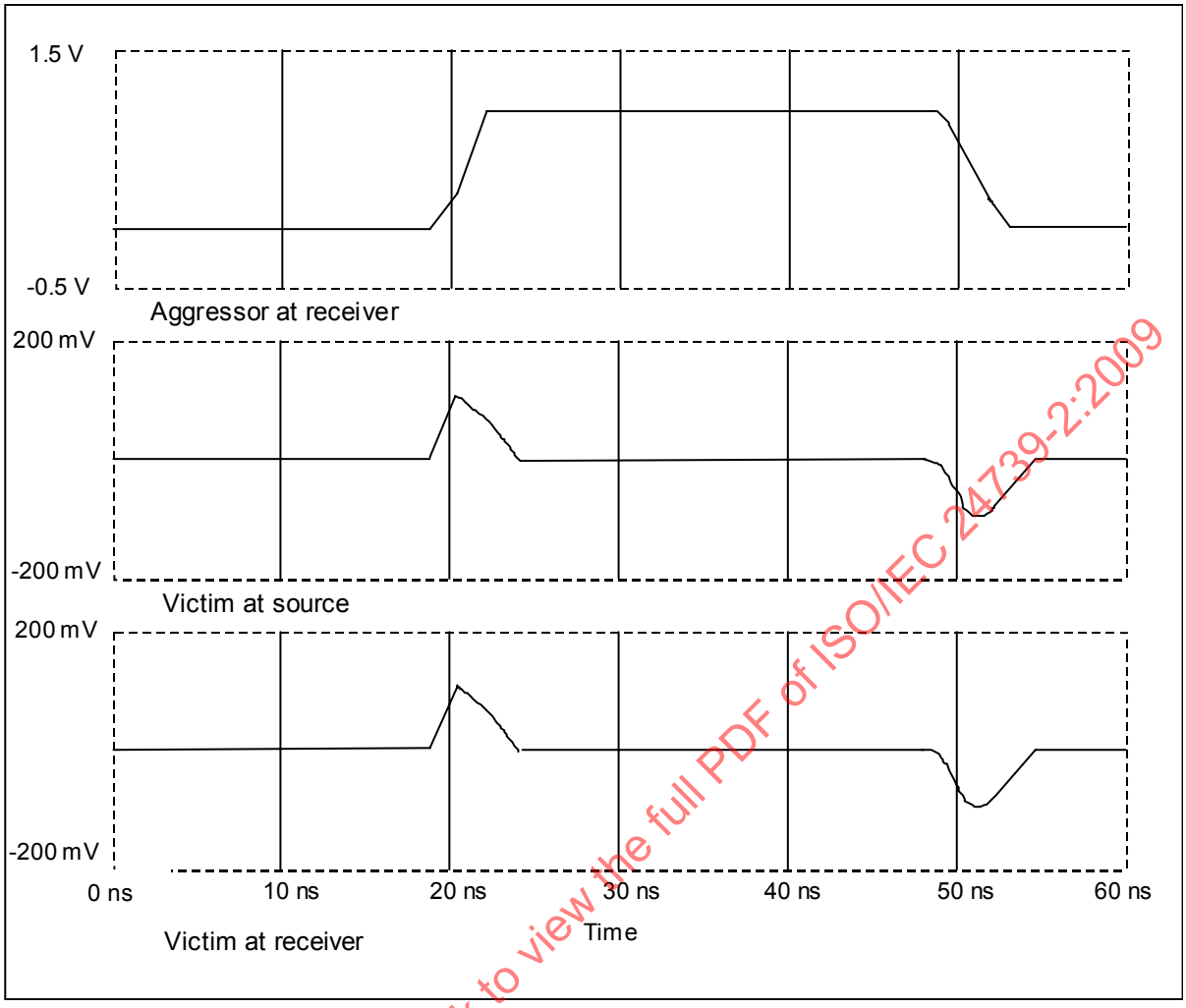


Figure D.11 – Waveforms resulting from capacitive coupling (at transmitter and receiver of aggressor and victim lines)

D.2.3.3 Inductive coupling

In the following, inductive coupling is modelled as an inductor in series with each signal, with some coupling factor K representing the extent to which the inductors' magnetic fields overlap. In effect, these two inductors constitute a transformer, by creating a stepped-down version of the aggressor signal on the victim line. The amplitude of the signal produced on the victim line is proportional to the rate of change in current (d*i*/d*t*) on the aggressor line. Since the impedance of a transmission line is resistive, for points in the middle of a transmission line d*i*/d*t* will be proportional to d*V*/d*t*. Because the crosstalk signal produced across the inductance in the victim line is in series with the transmission line, it has a different sign at each end of the inductor. Because the current in an inductor always opposes the magnetic field that produced it, the polarity of the crosstalk signal is reversed from the polarity of the d*i*/d*t* on the aggressor line that produced it. As a result of these two facts, inductive crosstalk creates a pulse of forward crosstalk with polarity opposite to the edge on the aggressor and a pulse of reverse crosstalk with the same polarity as the aggressor edgeFigure D.12 is a schematic of a model for inductive coupling. Figure D.13 shows waveforms resulting from inductive coupling at the sender and recipient component I/Os of the aggressor and victim lines.

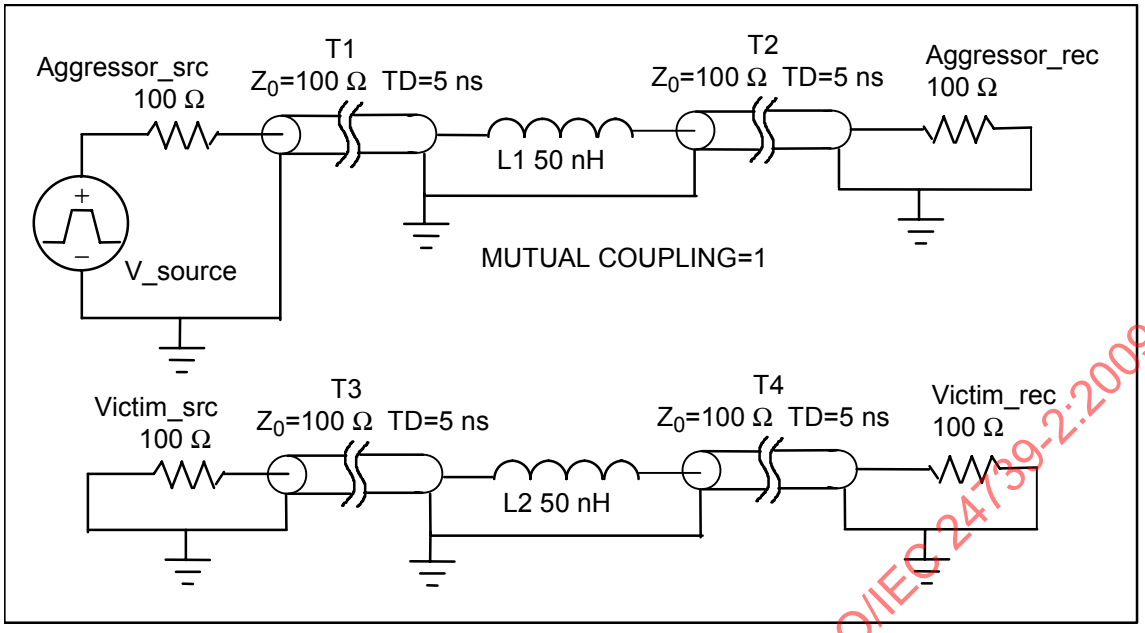


Figure D.12 – Model of inductive coupling

Note that the box in Figure D.12, Figure D.14 and Figure D.18 between L1, L2 and K2 is a PSPICE element representing the inductive coupling between L1 and L2 having the coupling value listed in the respective figures.

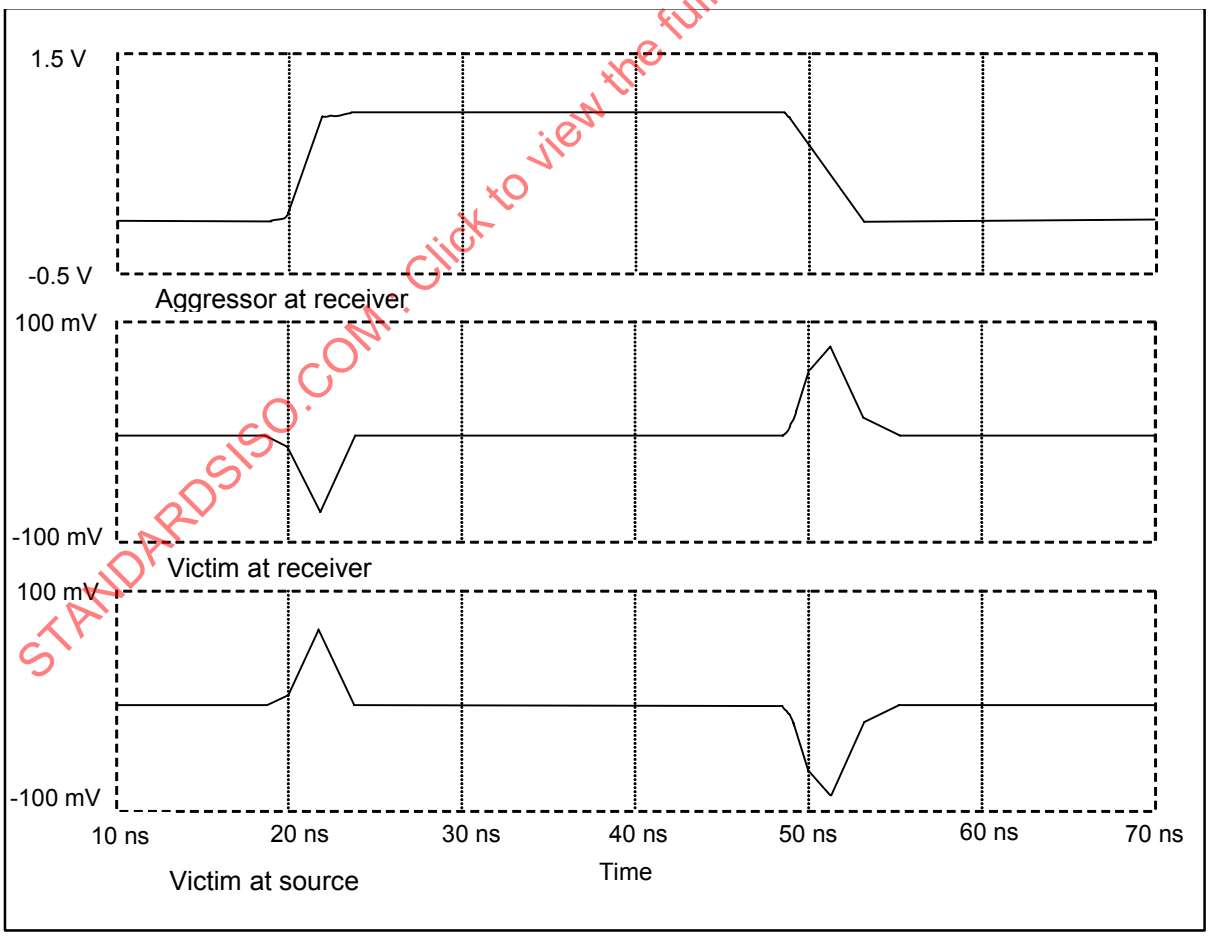


Figure D.13 – Waveforms resulting from inductive coupling (at transmitter and receiver of aggressor and victim lines)

D.2.3.4 Mixed capacitive and inductive coupling

Most occurrences of electromagnetic coupling involve both capacitive and inductive coupling. In this case the forward and reverse crosstalk contributions of the capacitance and inductance add together. Because the forward inductive crosstalk and the forward capacitive crosstalk have opposite signs, they tend to cancel, while the reverse crosstalk from both effects have the same sign and add together. Depending on the ratio of inductive to capacitive coupling, the forward crosstalk may sum to zero when both effects are added together. Figure D.14 is a schematic of a model for mixed capacitive and inductive coupling Figure D.15 shows waveforms resulting from mixed capacitive and inductive coupling at the sender and recipient component I/Os of the aggressor and victim lines.

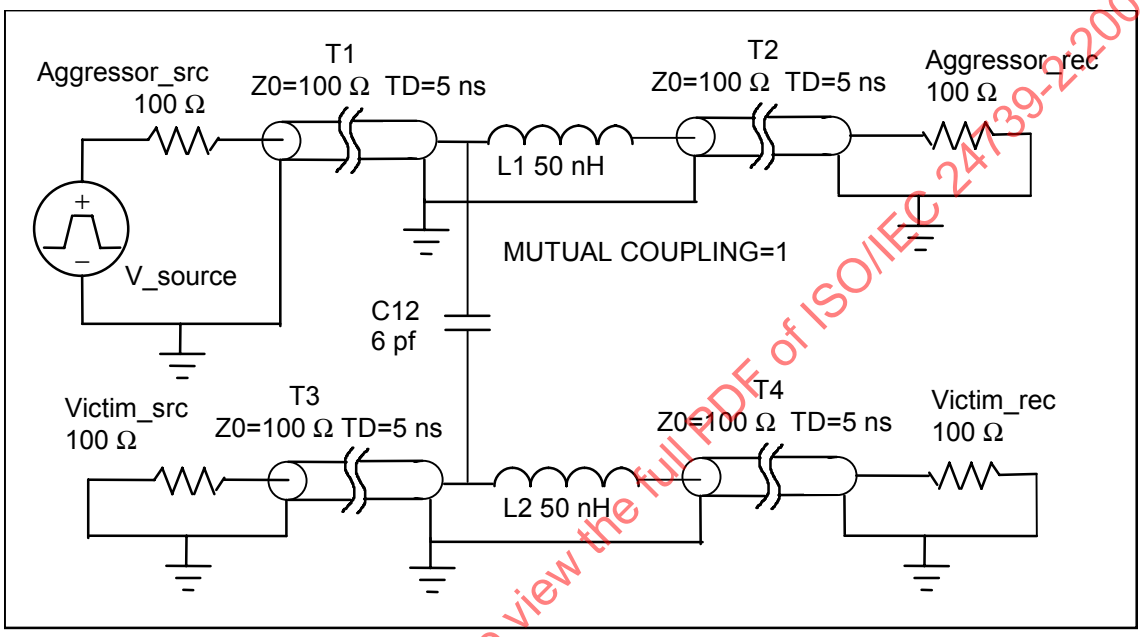


Figure D.14 – Model of capacitive and inductive coupling

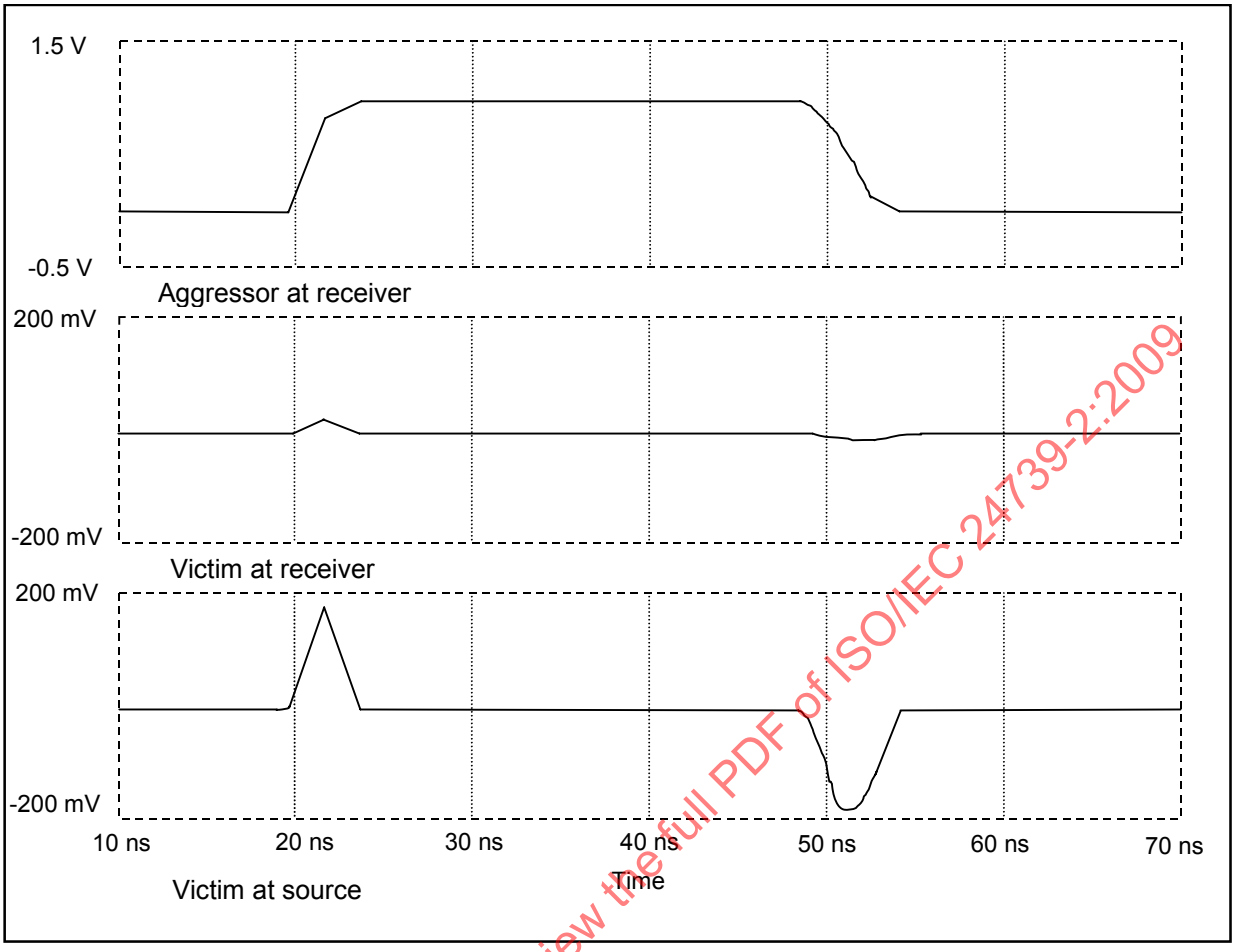


Figure D.15 – Waveforms resulting from mixed capacitive and inductive coupling (at transmitter and receiver of aggressor and victim lines)

D.2.3.5 Crosstalk from distributed coupling

When transmission lines are placed parallel with and in close proximity to, each other, as is the case for PCB traces, wires in a ribbon cable, etc., the coupling that occurs is continuous along the length of the transmission lines. To find the crosstalk waveforms at the source and recipient, divide the transmission lines into segments and treat each segment as an instance of capacitive and inductive coupling. Each segment produces forward and reverse crosstalk as the aggressor edge goes by. Sum the contributions from each of these segments, delaying their arrival at the ends according to the segment's position along the transmission line. This procedure shows that the forward crosstalk contributions all add together and arrive simultaneously with the aggressor edge, while the reverse crosstalk is spread out along the length of the transmission line and produces a long flat pulse travelling back toward the source. Figure D.16 shows a schematic model for a transmission line with three coupled conductors, connected as two signal wires and a ground return. The waveform at the source end of the victim line in Figure D.17 shows that the reverse crosstalk pulse begins when the edge is driven onto the aggressor line and continues to be observed at the source until one system delay after the end of the edge is terminated at the recipient on the aggressor line. The waveform at the victim recipient's component I/O shows that the forward crosstalk arrives simultaneously with the edge on the aggressor line, or even slightly before, because the energy in the crosstalk pulse has been subtracted from the edge on the aggressor, reducing its rise time at the recipient.