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Road vehicles — In-vehicle Ethernet —

Part 5: Optical 1-Gbit/s physical layer system requirements and test plans

Véhicules routiers — Ethernet embarqué —

Partie 5: Exigences et plans de test du système de couche physique à 1-Gbit/s optique

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Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular, the different approval criteria needed for the different types of ISO documents should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO shall not be held responsible for identifying any or all such patent rights. Details of any patent rights identified during the development of the document will be in the Introduction and/or on the ISO list of patent declarations received (see www.iso.org/patents).

Any trade name used in this document is information given for the convenience of users and does not constitute an endorsement.

For an explanation of the voluntary nature of standards, the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT) see www.iso.org/iso/foreword.html.

This document was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

A list of all parts in the ISO 21111 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html.

Introduction

The ISO 21111 series includes in-vehicle Ethernet requirements and test plans that are disseminated in other International Standards and complements them with additional test methods and requirements. The resulting requirement and test plans are structured in different documents following the Open Systems Interconnection (OSI) reference model and grouping the documents that depend on the physical media and bit rate used.

In general, the Ethernet requirements are specified in ISO/IEC/IEEE 8802-3. The ISO 21111 series provides supplemental specifications (e.g. wake-up, I/O functionality), which are required for in-vehicle Ethernet applications. In road vehicles, Ethernet networks are used for different purposes requiring different bit-rates. Currently, the ISO 21111 series specifies the 1-Gbit/s optical and 100-Mbit/s electrical physical layer.

The ISO 21111 series contains requirement specifications and test methods related to the in-vehicle Ethernet. This includes requirement specifications for physical layer entity (e.g. connectors, physical layer implementations) providers, device (e.g. electronic control units, gateway units) suppliers, and system (e.g. network systems) designers. Additionally, there are test methods specified for conformance testing and for interoperability testing.

Safety (electrical safety, protection, fire, etc.) and electromagnetic compatibility (EMC) requirements are out of the scope of the ISO 21111 series.

The structure of the specifications given in the ISO 21111 series complies with the Open Systems Interconnection (OSI) reference model specified in ISO/IEC 7498-1[1] and ISO/IEC 10731[3].

ISO 21111-1 defines the terms which are used in this series of standards and provides an overview of the standards for in-vehicle Ethernet including the complementary relations to ISO/IEC/IEEE 8802-3, the document structure, type of physical entities, in-vehicle Ethernet specific functionalities and so on.

ISO 21111-2 specifies the interface between reconciliation sublayer and physical entity including reduced gigabit media independent interface (RGMII), and the common physical entity wake-up and synchronized link sleep functionalities, independent from physical media and bit rate.

ISO 21111-3 specifies supplemental requirements to a physical layer capable of transmitting 1-Gbit/s over plastic optical fibre compliant with ISO/IEC/IEEE 8802-3, with specific application to communications inside road vehicles, and a test plan for physical entity conformance testing.

ISO 21111-4 specifies the optical components requirements and test methods for 1-Gbit/s optical in-vehicle Ethernet.

This document specifies for 1-Gbit/s optical in-vehicle Ethernet, requirements on the physical layer at system level, requirements on the interoperability test set-ups, the interoperability test plan that checks the requirements for the physical layer at system level, requirements on the device-level physical layer conformance test set-ups, and device-level physical layer conformance test plan that checks a set of requirements for the OSI physical layer that are relevant for device vendors.

ISO 21111-6 specifies advanced features of an ISO/IEC/IEEE 8802-3 in-vehicle Ethernet physical layer (often also called transceiver), e.g. for diagnostic purposes for in-vehicle Ethernet physical layers. It specifies advanced physical layer features, wake-up and sleep features, physical layer test suite, physical layer control requirements and conformance test plan, physical sublayers test suite and physical sublayers requirements and conformance test plan.

ISO 21111-7 specifies the implementation for ISO/IEC/IEEE 8802-3:2017/Amd 1:2017, which defines the interface implementation for automotive applications together with requirements on components used to realize this Bus Interface Network (BIN). ISO 21111-7 also defines further testing and system requirements for systems implemented according to the system specification. In addition, ISO 21111-7 defines the channels for tests of transceivers with a test wiring harness that simulates various electrical communication channels.

ISO 21111-8 specifies the transmission media, the channel performance and the tests for ISO/IEC/IEEE 8802-3 in-vehicle Ethernet.

ISO 21111-9 specifies the data link layer requirements and conformance test plan. It specifies the requirements and test plan for devices and systems with bridge functionality.

ISO 21111-10 specifies the application to network layer requirements and test plan. It specifies the requirements and test plan for devices and systems that include functionality related with OSI layers from 3 to 7.

Figure 1 shows the parts of the ISO 21111 series and the document structure.

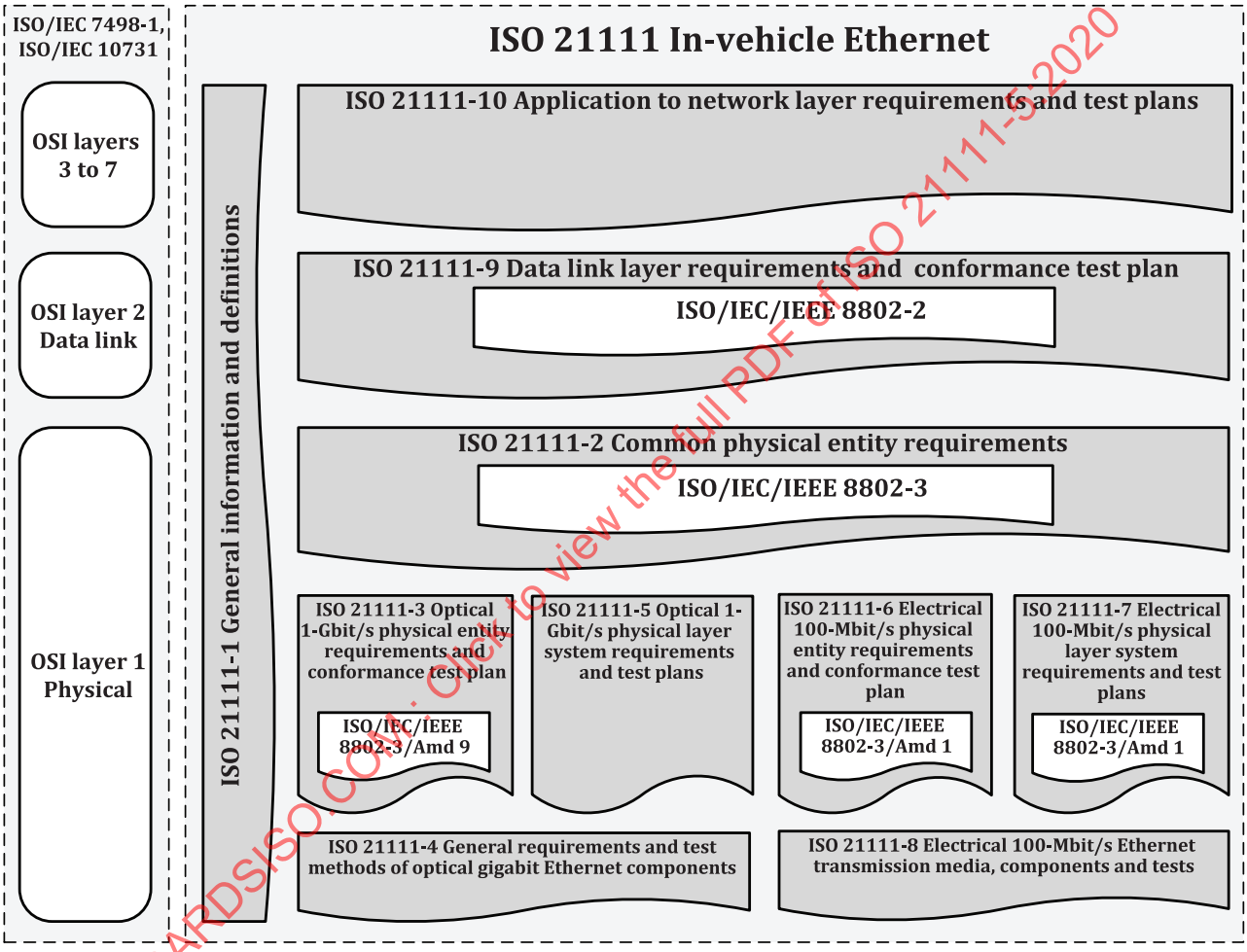


Figure 1 — In-vehicle Ethernet document reference according to OSI model

Road vehicles — In-vehicle Ethernet —

Part 5: Optical 1-Gbit/s physical layer system requirements and test plans

1 Scope

This document specifies:

— requirements on the physical layer at system level,

— requirements on the interoperability test set-ups,

— interoperability test plan that checks the requirements for the physical layer at system level,

— requirements on the device-level physical layer conformance test set-ups, and

— device-level physical layer conformance test plan that checks a set of requirements for the OSI physical layer that are relevant for device vendors.

The interoperability test plan checks the physical layer system requirements specified in this document and in ISO/IEC/IEEE 8802-3:2017/Amd 9.

This test plan is structured in four different test groups, attending to the kind of system requirements that covers:

— link status, that includes the tests that check the status of the link by using the content of the available registers and its accuracy with the real status of the link,

— link-up, that includes the tests that check the time that the IUT reaches a reliable link status from certain state,

— channel quality, that includes the tests that check the quality of the optical channel by using the content of the available registers and its accuracy with the real quality of the optical channel, and

— wake-up and sleep, that include tests that check that the transmission and reception of the wake-up and sleep events.

The device-level conformance test plan checks the device-level requirements specified in the ISO 21111 series and in ISO/IEC/IEEE 8802-3:2017/Amd 9.

This test plan is structured in four different test groups, attending to the test set-up required:

— high-attenuation channel,

— low-attenuation channel,

— optical IUT transmitter measurements, and

— wake-up and synchronised link sleep.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 21111-1[1)], *Road vehicles — In-vehicle Ethernet — Part 1: General information and definitions*

ISO 21111-2[2)], *Road vehicles —In-vehicle Ethernet — Part 2: Common medium-independent interface specifications*

ISO 21111-3, *Road vehicles — In-vehicle Ethernet — Part 3: Optical 1-Gbit/s physical layer specification and conformance test plan*

ISO 21111-4, *Road vehicles — In-vehicle Ethernet — Part 4: Optical 1-Gbit/s component requirements and test methods*

ISO/IEC/IEEE 8802-3, *Standard for Ethernet*

ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, *Physical Layer Specifications and Management Parameters for 1000 Mb/s Operation over Plastic Optical Fiber*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO/IEC/IEEE 8802-3, ISO 21111-1 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at http://www.electropedia.org/

3.1
network system
two or more devices connected bi-directionally through a physical medium

Note 1 to entry: Physical medium is defined in ISO 7498-1:1994.

3.2
GEPOF link status
reliability or unreliability of the bidirectional communication between two GEPOF physical entities as signalled by bit 2 of MDIO register 1.1 specified in ISO/IEC/IEEE 8802-3:2017/Amd 9

3.3
device-level physical layer conformance test plan
set of conformance test cases that covers physical layer requirements relevant for the device provider

3.4
cable plug
POF cable plug that fulfils the specification in ISO 21111-4

3.5
cable socket
POF cable socket that fulfils the specification in ISO 21111-4

1) Under preparation. Stage at the time of publication: ISO/DIS 21111-1:2020.

2) Under preparation. Stage at the time of publication: ISO/DIS 21111-2:2020.

3.6
in-line connector
connector resulting of the match of a *cable plug* (3.4) and a *cable socket* (3.5)

4 Symbols and abbreviated terms

4.1 Symbols

For the purposes of this document, the symbols of ISO 21111-1 and the following apply.

IDD_{device}	device current consumption
IDD_{min}	minimum device current consumption in operation
IDD_{max}	maximum device current consumption in operation
IDD_DIS_{min}	minimum device current consumption in sleep power state
IDD_DIS_{max}	maximum device current consumption in sleep power state
T	climatic chamber temperature
T_{device}	device climatic chamber temperature
T_{LP}	link partner climatic chamber temperature
T_{min}	minimum operating temperature
T_{max}	maximum operating temperature
T_{typ}	typical operating temperature
U	supply voltage
U_{device}	device supply voltage
U_{LP}	link partner supply voltage
U_{min}	minimum supply voltage
U_{max}	maximum supply voltage
U_{typ}	typical supply voltage

4.2 Abbreviated terms

For the purposes of this document, the abbreviated terms of ISO 21111-1 and the following apply.

AOP	average optical power
ER	extinction ratio
GESST	GEPOF entity stress test tool
IUT	implementation under test
LP	link partner
LT	lower tester

POF	plastic optical fibre
RIN	relative intensity noise
RMS	root mean square
TC	test coordinator
UT	upper tester

5 Physical layer system requirements and interoperability test setups requirements

5.1 General

Clause 5 specifies the physical layer system requirements and the interoperability test setup requirements.

The physical layer system requirements are structured by the functionality that they cover:

— The GEPOF link status comprises the physical layer system requirements related with the time and accuracy the network system signals a new status in the GEPOF link (see 5.2),

— The GEPOF link-up time comprises the physical layer system requirements related with the time the network system signals a reliable GEPOF link status from a given initial power state of the two physical entities involved in the GEPOF link (see 5.3),

— The channel quality comprises the physical layer system requirements related with the time and accuracy the network system signals a change of the channel quality in the GEPOF link (see 5.4),

— The communication reliability comprises the physical layer system requirements related with the communication reliability when the devices in the network system are under certain climatic loads and the communication channel is set (see 5.5).

The reference network system used to specify the physical layer system requirements is shown in Figure 2.

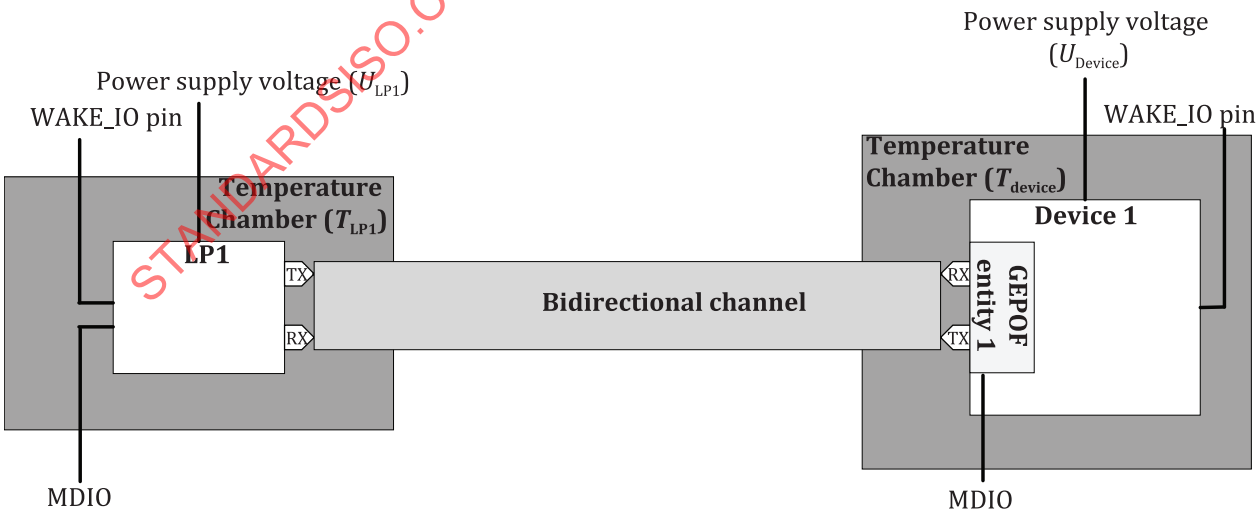


Figure 2 — Reference network system for physical layer system requirements definition

The interoperability test set-ups requirements are specified in 5.6. They include requirements on the channels that are used in the test set-ups and requirements on the device and LP used in the test set-ups.

5.2 GEPOF link status requirements

5.2.1 IOP_GEPOF_REQ_LINK_STATUS_1

REQ	1.1 PHY — IOP_GEPOF_REQ_LINK_STATUS_1
The time measured from the instant when the GEPOF link status changes to "bidirectional reliable link is established" till the reception of the first Ethernet frame in the device shall be lower than 0,5 ms when Ethernet frames are sent continuously from the LP.	

5.2.2 IOP_GEPOF_REQ_LINK_STATUS_2

REQ	1.2 PHY — IOP_GEPOF_REQ_LINK_STATUS_2
The time measured from the instant when the GEPOF link becomes unreliable till the GEPOF link status changes to "bidirectional unreliable link" shall be lower than 5 ms.	

5.3 GEPOF link-up requirements

5.3.1 IOP_GEPOF_REQ_LINK_UP_1

REQ	1.3 PHY — IOP_GEPOF_REQ_LINK_UP_1
The time measured from the instant when the GEPOF entity 1 receives a PHY_WakeUp.request from the data link layer as specified in ISO 21111-2 till the GEPOF link status in GEPOF entity changes to "bidirectional reliable link is established" shall be lower than 100 ms. The initial power state of the GEPOF entity in device 1 and its LP to measure this time shall be Sleep as defined in ISO 21111-2.	

5.3.2 IOP_GEPOF_REQ_LINK_UP_2

REQ	1.4 PHY — IOP_GEPOF_REQ_LINK_UP_2
The time measured from the instant when the GEPOF entity 1 receives a WakeUp_request event as specified in ISO 21111-2 till the GEPOF link status in GEPOF entity 1 changes to "bidirectional reliable link is established" shall be lower than 100 ms. The initial power state of the GEPOF entity 1 to measure this time shall be Sleep as defined in ISO 21111-2. The initial power state of the LP to measure this time shall be Normal as defined in ISO 21111-2.	

5.3.3 IOP_GEPOF_REQ_LINK_UP_3

REQ	1.5 PHY — IOP_GEPOF_REQ_LINK_UP_3
The time measured from the instant when the GEPOF entity 1 is reset till the GEPOF link status in GEPOF entity 1 changes to "bidirectional reliable link is established" shall be lower than 100 ms. The initial power state of the GEPOF entity 1 to measure this time shall be Normal as defined in ISO 21111-2. The initial power state of the LP to measure this time shall be Normal as defined in ISO 21111-2.	

5.3.4 IOP_GEPOF_REQ_LINK_UP_4

REQ	1.6 PHY — IOP_GEPOF_REQ_LINK_UP_4
The time measured from the instant when the LP is reset till the GEPOF link status in GEPOF entity 1 changes to "bidirectional reliable link is established" shall be lower than 100 ms. The initial power state of the GEPOF entity 1 to measure this time shall be Normal as defined in ISO 21111-2. The initial power state of the LP to measure this time shall be Normal as defined in ISO 21111-2.	

5.3.5 IOP_GEPOF_REQ_LINK_UP_5

REQ	1.7 PHY — IOP_GEPOF_REQ_LINK_UP_5
The time measured from the instant when the GEPOF entity 1 receives a WakeUp request event as specified in ISO 21111-2 till the GEPOF link status in GEPOF entity 1 changes to "bidirectional reliable link is established" shall be lower than 100 ms. The initial power state of the GEPOF entity 1 to measure this time shall be Normal as defined in ISO 21111-2. The initial power state of the LP to measure this time shall be Normal as defined in ISO 21111-2.	

5.4 Channel quality requirements

5.4.1 IOP_GEPOF_REQ_CH_QLTY_1

REQ	1.8 PHY — IOP_GEPOF_REQ_CH_QLTY_1
The GEPOF entity 1 shall indicate the channel quality decrease for a channel with decreasing quality.	

5.4.2 IOP_GEPOF_REQ_CH_QLTY_2

REQ	1.9 PHY — IOP_GEPOF_REQ_CH_QLTY_2
The GEPOF entity 1 shall indicate the channel quality increase for a channel with increasing quality.	

5.5 Communication reliability under climatic loads requirements

5.5.1 IOP_GEPOF_REQ_RELIABILITY_TEMP_1

REQ	1.10 PHY — IOP_GEPOF_REQ_RELIABILITY_TEMP_1
The communication between GEPOF entity 1 and its LP shall be reliable as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9 when: — the device that includes the GEPOF entity 1 is located in an oven with temperature set to T_{max}, — the LP is located in an oven with temperature set to T_{min}, and — the communication channel between them is set as bidirectional high attenuation as specified in REQ 1.20 and REQ 1.21.	

5.5.2 IOP_GEPOF_REQ_RELIABILITY_TEMP_2

REQ	1.11 PHY — IOP_GEPOF_REQ_RELIABILITY_TEMP_2
The communication between GEPOF entity 1 and its LP shall be reliable as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9 when: — the device that includes the GEPOF entity 1 is located in an oven with temperature set to T_{min}, — the LP is located in an oven with temperature set to T_{max}, and — the communication channel between them is set as bidirectional high attenuation as specified in REQ 1.20 and REQ 1.21.	

5.5.3 IOP_GEPOF_REQ_RELIABILITY_TEMP_3

REQ	1.12 PHY — IOP_GEPOF_REQ_RELIABILITY_TEMP_3
The communication between GEPOF entity 1 and its LP shall be reliable as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9 when: — the device that includes the GEPOF entity 1 is located in an oven with temperature set to T_{min}, — the LP is located in an oven with temperature set to T_{min}, and — the communication channel between them is set as bidirectional high attenuation as specified in REQ 1.20 and REQ 1.21.	

5.5.4 IOP_GEPOF_REQ_RELIABILITY_TEMP_4

REQ	1.13 PHY — IOP_GEPOF_REQ_RELIABILITY_TEMP_4
The communication between GEPOF entity 1 and its LP shall be reliable as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9 when: — the device that includes the GEPOF entity 1 is located in an oven with temperature set to T_{max}, — the LP is located in an oven with temperature set to T_{max}, and — the communication channel between them is set as bidirectional high attenuation as specified in REQ 1.20 and REQ 1.21.	

5.5.5 IOP_GEPOF_REQ_RELIABILITY_TEMP_5

REQ	1.14 PHY — IOP_GEPOF_REQ_RELIABILITY_TEMP_5
The communication between GEPOF entity 1 and its LP shall be reliable as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9 when: — the device that includes the GEPOF entity 1 is located in an oven with temperature set to T_{max}, — the LP is located in an oven with temperature set to T_{min}, and — the communication channel between them is set as bidirectional low attenuation as specified in REQ 1.22 and REQ 1.23.	

5.5.6 IOP_GEPOF_REQ_RELIABILITY_TEMP_6

REQ	1.15 PHY — IOP_GEPOF_REQ_RELIABILITY_TEMP_6
The communication between GEPOF entity 1 and its LP shall be reliable as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9 when: — the device that includes the GEPOF entity 1 is located in an oven with temperature set to T_{min}, — the LP is located in an oven with temperature set to T_{max}, and — the communication channel between them is set as bidirectional low attenuation as specified in REQ 1.22 and REQ 1.23.	

5.5.7 IOP_GEPOF_REQ_RELIABILITY_TEMP_7

REQ	1.16 PHY — IOP_GEPOF_REQ_RELIABILITY_TEMP_7
The communication between GEPOF entity 1 and its LP shall be reliable as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9 when: — the device that includes the GEPOF entity 1 is located in an oven with temperature set to T_{min}, — the LP is located in an oven with temperature set to T_{min}, and — the communication channel between them is set as bidirectional low attenuation as specified in REQ 1.22 and REQ 1.23.	

5.5.8 IOP_GEPOF_REQ_RELIABILITY_TEMP_8

REQ	1.17 PHY — IOP_GEPOF_REQ_RELIABILITY_TEMP_8
The communication between GEPOF entity 1 and its LP shall be reliable as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9 when: — the device that includes the GEPOF entity 1 is located in an oven with temperature set to T_{max}, — the LP is located in an oven with temperature set to T_{max}, and — the communication channel between them is set as bidirectional low attenuation as specified in REQ 1.22 and REQ 1.23.	

5.5.9 IOP_GEPOF_REQ_RELIABILITY_TEMP_9

REQ	1.18 PHY — IOP_GEPOF_REQ_RELIABILITY_TEMP_9
The communication between GEPOF entity 1 and its LP shall be reliable as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9 when: — the device that includes the GEPOF entity 1 is located in an oven with temperature set to T_{device}, — the LP is located in an oven with temperature set to T_{LP}, — the communication channel between them is set as bidirectional high attenuation as specified in REQ 1.20 and REQ 1.21, — the initial temperature of T_{device} is equal to T_{min} and is increased linearly till it reaches T_{max} in 30 min, and — the initial temperature of T_{LP} is equal to T_{max} and is decreased linearly till it reaches T_{min} in 30 min.	

5.5.10 IOP_GEPOF_REQ_RELIABILITY_TEMP_10

REQ	1.19 PHY — IOP_GEPOF_REQ_RELIABILITY_TEMP_10
The communication between GEPOF entity 1 and its LP shall be reliable as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9 when: — the device that includes the GEPOF entity 1 is located in an oven with temperature set to T_{device}, — the LP is located in an oven with temperature set to T_{LP}, — the communication channel between them is set as bidirectional low attenuation as specified in REQ 1.22 and REQ 1.23, — the initial temperature of T_{device} is equal to T_{min} and is increased linearly till it reaches T_{max} in 30 min, and — the initial temperature of T_{LP} is equal to T_{max} and is decreased linearly till it reaches T_{min} in 30 min.	

5.6 Test set-up requirements

5.6.1 General

5.6 specifies the requirements of the test set-ups that are used in the interoperability test plan.

Most of the test set-ups involve a communication channel between a device and its LP. Different types of communication channels are specified in 5.6 and examples of realization are given.

The requirements on the device and LP for the test set-ups are specified in 5.6.3.

5.6.2 Channel requirements

5.6.2.1 Bidirectional high attenuation channel

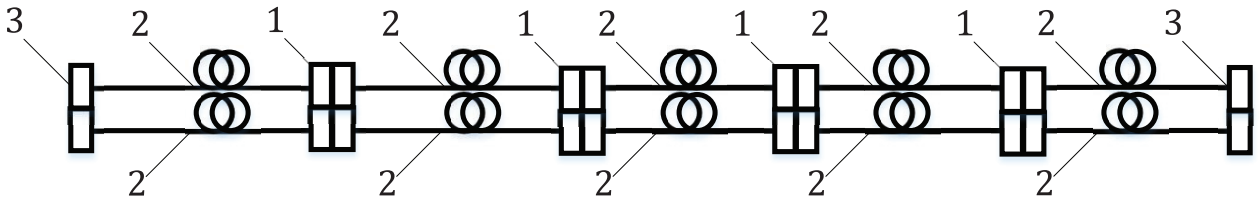
5.6.2.1.1 Bidirectional high attenuation channel requirements

REQ	1.20 PHY — Bidirectional high attenuation channel requirement — Bidirectional channel structure
The bidirectional high attenuation channel type shall be composed of two unidirectional high attenuation channels. Each of the unidirectional high attenuation channels shall comply with REQ 1.21.	

REQ	1.21 PHY — Bidirectional high attenuation channel requirement — Unidirectional channel requirements
The unidirectional high attenuation channel shall have an insertion loss measured at 0 Hz between 6 dB and 7 dB. The normalized frequency response of the unidirectional high attenuation channel shall be between the normalized frequency response specified in ISO/IEC/IEEE 8802-3:2017/Amd 9 for channel type III and 0,2 dB more for the frequency range from 0 MHz to 162,5 MHz. The insertion loss and transfer function requirement shall be fulfilled at (23 ± 2) °C.	

5.6.2.1.2 Example for bidirectional high attenuation channel implementation.

Figure 3 shows an example for a bidirectional high attenuation channel implementation. The simplex POF cable, in-line connector and cable plug fulfil the requirements given in ISO 21111-4. The two-parallel simplex POF cables can be substituted by a single duplex POF cable.



Key

1 in-line connector
2 3-m simplex POF cable
3 cable plug

Figure 3 — Example for bidirectional high attenuation channel implementation

5.6.2.2 Bidirectional low attenuation channel

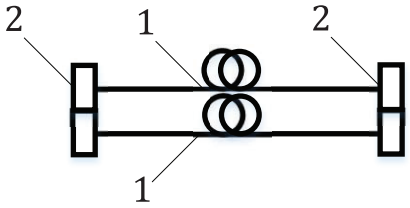
5.6.2.2.1 Bidirectional low attenuation channel requirements

REQ	1.22 PHY — Bidirectional low attenuation channel requirement — Bidirectional channel structure
The bidirectional low attenuation channel type shall be composed of two unidirectional low attenuation channels. Each of the unidirectional low attenuation channels shall comply with REQ 1.23.	

REQ	1.23 PHY — Bidirectional low attenuation channel requirement — Unidirectional channel requirements
The unidirectional low attenuation channel type shall have an insertion loss measured at 0 Hz between 2,5 dB and 3 dB. The lower limit for transfer function magnitude shall be −0,25 dB for the frequency range from 0 Hz to 160 MHz. The upper limit for transfer function magnitude shall be 0 dB for the frequency range from 0 Hz to 160 MHz. The insertion loss and transfer function requirement shall be fulfilled at (23 ± 2) °C.	

5.6.2.2.2 Example for bidirectional low attenuation channel implementation

Figure 4 shows an example for a bidirectional low attenuation channel implementation. The simplex POF cable and cable plug fulfil the requirements given in ISO 21111-4. The two-parallel simplex POF cables can be substituted by a single duplex POF cable.



Key

1 0,5-m simplex POF cable
2 cable plug

Figure 4 — Example for bidirectional low attenuation channel implementation

5.6.2.3 Variable attenuation channel

5.6.2.3.1 Variable attenuation channel requirements

REQ	1.24 PHY — Variable attenuation channel requirements — Bidirectional channel structure
The variable attenuation channel type shall be composed of one unidirectional variable attenuation channel that shall comply with REQ 1.25 and one unidirectional low attenuation channel that shall comply with REQ 1.23. The unidirectional variable attenuation channel shall connect the upper-left and upper-right ports of the variable attenuation channel. The unidirectional low attenuation channel shall connect the lower-left and lower-right ports of the variable attenuation channel.	

REQ	1.25 PHY — Variable attenuation channel requirements — Unidirectional channel requirements
The variable attenuation channel type shall have an insertion loss measured at 0 Hz programmable between 3 dB and 10 dB. The lower limit for transfer function magnitude shall be the requirement specified in ISO/IEC/IEEE 8802-3:2017/Amd 9 for channel type III for the frequency range from 0 Hz to 160 MHz. The upper limit for transfer function magnitude shall be 0 dB for the frequency range from 0 Hz to 160 MHz. The insertion loss and transfer function requirement shall be fulfilled at (23 ± 2) °C and for all the programmable insertion loss measured at 0 Hz.	

5.6.2.3.2 Example for variable attenuation channel implementation

Figure 5 shows an example for a variable attenuation channel implementation. The simplex POF cable and cable plug fulfil the requirements given in ISO 21111-4. Note that the unidirectional variable attenuation channel is implemented only in one communication direction.

5.6.3 Device and LP requirements for interoperability test plan

REQ	1.26 PHY — Device and LP requirements for interoperability test plan — GEPOF entities requirements
Each of the GEPOF entities in the device and LP shall fulfil the requirements in ISO 21111-3 and ISO/IEC/IEEE 8802-3:2017/Amd 9.	

REQ	1.27 PHY — Device and LP requirements for interoperability test plan — MDIO interface
The device and the LP shall include at least one accessible MDIO interface as specified in ISO/IEC/IEEE 8802-3 that allows the individual access to each set of MDIO registers of each GEPOF entity in the device or LP.	

REQ	1.28 PHY — Device and LP requirements for interoperability test plan — Access and control of PHY service interface and neighbour service interface
If the device or the LP implements the wake-up and synchronized link sleep functionality as specified in ISO 21111-3, it shall include a way to access and control PHY service interface and neighbour service interface, as specified in ISO 21111-2.	

REQ	1.29 PHY — Device and LP requirements for interoperability test plan — Ethernet interface
The device and the LP shall include at least one Ethernet physical layer capable of 1 Gbit/s in addition to the one provided by the GEPOF entity.	

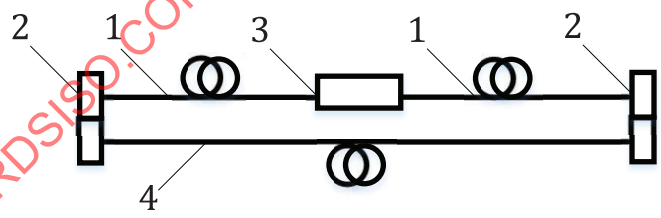
The link status has two possible states:

— "bidirectional reliable link is established" when the MDIO register 1.1 is equal to 1_2, and

— "bidirectional unreliable link" when the MDIO register 1.1 is equal to 0_2.

REQ	1.30 PHY — Device and LP requirements for interoperability test plan — Access to link status
The device shall include constant access to the MDIO register 1.1 that contains the current link status.	

REQ	1.31 PHY — Device and LP requirements for interoperability test plan — PMD_TXPWR.request(tx_pwr) control
The device and the LP shall include a mechanism to control the generation of the request PMD_TXPWR.request(tx_pwr) with a controlled value of the tx_pwr parameter as specified in ISO/IEEE/IEC 8802-3:2017/Amd 9:2018, 115.6.1.3.	



Key

1 0,5-m simplex POF cable
2 cable plug
3 optical variable attenuator
4 1-m simplex POF cable

Figure 5 — Example for variable attenuation channel implementation

6 Interoperability test plan set-ups

6.1 General

The objective of the interoperability test plan is to verify the physical layer system requirements that need a set-up with at least two GEPOF entities. These test set-ups are relevant for the network system designer.

The IUT for this test plan is the complete network system that includes two or more GEPOF physical entities implemented in, at least, one device and its LP. The interoperability test set-up determines the IUT that is used in each test case.

The IUT and the UT are controlled by the TC. The TC implements the functionality of the test coordination procedure specified in ISO/IEC 9646-1.

The IUT has communication with the UT. The UT is able to generate and analyse data from the IUT and check if the result complies with the IUT requirements, as specified in ISO/IEC 9646-1.

Figure 6 shows the relationship between the IUT, the UT and the TC.

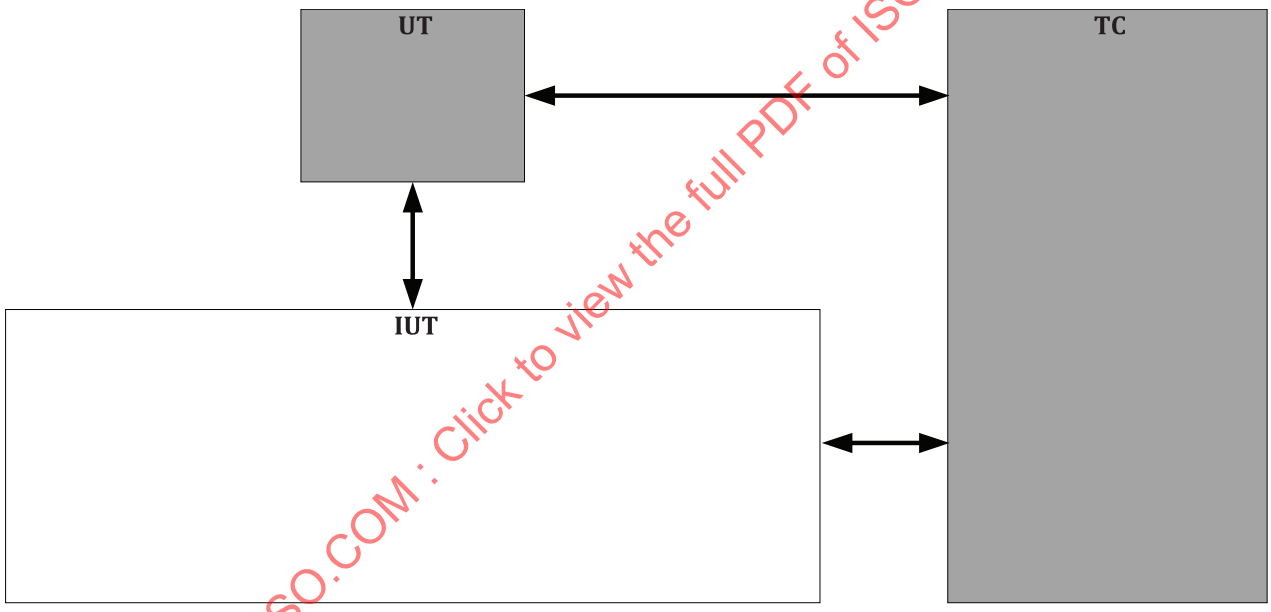


Figure 6 — Interoperability test environment

6.2 Interoperability test set-up 1

The interoperability test set-up 1 is composed of one device and its LP connected by one bidirectional channel that fulfils the requirements for the bidirectional high attenuation channel type specified in 5.6.2.1.

The device is placed inside a temperature chamber set to a controlled temperature T_{device}.

The device is powered by a controlled power supply voltage U_{device}.

The LP is placed inside a temperature chamber set to a controlled temperature T_{LP}.

The LP is powered by a controlled power supply voltage U_{LP}.

The device, LP1 and LP2 may include a wake I/O block connected to a WAKE_IO pin as specified in ISO 21111-2:—, 6.6.

For the test cases that use this test set-up, to power up the device or LP means to set the power_off_ entity variable specified in ISO 21111-2 to FALSE for the GEPOF entity included in the device or LP.

Symmetrically, to power down the device or LP means to set the power_off_entity variable specified in ISO 21111-2 to TRUE for the GEPOF entity included in the device or LP.

REQ	1.32 PHY —Interoperability test plan set-ups — Interoperability test set-up 1
The interoperability test setup 1 shall include the elements and the placement specified in Figure 7.	

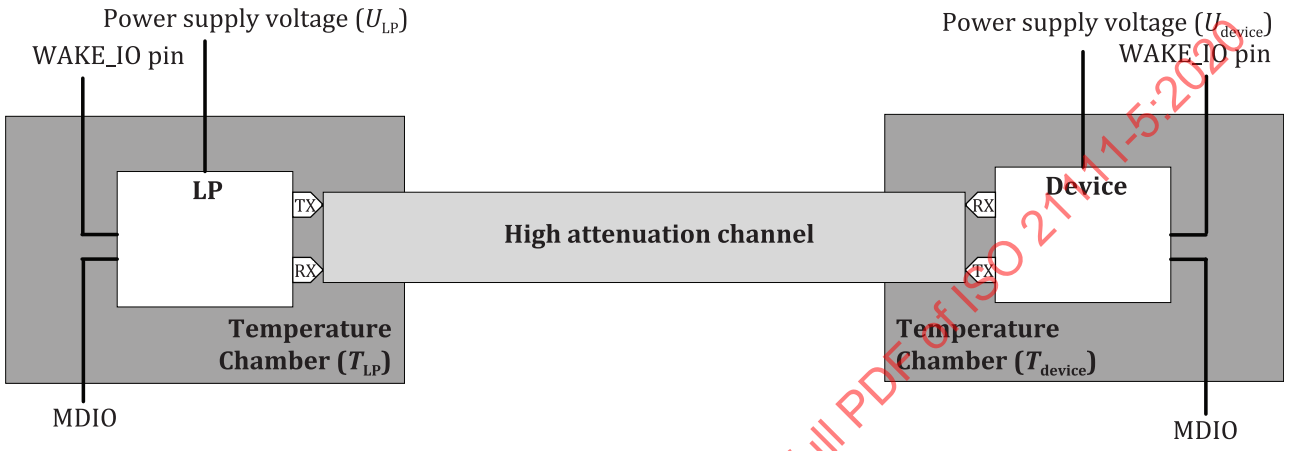


Figure 7 — Interoperability test set-up 1

6.3 Interoperability test set-up 2

The interoperability test set-up 2 is composed by one device and its LP connected by the variable attenuation channel type specified in 5.6.2.3.

The variable attenuation channel implies that the unidirectional channel between the LP transmission and the device reception fulfils REQ 1.25 and that the unidirectional channel between the device transmission and the LP reception fulfils REQ 1.23.

The device is placed inside a temperature chamber set to a controlled temperature T_{device}.

The device is powered by a controlled power supply voltage U_{device}.

The device, LP1 and LP2 may include a wake I/O block connected to a WAKE_IO pin as specified in ISO 21111-2:—, 6.6.

For the test cases that use this test set-up, to power up the device or LP means to set the power_off_ entity variable specified in ISO 21111-2 to FALSE for the GEPOF entity included in the device or LP.

Symmetrically, to power down the device or LP means to set the power_off_entity variable specified in ISO 21111-2 to TRUE for the GEPOF entity included in the device or LP.

The LP is placed inside a temperature chamber set to a controlled temperature T_{LP}.

The LP is powered by a controlled power supply voltage U_{LP}.

REQ	1.33 PHY — Interoperability test plan set-ups — Interoperability test set-up 2
The interoperability test setup 2 shall include the elements and the placement specified in Figure 8.	

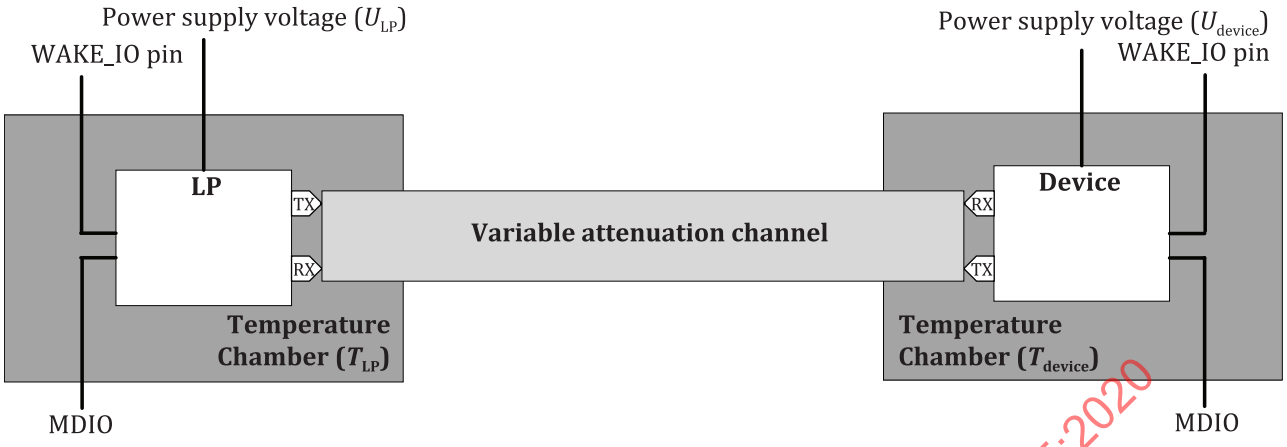


Figure 8 — Interoperability test set-up 2

6.4 Interoperability test set-up 3

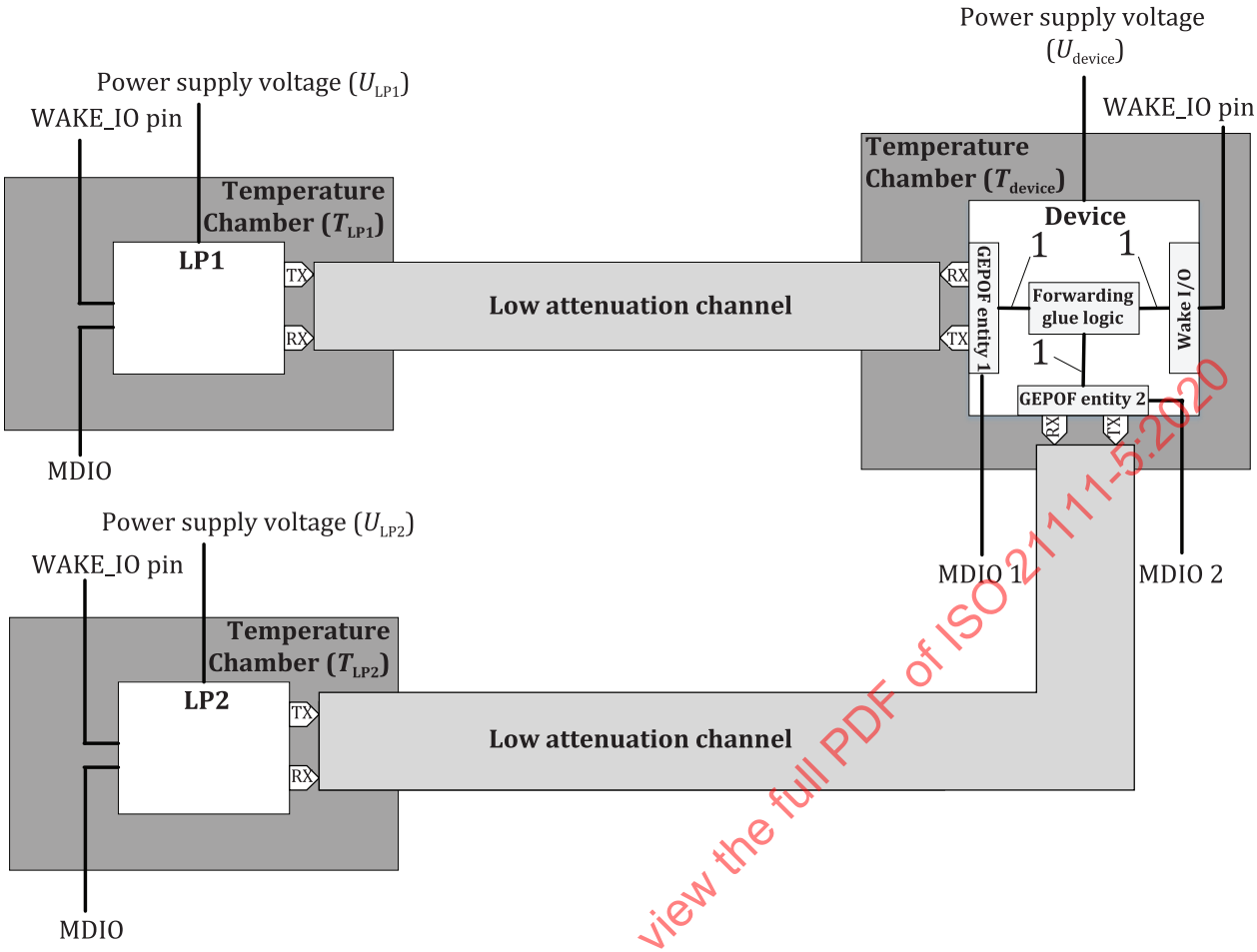
The interoperability test set-up 3 is composed of one device that includes at least two GEPOF entities and two LPs connected each one with each of the two GEPOF entities in the device by means of two bidirectional channels.

The bidirectional channel between each LP and the device fulfils the requirements for the bidirectional low attenuation channel type specified in 5.6.2.2.

The device, LP1 and LP2 may include a wake I/O block connected to a WAKE_IO pin as specified in ISO 21111-2:—, 6.6.

For the test cases that use this test set-up, to power up the device means to set the power_off_entity variable specified in ISO 21111-2 to FALSE for each of the GEPOF entities that are included in the device.

REQ	1.34 PHY — Interoperability test plan set-ups — Interoperability test set-up 3
The interoperability test setup 3 shall include the elements and the placement specified in Figure 9.	



Key

1 NPHY service interface as specified in ISO 21111-2

Figure 9 — Interoperability test set-up 3

6.5 Interoperability test set-up 4

The interoperability test set-up 4 is composed of one device that includes at least two GEPOF entities and two LPs. One LP is connected with one of the two GEPOF entities in the device by means of a bidirectional channel.

The LP1 may include a wake I/O block connected to a WAKE_IO pin as specified in ISO 21111-2:—, 6.6.

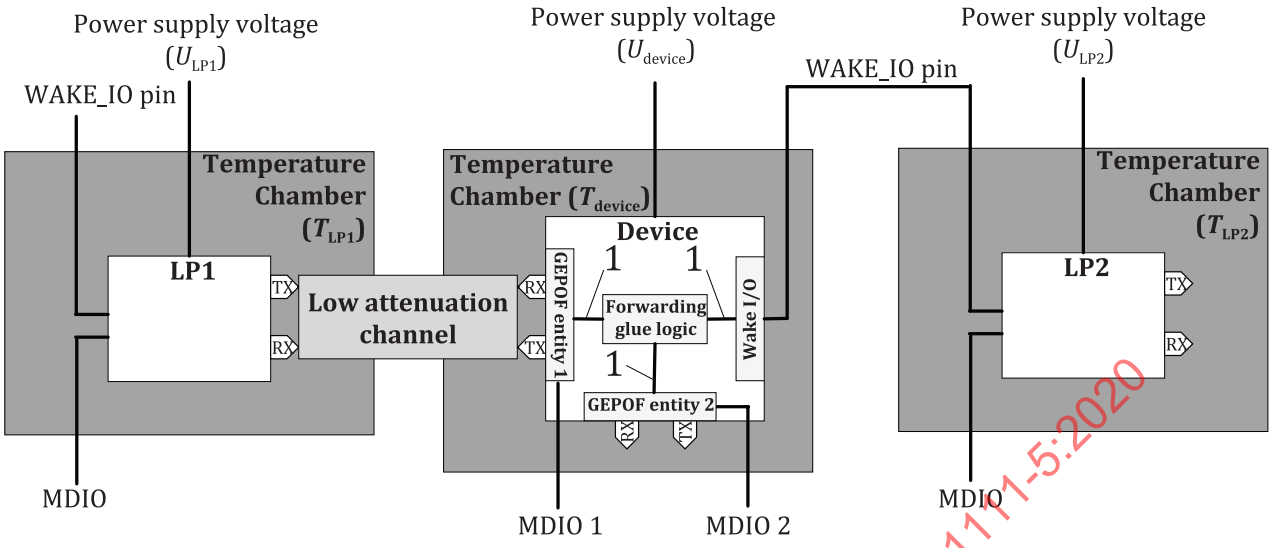
The device and LP2 include a wake I/O block connected to a WAKE_IO pin as specified in ISO 21111-2:—, 6.6.

The bidirectional channel between LP1 and the device fulfils the requirements for the bidirectional low attenuation channel type specified in 5.6.2.2.

The LP2 is connected to the device by means of the WAKE_IO pin specified in ISO 21111-2.

For the test cases that use this test set-up, to power up the device means to set the power_off_entity variable specified in ISO 21111-2 to FALSE for each of the GEPOF entities that are included in the device.

REQ	1.35 PHY — Interoperability test plan set-ups — Interoperability test set-up 4
The interoperability test setup 4 shall include the elements and the placement specified in Figure 10.	



Key

1 NPHY service interface as specified in ISO 21111-2

Figure 10 — Interoperability test set-up 4

7 Interoperability test plan

7.1 General

The interoperability test plan is a set of test cases that checks system network requirements and needs a test set-up with at least one GEPOF entity and its LP. This test plan is relevant for system network designers.

This test plan is structured in test groups. The test cases in the same test group share the same test set-up.

The interoperability test cases, which require variations of individual parameters, shall be repeated for each value of the parameter.

The interoperability test case specifications are intended to provide a high-level description of the motivation, resources, procedures, and methodologies pertinent to each test case. Each interoperability test case is specified according to a common structure as shown in Table 1.

Table 1 — Test case structure

Item	Content
Number – Title	**1 – Test case structure**
Purpose	The purpose is a brief statement outlining what the test case attempts are to achieve. The test case is written at the functional level.
Reference	The purpose of reference is to specify source material external to the test plan, including any other references that might be helpful in understanding the test methodology and/or test case results. External sources are always referenced by number when mentioned in the test case description. Any other references not specified by number are stated with respect to the test plan document itself.
Prerequisite	The purpose of prerequisites is to specify the test case hardware and/or software needed to perform the test case. This is generally expressed in terms of minimum requirements. In some cases, specific equipment manufacturer/model information may be provided.

Table 1 *(continued)*

Item	Content
Set-up	The purpose of set-up is to describe the initial configuration of the test case environment. Small changes in the configuration should not be included here and are generally covered in the test step section below.
Step	The test case steps include the test case description, which contains the systematic instructions for carrying out the test case. It provides a cookbook approach to testing and may be interspersed with observable results. Each test case step shall have a numeric number in ascending order.
Iterations	The purpose of test case iterations is to include test procedure definitions, which are repeated more than once.
Expected response	The purpose of expected response is to describe the expected results to be examined by the test person in order to verify that the test case is operating. When multiple values for an observable are possible, this description provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test case is generally based on the successful (or unsuccessful) detection of a specific observable.
Remark	The purpose of remark is to describe known issues with the test case steps, which can affect test results in certain situations. It can also refer the reader to test plan annexes and/or white papers that can provide more detail regarding these issues.

Some of the test cases refer to different values of the climatic chamber temperature T and different values of the voltage U that is supplied to the device and to the LP.

REQ	**1.36 PHY — Interoperability test plan — Temperature and voltage values**
The typical, minimum, and maximum values T_{typ}, T_{min}, T_{max}, U_{typ}, U_{min}, and U_{max} shall be provided by the test person.	

7.2 High attenuation channel with climatic load

Table 2 specifies the interoperability test case 1.ITC_01_link-up_1_device_sleep for the high attenuation channel specified in 5.6.2.1.

Table 2 — 1.ITC_01_link-up_1_device_sleep — High attenuation channel with climatic load

Item	Content
Number – Title	**1.ITC_01_link-up_1_device_sleep — Link-up time when device is in sleep power state under high attenuation channel**
Purpose	This test case determines the link-up time from reset when the device is in sleep power state in a controlled network system at typical temperature and power supply voltage. The test case verifies that the calculated link up time is lower than 100 ms.
Reference	ISO 21111-3:2020, 6.4, REQ 1.5.
Prerequisites	Device shall provide access to the interfaces specified in 5.6.3.
Set-up	6.2 - Interoperability test set-up 1.

Table 2 *(continued)*

Item	Content
Number – Title	**1.ITC_01_link-up_1_device_sleep — Link-up time when device is in sleep power state under high attenuation channel**
Step	1. The TC shall set the device climatic chamber temperature T_{device} to T_{typ}. 2. The TC shall set the device power supply voltage U_{device} to U_{typ}. 3. The TC shall set the LP climatic chamber temperature T_{LP} to T_{typ}. 4. The TC shall set the LP power supply voltage U_{LP} to U_{typ}. 5. The TC shall power up the LP. 6. The TC shall power up the device. 7. The TC shall wait 100 ms. 8. The UT shall write the device MDIO register bit 15 of the MDIO register 1.0 with 1_2. Then the TC shall reset to zero the T_LINKUP timer and start it. 9. The TC shall wait till the device MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 10. The UT shall get the device link status atleast once each millisecond. 11. When the device link status is equal to "bidirectional reliable link is established", the TC shall stop the T_LINKUP timer. 12. The TC shall check that the value in the T_LINKUP timer is lower than 100 ms.
Iterations	N/A
Expected response	Result of check in step 12 is OK.
Remarks	N/A

Table 3 specifies the interoperability test case 1.ITC_02_link-up_2_LP_sleep for the high attenuation channel specified in 5.6.2.1.

Table 3 — 1.ITC_02_link-up_2_LP_sleep — High attenuation channel with climatic load

Item	Content
Number – Title	**1.ITC_02_link-up_2_LP_sleep — Link-up time when LP is in sleep power state under high attenuation channel**
Purpose	This test case determines the link-up time when the LP is in sleep power state in a controlled network system at typical temperature and power supply voltage. The test case verifies that the calculated link up time is lower than 100 ms.
Reference	ISO 21111-3:2020, 6.4, REQ 1.6.
Prerequisites	Device shall provide access to the interfaces specified in 5.6.3.
Set-up	6.2 - Interoperability test set-up 1.

Table 3 *(continued)*

Item	Content
Number – Title	**1.ITC_02_link-up_2_LP_sleep — Link-up time when LP is in sleep power state under high attenuation channel**
Step	1. The TC shall set the device climatic chamber temperature T_{device} to T_{typ}. 2. The TC shall set the device power supply voltage U_{device} to U_{typ}. 3. The TC shall set the LP climatic chamber temperature T_{LP} to T_{typ}. 4. The TC shall set the LP power supply voltage U_{LP} to U_{typ}. 5. The TC shall power up the LP. 6. The TC shall power up the device. 7. The TC shall wait 100 ms. 8. The UT shall write the device MDIO register bit 15 of the MDIO register 1.0 with 1_2. 9. The TC shall wait till the device MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 10. The UT shall write the LP MDIO register bit 15 of the MDIO register 1.0 with 1_2. Then the TC shall reset to zero the T_LINKUP timer and start it. 11. The TC shall wait till the LP MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 12. The UT shall get the device link status at least once each millisecond. 13. When device link status is equal to "bidirectional reliable link is established", the TC shall stop the T_LINKUP timer. 14. The TC shall check that the value in the T_LINKUP timer is lower than 100 ms.
Iterations	N/A
Expected response	Result of check in step 14 is OK.
Remarks	N/A

Table 5 specifies the interoperability test case 1.ITC_03_temp_1 for the high attenuation channel specified in 5.6.2.1. The iterations for this test case are specified in Table 4.

Table 4 — Required test case conditions T_{device} and T_{LP} for 1.ITC_03_temp_1

Iteration	T_{device}	T_{LP}
1	T_{max}	T_{min}
2	T_{min}	T_{max}
3	T_{min}	T_{min}
4	T_{max}	T_{max}

Table 5 — 1.ITC_03_temp_1 — High attenuation channel with climatic load

Item	Content
Number – Title	**1.ITC_03_temp_1 — System reliability under high attenuation channel and different extreme temperature for device and LP**
Purpose	This test case determines the system reliability when the device and LP are connected by a high attenuation channel. The device is set to a temperature in one extreme of the temperature range specified by the device vendor. Conversely, the LP is set to a temperature in the opposite extreme of the temperature range specified by the LP vendor.

Table 5 *(continued)*

Item	Content
Number – Title	**1.ITC_03_temp_1 — System reliability under high attenuation channel and different extreme temperature for device and LP**
Reference	REQ 1.10, REQ 1.11, REQ 1.12, REQ 1.13.
Prerequisites	Device shall provide access to the interfaces specified in 5.6.3.
Set-up	6.2 - Interoperability test set-up 1.
Step	1. The TC shall set the device climatic chamber temperature T_{device} to the corresponding value for the current iteration. 2. The TC shall set the device power supply voltage U_{device} to U_{typ}. 3. The TC shall set the LP climatic chamber temperature T_{LP} to the corresponding value for the current iteration. 4. The TC shall set the LP power supply voltage U_{LP} to U_{typ}. 5. The TC shall power up the LP. 6. The TC shall power up the device. 7. The TC shall wait 100 ms. 8. The UT shall write the device MDIO register bit 15 to bit 13 of the MDIO register 3.518 with 001_2. 9. The UT shall write the device MDIO register bit 15 of the MDIO register 1.0 with 1_2. 10. The TC shall wait till the device MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 11. The UT shall write the LP MDIO register bit 15 to bit 13 of the MDIO register 3.518 with 001_2. 12. The UT shall write the LP MDIO register bit 15 of the MDIO register 1.0 with 1_2. 13. The TC shall wait till the LP MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 14. The UT shall read bit 15 to bit 0 from the device MDIO register 3.522. 15. The UT shall read bit 15 to bit 0 from the LP MDIO register 3.522. 16. The TC shall wait 15 min. 17. The UT shall read bit 15 to bit 0 from the device MDIO register 3.522. The TC shall check that it is equal to 0000_{16}. 18. The UT shall read bit 15 to bit 0 from the LP MDIO register 3.522. The TC shall check that it is equal to 0000_{16}.
Iterations	Perform iteration with test case conditions T_{device} and T_{LP} specified in Table 4.
Expected response	Result of check in steps 17 and 18 is OK for all iterations.
Remarks	N/A

Table 6 specifies the interoperability test case 1.ITC_04_temp_2 for the high attenuation channel specified in 5.6.2.1.

Table 6 — 1.ITC_04_temp_2 — High attenuation channel with climatic load

Item	Content
Number – Title	**1.ITC_04_temp_2 — System reliability under high attenuation channel and changing temperature for device and LP**
Purpose	This test case determines the system reliability when the device and LP are connected by a high attenuation channel and the temperature in the device and in the LP is changing in the range of temperatures specified by the LP vendor.
Reference	REQ 1.18.
Prerequisites	Device shall provide access to the interfaces specified in 5.6.3.
Set-up	6.2 - Interoperability test set-up 1.
Step	1. The TC shall set the device climatic chamber temperature T_{device} to the corresponding value for the current iteration. 2. The TC shall set the device power supply voltage U_{device} to U_{typ}. 3. The TC shall set the LP climatic chamber temperature T_{LP} to T_{max}. 4. The TC shall set the LP power supply voltage U_{LP} to U_{typ}. 5. The TC shall power up the LP. 6. The TC shall power up the device. 7. The TC shall wait 100 ms. 8. The UT shall write the device MDIO register bit 15 to bit 13 of the MDIO register 3.518 with 001_2. 9. The UT shall write the device MDIO register bit 15 of the MDIO register 1.0 with 1_2. 10. The TC shall wait till the device MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 11. The UT shall write the LP MDIO register bit 15 to bit 13 of the MDIO register 3.518 with 001_2. 12. The UT shall write the LP MDIO register bit 15 of the MDIO register 1.0 with 1_2. 13. The TC shall wait till the LP MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 14. The UT shall read bit 15 to bit 0 from the device MDIO register 3.522. 15. The UT shall read bit 15 to bit 0 from the LP MDIO register 3.522. 16. The TC shall set the device climatic chamber temperature to increase from T_{min} to T_{max} in 30 min. 17. The TC shall set the LP climatic chamber temperature to decrease from T_{max} to T_{min} in 30 min. 18. The TC shall wait 30 min. 19. The UT shall read bit 15 to bit 0 from the device MDIO register 3.522. The TC shall check that it is equal to 0000_{16}. 20. The UT shall read bit 15 to bit 0 from the LP MDIO register 3.522. The TC shall check that it is equal to 0000_{16}.
Iterations	Perform iteration with test case conditions T_{device} and T_{LP} specified in Table 4.
Expected response	Result of check in steps 19 and 20 is OK for all iterations.
Remarks	N/A

7.3 Low attenuation channel with climatic load

Table 8 specifies the interoperability test case 1.ITC_05_temp_3 for the low attenuation channel specified in 5.6.2.2. The iterations for this test case are specified in Table 7.

Table 7 — Required test case conditions T_{device} and T_{LP} for 1.ITC_05_temp_3

Iteration	T_{device}	T_{LP}
1	T_{max}	T_{min}
2	T_{min}	T_{max}
3	T_{min}	T_{min}
4	T_{max}	T_{max}

Table 8 — 1.ITC_05_temp_3 — Low attenuation channel with climatic load

Item	Content
Number – Title	**1.ITC_05_temp_3 — System reliability under low attenuation channel and different extreme temperature for device and LP**
Purpose	This test case determines the system reliability when the device and LP are connected by a low attenuation channel and the temperature in the device is in one extreme of the range of temperatures specified by the device vendor and the LP is in the opposite extreme of the range of temperatures specified by the LP vendor.
Reference	REQ 1.14, REQ 1.15, REQ 1.16, REQ 1.17.
Prerequisites	Device shall provide access to the interfaces specified in 5.6.3.
Set-up	6.3 - Interoperability test set-up 2.
Step	1. The TC shall set the device climatic chamber temperature T_{device} to the corresponding value for the current iteration. 2. The TC shall set the device power supply voltage U_{device} to U_{typ}. 3. The TC shall set the LP climatic chamber temperature T_{LP} to the corresponding value for the current iteration. 4. The TC shall set the LP power supply voltage U_{LP} to U_{typ}. 5. The TC shall power up the LP. 6. The TC shall power up the device. 7. The TC shall wait 100 ms. 8. The UT shall write the device MDIO register bit 15 to bit 13 of the MDIO register 3.518 with 001_2. 9. The UT shall write the device MDIO register bit 15 of the MDIO register 1.0 with 1_2. 10. The TC shall wait till the device MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 11. The UT shall write the LP MDIO register bit 15 to bit 13 of the MDIO register 3.518 with 001_2. 12. The UT shall write the LP MDIO register bit 15 of the MDIO register 1.0 with 1_2. 13. The TC shall wait till the LP MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 14. The UT shall read bit 15 to bit 0 from the device MDIO register 3.522. 15. The UT shall read bit 15 to bit 0 from the LP MDIO register 3.522. 16. The TC shall wait 15 min.

Table 8 *(continued)*

Item	Content
Number – Title	**1.ITC_05_temp_3 — System reliability under low attenuation channel and different extreme temperature for device and LP**
	17. The UT shall read bit 15 to bit 0 from the device MDIO register 3.522. The TC shall check that it is equal to 0000_{16}. 18. The UT shall read bit 15 to bit 0 from the LP MDIO register 3.522. The TC shall check that it is equal to 0000_{16}.
Iterations	Perform iteration with test case conditions T_{device} and T_{LP} specified in Table 7.
Expected response	Result of check in steps 17 and 18 is OK for all iterations.
Remarks	N/A

Table 9 specifies the interoperability test case 1.ITC_06_temp_4 for the low attenuation channel specified in 5.6.2.2.

Table 9 — 1.ITC_06_temp_4 — Low attenuation channel with climatic load

Item	Content
Number – Title	**1.ITC_06_temp_4 — System reliability under low attenuation channel and changing temperature for device and LP**
Purpose	This test case determines the system reliability when the device and LP are connected by a low attenuation channel and the temperature in the device and in the LP is changing in the range of temperatures specified by the LP vendor.
Reference	REQ 1.19.
Prerequisites	Device shall provide access to the interfaces specified in 5.6.3.
Set-up	6.3 - Interoperability test set-up 2.
Step	1. The TC shall set the device climatic chamber temperature T_{device} to T_{min}. 2. The TC shall set the device power supply voltage U_{device} to U_{typ}. 3. The TC shall set the LP climatic chamber temperature T_{LP} to T_{max}. 4. The TC shall set the LP power supply voltage U_{LP} to U_{typ}. 5. The TC shall power up the LP. 6. The TC shall power up the device. 7. The TC shall wait 100 ms. 8. The UT shall write the device MDIO register bit 15 to bit 13 of the MDIO register 3.518 with 001_2. 9. The UT shall write the device MDIO register bit 15 of the MDIO register 1.0 with 1_2. 10. The TC shall wait till the device MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 11. The UT shall write the LP MDIO register bit 15 to bit 13 of the MDIO register 3.518 with 001_2. 12. The UT shall write the LP MDIO register bit 15 of the MDIO register 1.0 with 1_2. 13. The TC shall wait till the LP MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

Table 9 *(continued)*

Item	Content
Number – Title	**1.ITC_06_temp_4 — System reliability under low attenuation channel and changing temperature for device and LP**
	14. The UT shall read bit 15 to bit 0 from the device MDIO register 3.522. 15. The UT shall read bit 15 to bit 0 from the LP MDIO register 3.522. 16. The TC shall set the device climatic chamber temperature to increase from T_{min} to T_{max} in 30 min. 17. The TC shall set the LP climatic chamber temperature to decrease from T_{max} to T_{min} in 30 min. 18. The TC shall wait 30 min. 19. The UT shall read bit 15 to bit 0 from the device MDIO register 3.522. The TC shall check that it is equal to 0000_{16}. 20. The UT shall read bit 15 to bit 0 from the LP MDIO register 3.522. The TC shall check that it is equal to 0000_{16}.
Iterations	N/A
Expected response	Result of check in steps 19 and 20 is OK.
Remarks	N/A

7.4 Link status time

Table 10 specifies the interoperability test case 1.ITC_07_link_status_rx_Eth for the high attenuation channel specified in 5.6.2.1.

Table 10 — 1.ITC_07_link_status_rx_Eth — Link status time

Item	Content
Number – Title	**1.ITC_07_link_status_rx_Eth — Time from link status to first Ethernet frame reception under high attenuation channel**
Purpose	This test case determines the time from the link status changes to "bidirectional reliable link is established" to the reception of the first Ethernet frame.
Reference	REQ 1.1.
Prerequisites	Device shall provide access to the interfaces specified in 5.6.3.
Set-up	6.2 - Interoperability test set-up 1.
Step	1. The TC shall set the device climatic chamber temperature T_{device} to T_{typ}. 2. The TC shall set the device power supply voltage U_{device} to U_{typ}. 3. The TC shall set the LP climatic chamber temperature T_{LP} to T_{typ}. 4. The TC shall set the LP power supply voltage U_{LP} to U_{typ}. 5. The TC shall power up the LP. 6. The TC shall power up the device. 7. The TC shall wait 100 ms.

Table 10 *(continued)*

Item	Content
Number – Title	**1.ITC_07_link_status_rx_Eth — Time from link status to first Ethernet frame reception under high attenuation channel**
	8. The UT shall set the IUT to transmit continuously valid Ethernet frames with 64 bytes length from LP to device. The inter frame gap is set to the minimum. 9. The UT shall write the device MDIO register bit 15 of the MDIO register 1.0 with 1_2. 10. The TC shall wait till the device MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 11. The UT shall write the LP MDIO register bit 15 of the MDIO register 1.0 with 1_2. 12. The TC shall wait till the LP MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 13. The TC shall wait till the device link status is equal to "bidirectional reliable link is established". 14. The TC shall check that the device receives correctly the Ethernet frames. 15. The UT shall write the device MDIO register bit 15 of the MDIO register 1.0 with 1_2. 16. The TC shall wait till the device MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 17. When the device link status is equal to "bidirectional reliable link is established", the TC shall start the T_LINKSTATUS timer. 18. When the device receives the first correct Ethernet frame, the TC shall stop the T_LINKSATUS timer. 19. The TC shall check that the value in the T_LINKSTATUS timer is lower than 0,5 ms.
Iterations	N/A
Expected response	Result of check in steps 14 and 19 is OK.
Remarks	N/A

Table 11 specifies the interoperability test case 1.ITC_08_link_status_unreliable for the high attenuation channel specified in 5.6.2.1.

Table 11 — 1.ITC_08_link_status_unreliable — Link status time

Item	Content
Number – Title	**1.ITC_08_link_status_unreliable — Time from unreliable link to link status equal to "bidirectional link unreliable"**
Purpose	This test case determines the time from physically unreliable link to link status changes to "bidirectional link unreliable".
Reference	REQ 1.2.
Prerequisites	Device shall provide access to the interfaces specified in 5.6.3.
Set-up	6.2 - Interoperability test set-up 1.
Step	1. The TC shall set the device climatic chamber temperature T_{device} to T_{typ}. 2. The TC shall set the device power supply voltage U_{device} to U_{typ}. 3. The TC shall set the LP climatic chamber temperature T_{LP} to T_{typ}. 4. The TC shall set the LP power supply voltage U_{LP} to U_{typ}. 5. The TC shall power up the LP. 6. The TC shall power up the device. 7. The TC shall wait 100 ms. 8. The UT shall write the device MDIO register bit 12 to bit 10 of the MDIO register 3.518 with 001_2. 9. The UT shall write the device MDIO register bit 15 of the MDIO register 1.0 with 1_2. 10. The TC shall wait till the device MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 11. The UT shall write the LP MDIO register bit 12 to bit 10 of the MDIO register 3.518 with 001_2. 12. The UT shall write the LP MDIO register bit 15 of the MDIO register 1.0 with 1_2. 13. The TC shall wait till the LP MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 14. The TC shall wait till the device link status is equal to "bidirectional reliable link is established". 15. The TC shall disable the optical transmission in the LP. Then the TC shall reset to zero the T_LINKUP timer and start it. 16. The UT shall get the device link status at least once each millisecond. 17. When the device link status is equal to "bidirectional unreliable link", the TC shall stop the T_LINKUP timer. 18. The TC shall check that the value in the T_LINKUP timer is lower than 5 ms.
Iterations	N/A
Expected response	Result of check in step 18 is OK.
Remarks	N/A

7.5 Channel quality

Table 12 specifies the interoperability test case 1.ITC_09_decrease_ch_quality for the variable attenuation channel specified in 5.6.2.3.

Table 12 — 1.ITC_09_decrease_ch_quality — Channel quality

Item	Content
Number – Title	**1.ITC_09_decrease_ch_quality — Decrease channel quality measurement**
Purpose	This test case determines that if the channel decreases its quality, then the reported quality also decreases.
Reference	REQ 1.8.
Prerequisites	Device shall provide access to the interfaces specified in 5.6.3.
Set-up	6.3 - Interoperability test set-up 2.
Step	1. The TC shall set the device climatic chamber temperature T_{device} to T_{typ}. 2. The TC shall set the device power supply voltage U_{device} to U_{typ}. 3. The TC shall set the LP climatic chamber temperature T_{LP} to T_{typ}. 4. The TC shall set the LP power supply voltage U_{LP} to U_{typ}. 5. The TC shall power up the LP. 6. The TC shall power up the device. 7. The TC shall set MINMARGIN to zero. 8. The TC shall set MAXMARGIN to zero. 9. The TC shall set channel attenuation to 3 dB. 10. The TC shall wait 100 ms. 11. The TC shall wait till the device link status is equal to "bidirectional reliable link is established". 12. The UT shall read bit 7 to bit 0 from the device MDIO register 3.520 and store it into LINKMARGIN variable. 13. If LINKMARGIN is lower than the current value of MINMARGIN, then the TC shall store LINKMARGIN into MINMARGIN. 14. If LINKMARGIN is greater than the current value of MAXMARGIN, then the TC shall store LINKMARGIN into MAXMARGIN. 15. The TC shall repeat 100 times the steps 10 to 14. 16. The TC shall set MIDMARGIN to MAXMARGIN/2 + MINMARGIN/2. 17. The TC shall set MIDMARGIN_HIGH to MIDMARGIN. 18. The TC shall increase channel attenuation in 1 dB. 19. The TC shall repeat steps 12 to 16.

Table 12 *(continued)*

Item	Content
Number – Title	**1.ITC_09_decrease_ch_quality — Decrease channel quality measurement**
	20. The TC shall set MIDMARGIN_LOW to MIDMARGIN. 21. The TC shall check that MIDMARGIN_HIGH – MIDMARGIN_LOW is equal to 1 dB within a margin error of 0,1 dB. 22. If link status is equal to "bidirectional reliable link is established", then the TC shall repeat steps 17 to 21.
Iterations	N/A
Expected response	Result of check in step 21 is OK.
Remarks	A graph with channel attenuation in the x axis and MIDMARGIN in the y axis after step 16 can be built.

Table 13 specifies the interoperability test case 1.ITC_10_increase_ch_quality for the variable attenuation channel specified in 5.6.2.3.

Table 13 — 1.ITC_10_increase_ch_quality — Channel quality

Item	Content
Number – Title	**1.ITC_10_increase_ch_quality — Increase channel quality measurement**
Purpose	This test case determines that if the channel increases its quality, then the reported quality also increases.
Reference	REQ 1.9.
Prerequisites	Device shall provide access to the interfaces specified in 5.6.3.
Set-up	6.3 - Interoperability test set-up 2.
Step	1. The TC shall set the device climatic chamber temperature T_{device} to T_{typ}. 2. The TC shall set the device power supply voltage U_{device} to U_{typ}. 3. The TC shall set the LP climatic chamber temperature T_{LP} to T_{typ}. 4. The TC shall set the LP power supply voltage U_{LP} to U_{typ}. 5. The TC shall power up the LP. 6. The TC shall power up the device. 7. The TC shall set MINMARGIN to zero. 8. The TC shall set MAXMARGIN to zero. 9. The TC shall set channel attenuation to 10 dB. 10. The TC shall wait 100 ms. 11. If the device link status is not equal to "bidirectional reliable link is established", then the TC shall decrease the channel attenuation in 1 dB. 12. The UT shall read bit 7 to bit 0 from the device MDIO register 3.520 and store it into LINKMARGIN variable. 13. If LINKMARGIN is lower than the current value of MINMARGIN, then the TC shall store LINKMARGIN into MINMARGIN.

Table 13 *(continued)*

Item	Content
Number – Title	**1.ITC_10_increase_ch_quality — Increase channel quality measurement**
	14. If LINKMARGIN is greater than the current value of MAXMARGIN, then the TC shall store LINKMARGIN into MAXMARGIN. 15. The TC shall repeat 100 times the steps 12 to 14. 16. The TC shall set MIDMARGIN to MAXMARGIN/2 + MINMARGIN/2. 17. The TC shall set MIDMARGIN_LOW to MIDMARGIN. 18. Decrease channel attenuation in 1 dB. 19. The TC shall repeat steps 12 to 16. 20. The TC shall set MIDMARGIN_HIGH to MIDMARGIN. 21. The TC shall check that MIDMARGIN_HIGH – MIDMARGIN_LOW is equal to 1 dB within a margin error of 0,1 dB. 22. If channel attenuation is greater than 3 dB, then the TC shall repeat steps 17 to 21.
Iterations	N/A
Expected response	Result of check in step 21 is OK.
Remarks	A graph with channel attenuation in the x axis and MIDMARGIN in the y axis after step 16 can be built.

8 Device-level physical layer conformance test set-ups requirements

8.1 General

Clause 8 specifies the requirements of the test set-ups that are used in the device-level physical layer conformance test plan.

Most of the test set-ups involve a communication channel between the GEPOF entity stress test tool and the IUT. The different types of communication channels specified in 5.6 are used for the test set-ups.

The requirements on the GEPOF entity stress test tool and IUT for the test set-ups are specified in 8.2.1 and 8.2.2.

8.2 Test set-up requirements

8.2.1 IUT requirements for device-level physical layer conformance test plan

REQ	1.37 PHY — IUT requirements for device-level physical layer conformance test plan — GEPOF entities requirements
Each of the GEPOF entities in the IUT shall fulfil the requirements in ISO 21111-3 and ISO/IEC/IEEE 8802-3:2017/Amd 9.	

REQ	1.38 PHY — IUT requirements for device-level physical layer conformance test plan — MDIO interface
The IUT shall include at least one accessible MDIO interface as specified in ISO/IEC/IEEE 8802-3 that allows the individual access to each set of MDIO registers of each GEPOF entity in the IUT.	

REQ	1.39 PHY — IUT requirements for device-level physical layer conformance test plan — SYNCE pin
The IUT shall include at least an output dedicated pin to export a 10-MHz square electrical signal synchronized with the internal clock of the GEPOF entity. This dedicated pin is called SYNCE.	

REQ	1.40 PHY — IUT requirements for device-level physical layer conformance test plan — PMD_TXPWR.request(tx_pwr) control
The IUT shall include a mechanism to control the generation of the request PMD_TXPWR.request(tx_pwr) with a controlled value of the tx_pwr parameter as specified in ISO/IEEE/IEC 8802-3:2017/Amd 9:2018, 115.6.1.3.	

REQ	1.41 PHY — IUT requirements for device-level physical layer conformance test plan — Access and control of PHY service interface and neighbour service interface
If the IUT implements the wake-up and synchronized link sleep functionality as specified in ISO 21111-3, it shall include a way to access and control PHY service interface and neighbour service interface, as specified in ISO 21111-2.	

REQ	1.42 PHY — IUT requirements for device-level physical layer conformance test plan — Ethernet interface
The IUT shall include at least one Ethernet physical layer capable of 1 Gbit/s in addition to the one provided by the GEPOF entity.	

8.2.2 GEPOF entity stress test tool requirements

The lower tester as defined in ISO/IEC 9646-1 is specified for two test set-ups of this test plan as the GEPOF entity stress test tool.

REQ	1.43 PHY — GEPOF entity stress test tool — Required functionality
The GEPOF entity stress test tool shall include the following functionality: — LP functionality as specified in ISO 21111-3 and ISO/IEC/IEEE 8802.3:2017/Amd 9, — reset of the LP inside the GEPOF entity stress tool independently of the rest of the functionality, — set of the power state, as specified in ISO 21111-2, of the LP inside the GEPOF entity stress tool independently of the rest of the functionality, — control of the generation of the PHY_WakeUp.request as defined in ISO 21111-2, of the LP inside the GEPOF entity stress tool, — report of the PHY_WakeUp.indication as defined in ISO 21111-2, of the LP inside the GEPOF entity stress tool, — control and sense the generation of the request PMD_TXPWR.request(tx_pwr) with a controlled value of the tx_pwr parameter as specified in ISO/IEEE/IEC 8802-3:2017/Amd 9:2018, 115.6.1.3, — controlled Ethernet frame traffic generation, — Ethernet frame traffic analysis, including Ethernet frame error detection, and — bit error rate calculation.	

REQ	1.44 PHY — GEPOF entity stress test tool — Required optical interfaces
The GEPOF entity stress test tool shall have at least two optical interfaces: — optical transmission interface, compliant with the MDI (TX) specified in ISO/IEC/IEEE 8802.3:2017/Amd 9, and — optical reception interface, compliant with the MDI (RX) specified in ISO/IEC/IEEE 8802.3:2017/Amd 9.	

REQ	1.45 PHY — GEPOF entity stress test tool — Required optical interfaces
The GEPOF entity stress test tool shall have at least two optical interfaces: — optical transmission interface, compliant with the MDI (TX) specified in ISO/IEC/IEEE 8802.3:2017/Amd 9, and — optical reception interface, compliant with the MDI (RX) specified in ISO/IEC/IEEE 8802.3:2017/Amd 9.	

REQ	1.46 PHY — GEPOF entity stress test tool — Components used requirements
The components used for the implementation of the GEPOF entity stress tool shall comply with the requirements specified in ISO 21111-4.	

9 Device-level physical layer conformance test plan set-ups

9.1 General

The objective of the device-level physical layer conformance test plan is to verify a subset of requirements that are relevant for the device vendor.

The IUT for this test plan is a device that includes one or more GEPOF physical entities.

Each test plan set-up in this subclause specifies the LT and service provider that are used.

The IUT, LT, service provider, and UT are controlled by the TC. The TC implements the functionality of the test coordination procedure specified in ISO/IEC 9646-1.

The IUT has communication with the UT. The UT is able to generate and analyse data from the IUT and check if the result complies with the IUT requirements, as specified in ISO/IEC 9646-1.

Figure 11 shows the relationship between the IUT, LT, service provider, UT, and the TC.

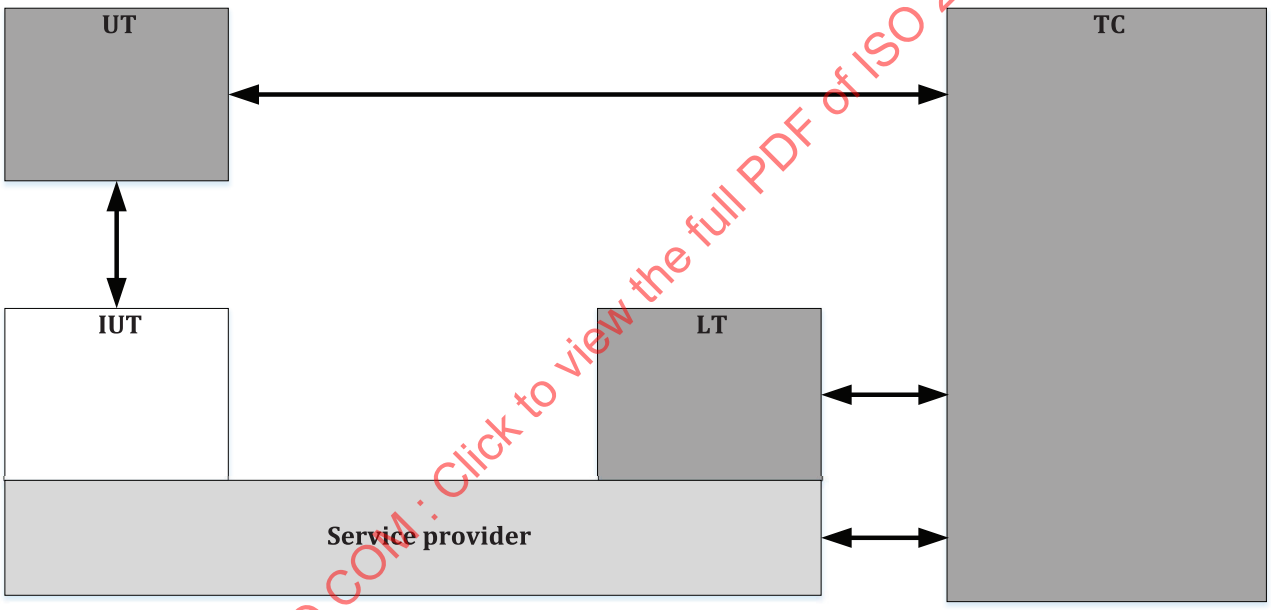


Figure 11 — Device-level physical layer conformance test environment

9.2 Device-level physical layer conformance test set-up 1

The device-level physical layer conformance test set-up 1 is composed of the IUT and one GEPOF entity stress test tool connected by a bidirectional channel that fulfils the requirements for the bidirectional high attenuation channel type specified in 5.6.2.1.

The IUT is placed inside a temperature chamber set to a controlled temperature *T*.

The IUT is powered by a controlled power supply voltage *U*.

The IUT may include a wake I/O block connected to a WAKE_IO pin as specified in ISO 21111-2: —, 6.6.

For the test cases that use this test set-up, to power up the IUT means to set the power_off_entity variable specified in ISO 21111-2 to FALSE for the GEPOF entity included in the IUT.

Symmetrically, to power down the IUT means to set the power_off_entity variable specified in ISO 21111-2 to TRUE for the GEPOF entity included in the IUT.

REQ	1.47 PHY — Device-level physical layer conformance test plan set-ups — Device-level physical layer conformance test set-up 1
The device-level physical layer conformance test setup 1 shall include the elements and the placement specified in Figure 12.	

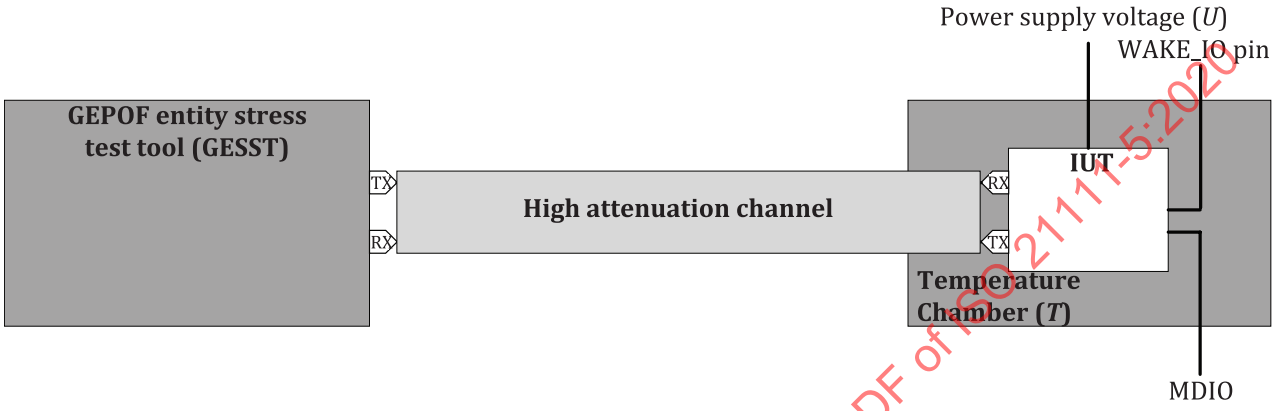


Figure 12 — Device-level physical layer conformance test set-up 1

9.3 Device-level physical layer conformance test set-up 2

The device-level physical layer conformance test set-up 1 is composed by the IUT and one GEPOF entity stress test tool connected by a bidirectional channel that fulfils the requirements for the bidirectional low attenuation channel type specified in 5.6.2.2.

The IUT is placed inside a temperature chamber set to a controlled temperature *T*.

The IUT is powered by a controlled power supply voltage *U*.

The IUT may include a wake I/O block connected to a WAKE_IO pin as specified in ISO 21111-2: —, 6.6.

For the test cases that use this test set-up, to power up the IUT means to set the power_off_entity variable specified in ISO 21111-2 to FALSE for the GEPOF entity included in the IUT.

Symmetrically, to power down the IUT means to set the power_off_entity variable specified in ISO 21111-2 to TRUE for the GEPOF entity included in the IUT.

REQ	1.48 PHY — Device-level physical layer conformance test plan set-ups — Device-level physical layer conformance test set-up 2
The device-level physical layer conformance test setup 2 shall include the elements and the placement specified in Figure 13.	

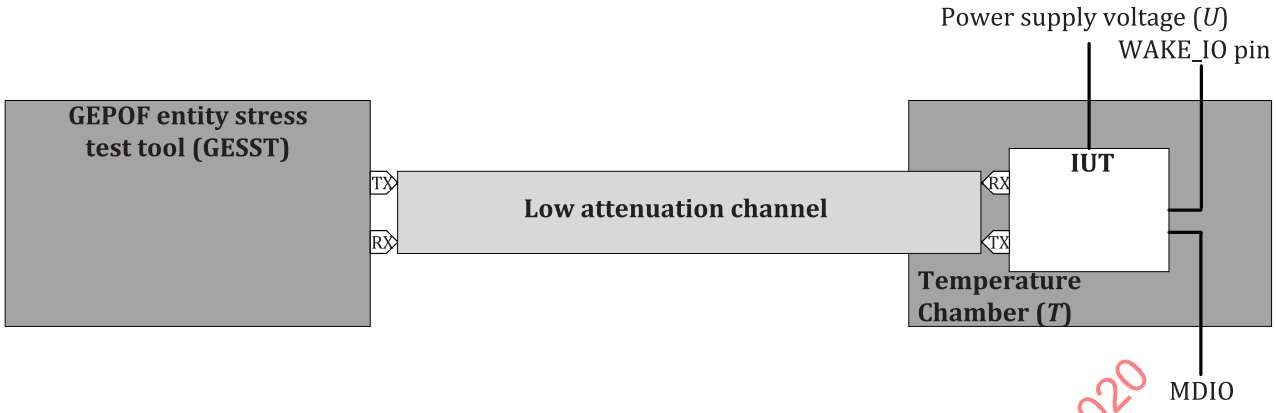


Figure 13 — Device-level physical layer conformance test set-up 2

9.4 Device-level physical layer conformance test set-up 3

The device-level physical layer conformance test set-up 3 is composed of the IUT and one oscilloscope with an optical to electrical converter connected by using a 1-m POF cable.

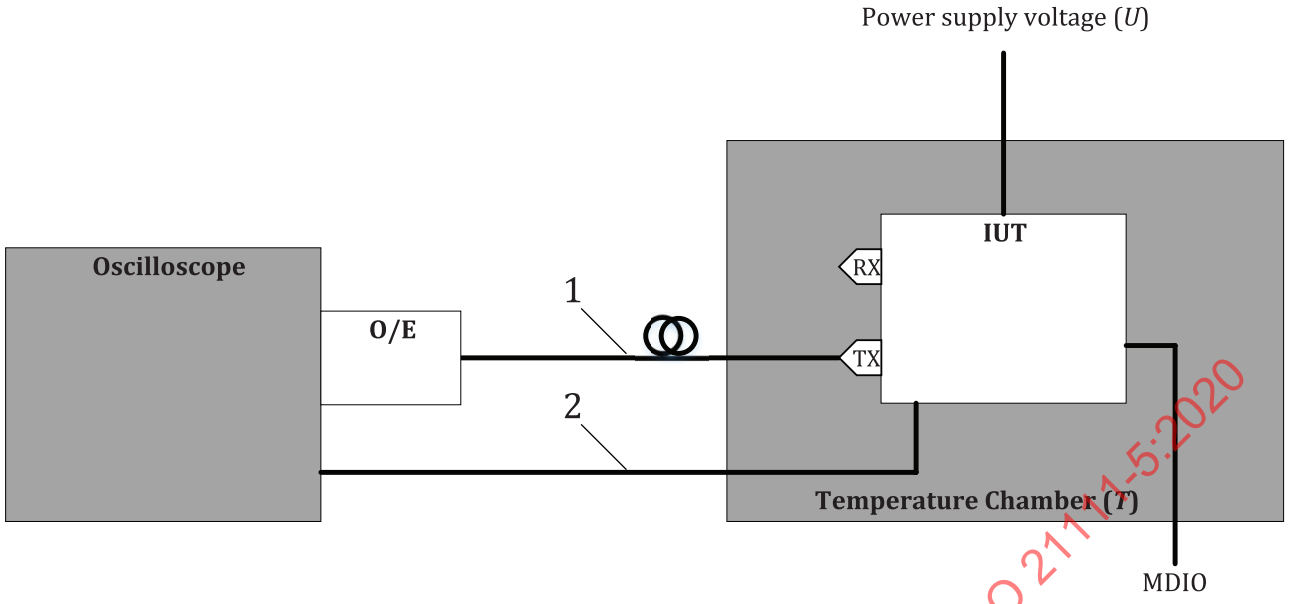
The POF cable is connected between the MDI (TX) interface of the IUT and the optical input of the optical to electrical converter.

The SYNCE pin of the IUT is connected to the external clock reference input of the oscilloscope.

The IUT is placed inside a temperature chamber set to a controlled temperature *T*.

The IUT is powered by a controlled power supply voltage *U*.

REQ	**1.49 PHY — Device-level physical layer conformance test plan set-ups — Device-level physical layer conformance test set-up 3**
The device-level physical layer conformance test setup 3 shall include the elements and the placement specified in Figure 14.	



Key

1 1-m simplex POF cable

2 SYNCE

Figure 14 — Device-level physical layer conformance test set-up 3

10 Device-level physical layer conformance test plan

10.1 General

The device-level physical layer conformance test plan is a set of test cases that checks physical layer requirements that are relevant for device vendors. This test plan is complementary to the physical layer conformance test plan specified in ISO 21111-3 that is typically required for GEPOF entity vendor. Additionally, component vendors are typically required to perform the applicable test methods specified in ISO 21111-4.

This test plan is structured in test groups. The test cases in the same test group share the same test set-up.

First test group includes the test cases that use a high attenuation channel.

Second test group includes the test cases that use a low attenuation channel.

Third test group includes the test cases that need to measure the optical IUT transmitter.

The wake-up and synchronized link sleep test group is divided in two subgroups.

The first subgroup includes the test cases that shall be run for a device that implements the wake-up and synchronized link sleep functionality, regardless the number of physical entities in the device.

The second subgroup includes the test cases that shall be run for a device that implements the wake-up and synchronized link sleep functionality and that includes more than one physical entity.

The device-level physical layer conformance test cases, which require variations of individual parameters, shall be repeated for each value of the parameter.

The device-level physical layer conformance test case specifications are intended to provide a high-level description of the motivation, resources, procedures, and methodologies pertinent to each test case. Each device-level physical layer conformance test case is specified according to a common structure also used for the interoperability test case (see Table 1). Some of the test cases are required

to be repeated for different values of the climatic chamber temperature T and different values of the voltage U that is supplied to the IUT. Table 14 specifies the required test case conditions T, U for variable temperature and supply test cases.

REQ	1.50 PHY — Device-level physical layer conformance test plan — Temperature and voltage values
The typical, minimum and maximum values T_{typ}, T_{min}, T_{max}, U_{typ}, U_{min} and U_{max} shall be provided by the test person.	

Table 14 — Required test case conditions T, U for variable temperature and supply test cases.

Iteration	T	U
1	T_{typ}	U_{typ}
2	T_{min}	U_{min}
3	T_{min}	U_{max}
4	T_{max}	U_{max}
5	T_{max}	U_{min}

10.2 High attenuation channel

Table 15 specifies the device-level physical layer conformance test case 1.DTC_01_system_reliability for the high attenuation channel specified in 5.6.2.1.

Table 15 — 1.DTC_01_system_reliability — High attenuation channel

Item	Content
Number – Title	**1.DTC_01_system_reliability — System reliability under high attenuation channel**
Purpose	This test case determines the communication reliability in a controlled network system at different temperatures and power supply voltages.
Reference	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.3, REQ 1.10, REQ 1.11, REQ 1.12, REQ 1.13.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1.
Set-up	9.2 - Device-level physical layer conformance test set-up 1.
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the GESST. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.518 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms.

Table 15 *(continued)*

Item	Content
Number – Title	**1.DTC_01_system_reliability — System reliability under high attenuation channel**
	10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the GESST to transmit continuously Ethernet frames of length randomly chosen between 1 byte and 1518 byte. The gaps between the Ethernet frames shall be at least 13 byte. 12. The TC shall wait 15 min. 13. The TC shall check that the GESST Ethernet frame error counter is equal to zero. 14. The TC shall check that the bit error rate reported by the GESST is lower than 10^{-12}. 15. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2.
Iterations	Perform iterations with test case conditions *T* and *U* as specified in Table 14.
Expected response	Result of check in steps 10, 13, 14 and 15 is OK for all iterations.
Remarks	N/A

Table 16 specifies the device-level physical layer conformance test case 1.DTC_02_link-up_LP_IUT_normal for the high attenuation channel specified in 5.6.2.1.

Table 16 — 1.DTC_02_link-up_LP_IUT_normal — High attenuation channel

Item	Content
Number – Title	**1.DTC_02_link-up_LP_IUT_normal — Link-up time when the LP and the IUT are in normal power state under high attenuation channel**
Purpose	This test case determines the link-up time when the LP and the IUT are in normal power state in a controlled network system at different temperatures and power supply voltages.
Reference	ISO 21111-3:2020, 6.4, REQ 1.7.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1.
Set-up	9.2 - Device-level physical layer conformance test set-up 1.
Step	1. The TC shall set climatic chamber temperature *T* to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage *U* to the corresponding value for the current iteration. 3. The TC shall power up the GESST. 4. The TC shall disable GESST optical power transmission. 5. The TC shall power up the IUT. 6. The TC shall wait 100 ms. 7. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.518 with 001_2. 8. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 9. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

Table 16 *(continued)*

Item	Content
Number – Title	**1.DTC_02_link-up_LP_IUT_normal — Link-up time when the LP and the IUT are in normal power state under high attenuation channel**
	10. The TC shall enable GESST optical power transmission. Then the TC shall reset to zero the T_LINKUP timer and start it. 11. The UT shall get the IUT link status at least once each millisecond. 12. When the IUT link status is equal to "bidirectional reliable link is established", the TC shall stop the T_LINKUP timer. 13. The TC shall check that the value in the T_LINKUP timer is lower than 100 ms.
Iterations	Perform iterations with test case conditions *T* and *U* as specified in Table 14.
Expected response	Result of check in step 13 is OK for all iterations.
Remarks	N/A

Table 17 specifies the device-level physical layer conformance test case 1.DTC_03_link-up_IUT_sleep for the high attenuation channel specified in 5.6.2.1.

Table 17 — 1.DTC_03_link-up_IUT_sleep — High attenuation channel

Item	Content
Number – Title	**1.DTC_03_link-up_IUT_sleep — Link-up time when IUT is in sleep power state under high attenuation channel**
Purpose	This test case determines the link-up time when the IUT is in sleep power state in a controlled network system at different temperatures and power supply voltages. The procedure to wake-up the IUT is the reception of a WakeUp_request event.
Reference	ISO 21111-3:2020, 6.4, REQ 1.4.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1.
Set-up	9.2 - Device-level physical layer conformance test set-up 1.
Step	1. The TC shall set climatic chamber temperature *T* to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage *U* to the corresponding value for the current iteration. 3. The TC shall power up the GESST. 4. The TC shall disable GESST optical power transmission. 5. The TC shall power up the IUT. 6. The TC shall wait 100 ms. 7. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.518 with 001_2. 8. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 9. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 10. The TC shall set IUT into sleep power state. 11. The TC shall enable GESST optical power transmission. Then the TC shall reset to zero the T_LINKUP timer and start it.

Table 17 *(continued)*

Item	Content
Number – Title	**1.DTC_03_link-up_IUT_sleep — Link-up time when IUT is in sleep power state under high attenuation channel**
	12. The UT shall get the IUT link status at least once each millisecond. 13. When the IUT link status is equal to "bidirectional reliable link is established", the TC shall stop the T_LINKUP timer. 14. The TC shall check that the value in the T_LINKUP timer is lower than 100 ms.
Iterations	Perform iterations with test case conditions *T* and *U* as specified in Table 14.
Expected response	Result of check in step 14 is OK for all iterations.
Remarks	N/A

Table 18 specifies the device-level physical layer conformance test case 1.DTC_04_link-up_LP_IUT_sleep for the high attenuation channel specified in 5.6.2.1.

Table 18 — 1.DTC_04_link-up_LP_IUT_sleep — High attenuation channel

Item	Content
Number – Title	**1.DTC_04_link-up_LP_IUT_sleep — Link-up time when the LP and the IUT are in sleep power state under high attenuation channel**
Purpose	This test case determines the link-up time when the LP and the IUT are in sleep power state in a controlled network system at different temperatures and power supply voltages. The LP wake-up is performed by a PHY_WakeUp_request.
Reference	ISO 21111-3:2020, 6.4, REQ 1.3.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1.
Set-up	9.2 - Device-level physical layer conformance test set-up 1.
Step	1. The TC shall set climatic chamber temperature *T* to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage *U* to the corresponding value for the current iteration. 3. The TC shall power up the GESST. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The TC shall set IUT and GESST into sleep power state. 7. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.518 with 001_2. 8. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 9. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 10. The TC shall set the GESST to generate the PHY_WakeUp.request. Then the TC shall reset to zero the T_LINKUP timer and start it. 11. The UT shall get the IUT link status at least once each millisecond. 12. When the IUT link status is equal to "bidirectional reliable link is established", the TC shall stop the T_LINKUP timer. 13. The TC shall check that the value in the T_LINKUP timer is lower than 100 ms.
Iterations	Perform iterations with test case conditions *T* and *U* as specified in Table 14.

Table 18 *(continued)*

Item	Content
Number – Title	**1.DTC_04_link-up_LP_IUT_sleep — Link-up time when the LP and the IUT are in sleep power state under high attenuation channel**
Expected response	Result of check in step 13 is OK for all iterations.
Remarks	N/A

Table 19 specifies the device-level physical layer conformance test case 1.DTC_05_consumption_operation for the high attenuation channel specified in 5.6.2.1.

Table 19 — 1.DTC_05_consumption_operation — High attenuation channel

Item	Content
Number – Title	**1.DTC_05_consumption_operation — IUT power consumption in operation under high attenuation channel**
Purpose	This test case determines the IUT power consumption in operation in a controlled network system at different temperatures and power supply voltages.
Reference	IDD_{min} and IDD_{max} shall be provided by the test person.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1.
Set-up	9.2 - Device-level physical layer conformance test set-up 1.
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the GESST. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.518 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms. 10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the GESST to transmit continuously Ethernet frames of length randomly chosen between 1 byte and 1518 byte. The gaps between the Ethernet frames shall be at least 13 byte. 12. The TC shall wait 15 min. 13. The TC shall measure IDD_{device}. 14. The TC shall check that IDD_{device} is higher than IDD_{min} and lower than IDD_{max}.
Iterations	Perform iterations with test case conditions T and U as specified in Table 14.
Expected response	Result of check in step 14 is OK for all iterations.
Remarks	N/A

Table 20 specifies the device-level physical layer conformance test case 1.DTC_06_consumption_sleep for the high attenuation channel specified in 5.6.2.1.

Table 20 — 1.DTC_06_consumption_sleep — High attenuation channel

Item	Content
Number – Title	**1.DTC_06_consumption_sleep — IUT power consumption in sleep power state under high attenuation channel**
Purpose	This test case determines the IUT power consumption in sleep power state in a controlled network system at different temperatures and power supply voltages.
Reference	IDD_DIS_{min} and IDD_DIS_{max} shall be provided by the test person.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1.
Set-up	9.2 - Device-level physical layer conformance test set-up 1.
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the GESST. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.518 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms. 10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the LP inside the GESST to sleep power state. 12. The TC shall set the IUT to sleep power state. 13. The TC shall measure IDD_{device}. 14. The TC shall check that IDD_{device} is higher than IDD_DIS_{min} and lower than IDD_DIS_{max}.
Iterations	Perform iterations with test case conditions T and U as specified in Table 14.
Expected response	Result of check in step 14 is OK for all iterations.
Remarks	N/A

10.3 Low attenuation channel

Table 21 specifies the device-level physical layer conformance test case 1.DTC_07_system_reliability for the low attenuation channel specified in 5.6.2.2.

Table 21 — 1.DTC_07_system_reliability — Low attenuation channel

Item	Content
Number – Title	**1.DTC_07_system_reliability — System reliability under low attenuation channel**
Purpose	This test case determines the communication reliability in a controlled network system at different temperatures and power supply voltages.
Reference	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.3.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1.
Set-up	9.3 - Device-level physical layer conformance test set-up 2.
Step	1. The TC shall set climatic chamber temperature *T* to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage *U* to the corresponding value for the current iteration. 3. The TC shall power up the GESST. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.518 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms. 10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the GESST to transmit continuously Ethernet frames of length randomly chosen between 1 byte and 1518 byte. The gaps between the Ethernet frames shall be at least 13 byte. 12. The TC shall wait 15 min. 13. The TC shall check that the GESST Ethernet frame error counter is equal to zero. 14. The TC shall check that the bit error rate reported by the GESST is lower than 10^{-12}. 15. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2.
Iterations	Perform iterations with test case conditions *T* and *U* as specified in Table 14.
Expected response	Result of check in steps 10, 13, 14 and 15 is OK for all iterations.
Remarks	N/A

Table 22 specifies the device-level physical layer conformance test case 1.DTC_08_link-up_IUT_normal for the low attenuation channel specified in 5.6.2.2.

Table 22 — 1.DTC_08_link-up_IUT_normal — Low attenuation channel

Item	Content
Number – Title	**1.DTC_08_link-up_IUT_normal — Link-up time when the LP and the IUT are in normal power state under low attenuation channel**
Purpose	This test case determines the link-up time when the LP and the IUT are in normal power state in a controlled network system at different temperatures and power supply voltages.
Reference	ISO 21111-3:2020, 6.4, REQ 1.7.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1.
Set-up	9.3 - Device-level physical layer conformance test set-up 2.
Step	1. The TC shall set climatic chamber temperature *T* to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage *U* to the corresponding value for the current iteration. 3. The TC shall power up the GESST. 4. The TC shall disable GESST optical power transmission. 5. The TC shall power up the IUT. 6. The TC shall wait 100 ms. 7. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.518 with 001_2. 8. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 9. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 10. The TC shall enable GESST optical power transmission. Then the TC shall reset to zero the T_LINKUP timer and start it. 11. The UT shall get the IUT link status at least once each millisecond. 12. When the IUT link status is equal to "bidirectional reliable link is established", the TC shall stop the T_LINKUP timer. 13. The TC shall check that the value in the T_LINKUP timer is lower than 100 ms.
Iterations	Perform iterations with test case conditions *T* and *U* as specified in Table 14.
Expected response	Result of check in step 13 is OK for all iterations.
Remarks	N/A

Table 23 specifies the device-level physical layer conformance test case 1.DTC_09_link-up_IUT_sleep for the low attenuation channel specified in 5.6.2.2.

Table 23 — 1.DTC_09_link-up_IUT_sleep — Low attenuation channel

Item	Content
Number – Title	**1.DTC_09_link-up_IUT_sleep — Link-up time when IUT is in sleep power state under low attenuation channel**
Purpose	This test case determines the link-up time when the IUT is in sleep power state in a controlled network system at different temperatures and power supply voltages. The procedure to wake-up the IUT is the reception of a WakeUp_request event.
Reference	ISO 21111-3:2020, 6.4, REQ 1.4.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1.
Set-up	9.3 - Device-level physical layer conformance test set-up 2.
Step	1. The TC shall set climatic chamber temperature *T* to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage *U* to the corresponding value for the current iteration. 3. The TC shall power up the GESST. 4. The TC shall disable GESST optical power transmission. 5. The TC shall power up the IUT. 6. The TC shall wait 100 ms. 7. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.518 with 001_2. 8. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 9. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 10. The TC shall set IUT into sleep power state. 11. The TC shall enable GESST optical power transmission. Then the TC shall reset to zero the T_LINKUP timer and start it. 12. The UT shall get the IUT link status at least once each millisecond. 13. When the IUT link status is equal to "bidirectional reliable link is established", the TC shall stop the T_LINKUP timer. 14. The TC shall check that the value in the T_LINKUP timer is lower than 100 ms.
Iterations	Perform iterations with test case conditions *T* and *U* as specified in Table 14.
Expected response	Result of check in step 14 is OK for all iterations.
Remarks	N/A

Table 24 specifies the device-level physical layer conformance test case 1.DTC_10_link-up_LP_IUT_sleep for the low attenuation channel specified in 5.6.2.2.

Table 24 — 1.DTC_10_link-up_LP_IUT_sleep — Low attenuation channel

Item	Content
Number – Title	**1.DTC_10_link-up_LP_IUT_sleep — Link-up time when the LP and the IUT are in sleep power state under high attenuation channel**
Purpose	This test case determines the link-up time when the LP and the IUT are in sleep power state in a controlled network system at different temperatures and power supply voltages. The LP wake-up is performed by a PHY_WakeUp_request.
Reference	ISO 21111-3:2020, 6.4, REQ 1.3.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1.
Set-up	9.3 - Device-level physical layer conformance test set-up 2.
Step	1. The TC shall set climatic chamber temperature *T* to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage *U* to the corresponding value for the current iteration. 3. The TC shall power up the GESST. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The TC shall set IUT and GESST into sleep power state. 7. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.518 with 001_2. 8. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 9. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 10. The TC shall set the GESST to generate the PHY_WakeUp.request. Then the TC shall reset to zero the T_LINKUP timer and start it. 11. The UT shall get the IUT link status at least once each millisecond. 12. When the IUT link status is equal to "bidirectional reliable link is established", the TC shall stop the T_LINKUP timer. 13. The TC shall check that the value in the T_LINKUP timer is lower than 100 ms.
Iterations	Perform iterations with test case conditions *T* and *U* as specified in Table 14.
Expected response	Result of check in step 13 is OK for all iterations.
Remarks	N/A

Table 25 specifies the device-level physical layer conformance test case 1.DTC_11_consumption_operation for the low attenuation channel specified in 5.6.2.2.

Table 25 — 1.DTC_11_consumption_operation — Low attenuation channel

Item	Content
Number – Title	**1.DTC_11_consumption_operation — IUT power consumption in operation under low attenuation channel**
Purpose	This test case determines the IUT power consumption in operation in a controlled network system at different temperatures and power supply voltages.
Reference	IDD_{min} and IDD_{max} shall be provided by the test person.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1.
Set-up	9.3 - Device-level physical layer conformance test set-up 2.
Step	1. The TC shall set climatic chamber temperature *T* to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage *U* to the corresponding value for the current iteration. 3. The TC shall power up the GESST. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.518 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms. 10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the GESST to transmit continuously Ethernet frames of length randomly chosen between 1 byte and 1518 byte. The gaps between the Ethernet frames shall be at least 13 byte. 12. The TC shall wait 15 min. 13. The TC shall measure IDD_{device}. 14. The TC shall check that IDD_{device} is higher than IDD_{min} and lower than IDD_{max}.
Iterations	Perform iterations with test case conditions *T* and *U* as specified in Table 14.
Expected response	Result of check in step 14 is OK for all iterations.
Remarks	N/A

Table 26 specifies the device-level physical layer conformance test case 1.DTC_12_consumption_sleep for the low attenuation channel specified in 5.6.2.2.

Table 26 — 1.DTC_12_consumption_sleep — Low attenuation channel

Item	Content
Number – Title	**1.DTC_12_consumption_sleep — IUT power consumption in sleep power state under low attenuation channel**
Purpose	This test case determines the IUT power consumption in sleep power state in a controlled network system at different temperatures and power supply voltages.
Reference	IDD_DIS_{min} and IDD_DIS_{max} shall be provided by the test person.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1.
Set-up	9.3 - Device-level physical layer conformance test set-up 2.
Step	1. The TC shall set climatic chamber temperature *T* to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage *U* to the corresponding value for the current iteration. 3. The TC shall power up the GESST. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.518 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms. 10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the LP inside the GESST to sleep power state. 12. The TC shall set the IUT to sleep power state. 13. The TC shall measure IDD_{device}. 14. The TC shall check that IDD_{device} is higher than IDD_DIS_{min} and lower than IDD_DIS_{max}.
Iterations	Perform iterations with test case conditions *T* and *U* as specified in Table 14.
Expected response	Result of check in step 14 is OK for all iterations.
Remarks	N/A

10.4 Optical IUT transmitter measurements

Table 27 specifies the device-level physical layer conformance test case 1.DTC_13_AOP for measuring IUT transmitter optical parameters.

Table 27 — 1.DTC_13_AOP — Optical IUT transmitter measurements

Item	Content
Number – Title	**1.DTC_13_AOP — Optical IUT transmitter AOP at TP2**
Purpose	This test case determines the IUT AOP at TP2 and checks that it is in the expected range.
Reference	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.3 and Table 115-8.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1. AOP measurement using set-up 9.4 shall be calibrated with a large area photodetector able to couple all the output optical power from the POF, as specified in the reference. This test case result shall include the method used to calibrate and calculate the AOP.
Set-up	9.4 - Device-level physical layer conformance test set-up 3.
Step	1. The TC shall set climatic chamber temperature *T* to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage *U* to the corresponding value for the current iteration. 3. The TC shall power up the IUT. 4. The TC shall wait 100 ms. 5. The UT shall write the IUT MDIO register bit 15 to bit 13 of the MDIO register 3.518 with 101_2. 6. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 7. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 8. The TC shall measure the voltage level in the oscilloscope and calculate the AOP.
Iterations	Perform iterations with test case conditions *T* and *U* as specified in Table 14.
Expected response	AOP obtained in step 8 measurement is in the range for RHC specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018 Table 115-8.
Remarks	AOP calculation from oscilloscope voltage measurement depends on the optical to electrical converter characteristics and calibration of the test set-up.

Table 28 specifies the device-level physical layer conformance test case 1.DTC_14_AOP_off for measuring IUT transmitter optical parameters.

Table 28 — 1.DTC_14_AOP_off — Optical IUT transmitter measurements

Item	Content
Number – Title	**1.DTC_14_AOP_off — Optical IUT transmitter AOP when transmission is set to OFF at TP2**
Purpose	This test case determines the IUT AOP at TP2 when the transmitter is set to off and checks that it is below the value specified.
Reference	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.3 and Table 115-8.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1. AOP measurement using set-up 9.4 shall be calibrated with a large area photodetector able to couple all the output optical power from the POF, as specified in the reference. This test case result shall include the method used to calibrate and calculate the AOP.
Set-up	9.4 - Device-level physical layer conformance test set-up 3.
Step	1. The TC shall set climatic chamber temperature *T* to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage *U* to the corresponding value for the current iteration. 3. The TC shall power up the IUT. 4. The TC shall wait 100 ms. 5. The UT shall write the IUT MDIO register bit 15 to bit 13 of the MDIO register 3.518 with 101_2. 6. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 7. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 8. The TC shall set the IUT TXPWR_EN input pin to zero. 9. The TC shall measure the voltage level in the oscilloscope and calculate the AOP.
Iterations	Perform iterations with test case conditions *T* and *U* as specified in Table 14.
Expected response	AOP obtained in step 9 measurement is lower than the maximum value for RHC specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018 Table 115-8.
Remarks	AOP calculation from oscilloscope voltage measurement depends on the optical to electrical converter characteristics and calibration of the test set-up.

Table 29 specifies the device-level physical layer conformance test case 1.DTC_15_distortion for measuring IUT transmitter optical parameters.

Table 29 — 1.DTC_15_distortion — Optical IUT transmitter measurements

Item	Content
Number – Title	**1.DTC_15_distortion — Optical IUT transmitter distortion at TP2**
Purpose	This test case determines the IUT distortion at TP2 and checks that it is in the expected range.
Reference	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.8 and Table 115-8.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1. The oscilloscope used in set-up 9.4 shall be able to store at least 13 µs sampled with the minimum sampling rate of 3,25 Gigasamples per second.
Set-up	9.4 - Device-level physical layer conformance test set-up 3.
Step	1. The TC shall set climatic chamber temperature *T* to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage *U* to the corresponding value for the current iteration. 3. The TC shall power up the IUT. 4. The TC shall wait 100 ms. 5. The UT shall write the IUT MDIO register bit 15 to bit 13 of the MDIO register 3.518 with 110_2. 6. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 7. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 8. The TC shall capture at least 13 µs of the transmitted optical signal with the oscilloscope. 9. The TC shall calculate the distortion values HD_2, HD_3, HD_4 and *RD* from the captured optical signal by using the processing specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.8.
Iterations	Perform iterations with test case conditions *T* and *U* as specified in Table 14.
Expected response	HD_2, HD_3, HD_4 and *RD* values obtained in step 9 measurements is lower than the maximum value for RHC specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018 Table 115-8.
Remarks	N/A

Table 30 specifies the device-level physical layer conformance test case 1.DTC_16_droop for measuring IUT transmitter optical parameters.

Table 30 — 1.DTC_16_droop — Optical IUT transmitter measurements

Item	Content
Number – Title	**1.DTC_16_droop — Optical IUT transmitter positive and negative droop output at TP2**
Purpose	This test case determines the IUT positive and negative droop output at TP2 and checks that they are in the expected range.
Reference	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.7 and Table 115-8.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1. AOP shall be previously calculated by using 1.DTC_13_AOP and the resulting voltage level in the oscilloscope shall be stored in $AOP_{voltage}$. Oscilloscope used for the set-up specified in 9.4 shall have a minimum bandwidth of 812,5 MHz (−3 dB cut-off frequency).
Set-up	9.4 - Device-level physical layer conformance test set-up 3.
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the IUT. 4. The TC shall wait 100 ms. 5. The UT shall write the IUT MDIO register bit 15 to bit 13 of the MDIO register 3.518 with 011_2. 6. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 7. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 8. The TC shall measure the voltage level in the oscilloscope over a 2-ns window centred 15 ns after the rising-edge crossing $AOP_{voltage}$. 9. The TC shall calculate the optical power in mW. Store it in P_1. 10. The TC shall measure the voltage level in the oscilloscope over a 2-ns window centred 15 ns after the falling-edge crossing $AOP_{voltage}$. 11. The TC shall calculate the optical power in mW. Store it in P_0. 12. The TC shall calculate and store the reference extinction ratio ER_0 as $ER_0 = 10 \times \log_{10}\left(\frac{P_1}{P_0}\right)$. 13. The UT shall write the IUT MDIO register bit 15 to bit 13 of the MDIO register 3.518 with 100_2. 14. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 15. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 16. The TC shall capture with the oscilloscope at least 47 µs of the optical signal. 17. The TC shall find the first rising-edge crossing $AOP_{voltage}$ in the capture. The TC shall set N to 1.

Table 30 *(continued)*

Item	Content
Number – Title	**1.DTC_16_droop — Optical IUT transmitter positive and negative droop output at TP2**
	18. The TC shall measure the voltage level in the oscilloscope over a 2-ns window centred 15 ns after the rising-edge crossing $AOP_{voltage}$. 19. The TC shall calculate the optical power in mW. Store it in P_1. 20. The TC shall measure the voltage level in the oscilloscope over a 2-ns window centred 15 ns after the falling-edge crossing $AOP_{voltage}$. 21. The TC shall calculate the optical power in mW. Store it in P_0. 22. The TC shall calculate and store the extinction ratio ER_N as $ER_N = 10 \times \log_{10}\left(\frac{P_1}{P_0}\right)$. 23. The TC shall find the next rising-edge crossing $AOP_{voltage}$ in the capture. The TC shall set N to $N + 1$. 24. The TC shall repeat procedure steps 18 to 23 until the next pair rising and falling-edge is in the capture. 25. The TC shall select the maximum value among the extinction ratios ER_N and store it in ER_{max}. 26. The TC shall select the minimum value among the extinction ratios ER_N and store it in ER_{min}. 27. The TC shall calculate the positive output droop DO^+ as $DO^+ = ER_{max} - ER_0$. 28. The TC shall calculate the negative output droop DO^- as $DO^- = ER_{min} - ER_0$.
Iterations	Perform iterations with test case conditions T and U as specified in Table 14.
Expected response	Positive and negative output droop DO^+ and DO^- obtained in steps 27 and 28 calculation is in the range for RHC specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018 Table 115-8.
Remarks	N/A

Table 31 specifies the device-level physical layer conformance test case 1.DTC_17_overshoot for measuring IUT transmitter optical parameters.

Table 31 — 1.DTC_17_overshoot — Optical IUT transmitter measurements

Item	Content
Number – Title	**1.DTC_17_overshoot — Optical IUT transmitter overshoot at TP2**
Purpose	This test case determines the IUT rising and falling edge overshoot at TP2 and checks that it is in the expected range.
Reference	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.6 and Table 115-8.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1. AOP shall be previously calculated by using 1.DTC_13_AOP and the resulting voltage level in the oscilloscope shall be stored in $AOP_{voltage}$. Oscilloscope used for the set-up specified in 9.4 shall have a minimum bandwidth of 812,5 MHz (–3 dB cut-off frequency).
Set-up	9.4 - Device-level physical layer conformance test set-up 3.

Table 31 *(continued)*

Item	Content
Number – Title	**1.DTC_17_overshoot — Optical IUT transmitter overshoot at TP2**
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the IUT. 4. The TC shall wait 100 ms. 5. The UT shall write the IUT MDIO register bit 15 to bit 13 of the MDIO register 3.518 with 011_2. 6. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 7. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 8. The TC shall capture with the oscilloscope at least 47 µs of the optical signal. 9. The TC shall find the first rising-edge crossing $AOP_{voltage}$ in the capture. The TC shall set N to 1. 10. The TC shall measure the maximum voltage level in the oscilloscope in the time interval between the rising-edge crossing $AOP_{voltage}$ and the next falling-edge crossing $AOP_{voltage}$. 11. The TC shall calculate the optical power in mW. Store it in P_{max}. 12. The TC shall measure the voltage level in the oscilloscope over a 2-ns window centred 15 ns after the rising-edge crossing $AOP_{voltage}$. 13. The TC shall calculate the optical power in mW. Store it in P_1. 14. The TC shall measure the minimum voltage level in the oscilloscope in the time interval between the falling-edge crossing $AOP_{voltage}$ and the next rising-edge crossing $AOP_{voltage}$. 15. The TC shall calculate the optical power in mW. Store it in P_{min}. 16. The TC shall measure the voltage level in the oscilloscope over a 2-ns window centred 15 ns after the falling-edge crossing $AOP_{voltage}$. 17. The TC shall calculate the optical power in mW. Store it in P_0. 18. The TC shall calculate the rising-edge overshoot OS_{rise} as $OS_{rise} = \frac{P_{max} - P_1}{P_1 - P_0}$. 19. The TC shall calculate the falling-edge overshoot OS_{fall} as $OS_{fall} = \frac{P_0 - P_{min}}{P_1 - P_0}$.
Iterations	Perform iterations with test case conditions T and U as specified in Table 14.
Expected response	Rising and falling-edge overshoot OS_{rise} and OS_{fall} obtained in steps 18 and 19 calculation are in the range for RHC specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018 Table 115-8.
Remarks	N/A

Table 32 specifies the device-level physical layer conformance test case 1.DTC_18_RMS_jitter for measuring IUT transmitter optical parameters.

Table 32 — 1.DTC_18_RMS_jitter — Optical IUT transmitter measurements

Item	Content
Number – Title	**1.DTC_18_RMS_jitter — Optical IUT transmitter RMS jitter at TP2**
Purpose	This test case determines the IUT RMS jitter at TP2 and checks that it is in the expected range.
Reference	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.9 and Table 115-8.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1. Oscilloscope used for the set-up specified in 9.4 shall have for this test case a high-frequency low-pass corner of at least 32,5 MHz with slope of -20 dB/decade. Oscilloscope used for the set-up specified in 9.4 shall have for this test case a low-frequency high-pass corner of maximum 1 KHz with slope of +20 dB/decade.
Set-up	9.4 - Device-level physical layer conformance test set-up 3.
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the IUT. 4. The TC shall wait 100 ms. 5. The UT shall write the IUT MDIO register bit 15 to bit 13 of the MDIO register 3.518 with 010_2. 6. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 7. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 8. The TC shall measure RMS jitter t_j of the crossing events of the optical signal captured by the oscilloscope over an interval of 2 ms ± 10 %. The unjittered clock reference is obtained following the procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.9 4).
Iterations	Perform iterations with test case conditions T and U as specified in Table 14.
Expected response	RMS jitter t_j obtained in step 8 measurement is in the range for RHC specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018 Table 115-8.
Remarks	N/A

Table 33 specifies the device-level physical layer conformance test case 1.DTC_19_ER for measuring IUT transmitter optical parameters.

Table 33 — 1.DTC_19_ER — Optical IUT transmitter measurements

Item	Content
Number – Title	**1.DTC_19_ER — Optical IUT transmitter ER at TP2**
Purpose	This test case determines the IUT ER at TP2 and checks that it is in the expected range.
Reference	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.3 and Table 115-8.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1. AOP shall be previously calculated by using 1.DTC_13_AOP and the resulting voltage level in the oscilloscope shall be stored in $AOP_{voltage}$. Oscilloscope used for the set-up specified in 9.4 shall have a minimum bandwidth of 812,5 MHz (–3 dB cut-off frequency).
Set-up	9.4 - Device-level physical layer conformance test set-up 3.

Table 33 *(continued)*

Item	Content
Number – Title	**1.DTC_19_ER — Optical IUT transmitter ER at TP2**
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the IUT. 4. The TC shall wait 100 ms. 5. The UT shall write the IUT MDIO register bit 15 to bit 13 of the MDIO register 3.518 with 011_2. 6. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 7. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 8. The TC shall measure the voltage level in the oscilloscope over a 2-ns window centred 15 ns after the rising-edge crossing $AOP_{voltage}$. 9. The TC shall calculate the optical power in mW. Store it in P_1. 10. The TC shall measure the voltage level in the oscilloscope over a 2-ns window centred 15 ns after the falling-edge crossing $AOP_{voltage}$. 11. The TC shall calculate the optical power in mW. Store it in P_0. 12. The TC shall calculate the extinction ratio ER as $ER = 10 \times \log_{10}\left(\frac{P_1}{P_0}\right)$.
Iterations	Perform iterations with test case conditions T and U as specified in Table 14.
Expected response	ER obtained in step 12 measurement is in the range for RHC specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018 Table 115-8.
Remarks	N/A

Table 34 specifies the device-level physical layer conformance test case 1.DTC_20_rise_fall_times for measuring IUT transmitter optical parameters.

Table 34 — 1.DTC_20_rise_fall_times — Optical IUT transmitter measurements

Item	Content
Number – Title	**1.DTC_20_rise_fall_times — Optical IUT transmitter rise and fall times at TP2**
Purpose	This test case determines the IUT rise and fall times at TP2 and checks that they are in the expected range.
Reference	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.4 and Table 115-8.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1. AOP measurement using the set-up in 9.4 shall be calibrated with a large area photodetector able to couple all the output optical power from the POF, as specified in the reference.
Set-up	9.4 - Device-level physical layer conformance test set-up 3.

Table 34 *(continued)*

Item	Content
Number – Title	**1.DTC_20_rise_fall_times — Optical IUT transmitter rise and fall times at TP2**
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the IUT. 4. The TC shall wait 100 ms. 5. The UT shall write the IUT MDIO register bit 15 to bit 13 of the MDIO register 3.518 with 011_2. 6. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 7. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 8. The TC shall measure the voltage level in the oscilloscope over a 2-ns window centred 15 ns after the rising-edge crossing $AOP_{voltage}$. 9. The TC shall calculate the optical power in mW. Store it in P_1. 10. The TC shall measure the voltage level in the oscilloscope over a 2-ns window centred 15 ns after the falling-edge crossing $AOP_{voltage}$. 11. The TC shall calculate the optical power in mW. Store it in P_0. 12. The TC shall calculate the rise time t_r as the time taken for the optical signal to transition from value $(0,1 \times P_1 + 0,9 \times P_0)$ to value $(0,1 \times P_0 + 0,9 \times P_1)$ and stay above the second value. 13. The TC shall calculate the fall time t_f as the time taken for the optical signal to transition from value $(0,1 \times P_0 + 0,9 \times P_1)$ to value $(0,1 \times P_1 + 0,9 \times P_0)$ and stay below the second value.
Iterations	Perform iterations with test case conditions T and U as specified in Table 14.
Expected response	Rise time t_r and fall time t_f obtained in steps 12 and 13 measurement are below the maximum values for RHC specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018 Table 115-8.
Remarks	N/A

Table 35 specifies the device-level physical layer conformance test case 1.DTC_21_RIN for measuring IUT transmitter optical parameters.

Table 35 — 1.DTC_21_RIN — Optical IUT transmitter measurements

Item	Content
Number – Title	**1.DTC_21_RIN — Optical IUT transmitter RIN at TP2**
Purpose	This test case determines the IUT RIN at TP2 and checks that it is in the expected range.
Reference	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.10 and Table 115-8.
Prerequisites	IUT shall provide access to the interfaces specified in 8.2.1.
Set-up	9.4 - Device-level physical layer conformance test set-up 3.