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Road vehicles— FlexRay communications system —

Part 4: **Electrical physical layer specification**

Véhicules routiers — Système de communications FlexRay —

Partie 4: Spécification de la couche d'application électrique

Reference number
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Foreword

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International Standards are drafted in accordance with the rules given in the ISO/IEC Directives, Part 2.

The main task of technical committees is to prepare International Standards. Draft International Standards adopted by the technical committees are circulated to the member bodies for voting. Publication as an International Standard requires approval by at least 75 % of the member bodies casting a vote.

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ISO 17458-4 was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 3, *Electrical and electronic equipment*.

ISO 17458 consists of the following parts, under the general title *Road vehicles — FlexRay communications system*:

— *Part 1: General information and use case definition*

— *Part 2: Data link layer specification*

— *Part 3: Data link layer conformance test specification*

— *Part 4: Electrical physical layer specification*

— *Part 5: Electrical physical layer conformance test specification*

Introduction

The FlexRay communications system is an automotive focused high speed network and was developed with several main objectives which were defined beyond the capabilities of established standardized bus systems like CAN and some other proprietary bus systems. Some of the basic characteristics of the FlexRay protocol are synchronous and asynchronous frame transfer, guaranteed frame latency and jitter during synchronous transfer, prioritization of frames during asynchronous transfer, single or multi-master clock synchronization, time synchronization across multiple networks, error detection and signalling, and scalable fault tolerance.

The FlexRay communications system is defined for advanced automotive control applications. It serves as a communication infrastructure for future generation high-speed control applications in vehicles by providing:

- A message exchange service that provides deterministic cycle based message transport;
- Synchronization service that provides a common time base to all nodes;
- Start-up service that provides an autonomous start-up procedure;
- Error management service that provides error handling and error signalling;
- Wakeup service that addresses the power management needs.

Since start of development the automotive industry world-wide supported the specification development. The FlexRay communications system has been successfully implemented in production vehicles today.

The ISO 17458 series specifies the use cases, the communication protocol and physical layer requirements of an in-vehicle communication network called "FlexRay communications system".

This part of ISO 17458 has been established in order to define the electrical physical layer of the FlexRay data link.

To achieve this, it is based on the Open Systems Interconnection (OSI) Basic Reference Model specified in ISO/IEC 7498-1 and ISO/IEC 10731, which structures communication systems into seven layers. When mapped on this model, the protocol and physical layer requirements specified by ISO 17458 are broken into:

- Diagnostic services (layer 7), specified in ISO 14229-1 [7], ISO 14229-4 [9];
- Presentation layer (layer 6), vehicle manufacturer specific;
- Session layer services (layer 5), specified in ISO 14229-2 [8];
- Transport layer services (layer 4), specified in ISO 10681-2 [1];
- Network layer services (layer 3), specified in ISO 10681-2 [1];
- Data link layer (layer 2), specified in ISO 17458-2, ISO 17458-3;
- Physical layer (layer 1), specified in ISO 17458-4, ISO 17458-5;

in accordance with Table 1.

Table 1 — FlexRay communications system specifications applicable to the OSI layers

Applicability	OSI 7 layers	FlexRay communications system	Vehicle manufacturer enhanced diagnostics
Seven layer according to ISO 7498-1 and ISO/IEC 10731	Application (layer 7)	vehicle manufacturer specific	ISO 14229-1, ISO 14229-4
	Presentation (layer 6)	vehicle manufacturer specific	vehicle manufacturer specific
	Session (layer 5)	vehicle manufacturer specific	ISO 14229-2
	Transport (layer 4)	vehicle manufacturer specific	ISO 10681-2
	Network (layer 3)	vehicle manufacturer specific	
	Data link (layer 2)	ISO 17458-2, ISO 17458-3	
	Physical (layer 1)	ISO 17458-4, ISO 17458-5	

Table 1 shows ISO 17458 Parts 2 – 5 being the common standards for the OSI layers 1 and 2 for the FlexRay communications system and the vehicle manufacturer enhanced diagnostics.

The FlexRay communications system column shows vehicle manufacturer specific definitions for OSI layers 3 – 7.

The vehicle manufacturer enhanced diagnostics column shows application layer services covered by ISO 14229-4 which have been defined in compliance with diagnostic services established in ISO 14229-1, but are not limited to use only with them. ISO 14229-4 is also compatible with most diagnostic services defined in national standards or vehicle manufacturer's specifications. The presentation layer is defined vehicle manufacturer specific. The session layer services are covered by ISO 14229-2. The transport protocol and network layer services are specified in ISO 10681.

Road vehicles — FlexRay communications system — Part 4: Electrical physical layer specification

1 Scope

This part of ISO 17458 specifies the electrical physical layer for FlexRay communications systems.

The electrical physical layer for FlexRay is designed for time-triggered networks with data-rates up to 10 Mbit/s to connect automotive electronic control units (ECUs). The medium that is used is dual wires. Signalling on the bus is accomplished by asserting a differential voltage between those wires. Topology variations range from point-to-point connections via linear passive busses and passive stars up to active star topologies.

This part of ISO 17458 includes the definition of electrical characteristics of the transmission itself and also documentation of basic functionality for bus driver (BD) and active star (AS) devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 17458-1, *Road vehicles — FlexRay communications system — Part 1: General information and use case definition*

ISO 17458-2, *Road vehicles — FlexRay communications system — Part 2: Data link layer specification*

3 Terms, definitions, symbols and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO 17458-1, ISO 17458-2 and the following apply.

3.1.1
alternating current busload
AC busload
equivalent circuit of a passive star from transmitting view of the bus driver

3.1.2
active elements
components which work with power supply and amplifiers

3.1.3
active star network
AS network
all *point-to-point* connections plugged to an *AS*

3.1.4
activity
See "*bus state*"
NOTE activity distinguishes two states: *Data_0* and *Data_1.*

3.1.5
Activity
signal to the Central_Logic when this *communication path* is not *idle(*see also *NoActivity)*

3.1.6
asymmetric delay budget
maximum bit-deformation in the time domain

NOTE It is derived from the specified synchronization and sampling procedure and the properties of their implementation. When transmitting a FlexRay data stream the receiving CC must be able to detect the data without any error. If the *asymmetric delay* of the data stream is higher than the *asymmetric delay budget*, the decoder samples faulty bit values.

3.1.7
asymmetric delay
bit-deformation in the time domain when passing a data stream e.g. via a *BD*

EXAMPLE

A data steam is applied to the BD´s input TxD: …00100

The single 1 at the centre shall have a length of 100 ns
The *BD* passes the data stream to its output *BP* and *BM.*
The single 1 may be shortened or lengthened a little bit to e.g. 102 ns
In this case the *asymmetric delay* has to be determined to 2 ns.

3.1.8
bus driver – bus driver interface
BD-BD-interface
consideration of all involved effects of the timing of each *BD*/*AS*

NOTE The timing is specified based on measurement set-ups easy to be used. When connecting two *BDs*/*AS*s (via e.g. a *passive star*) the resulting delays are not equal to twice the specified values.

3.1.9
bus guardian enable
BGE
input pin of the *BD that* allows deactivating the bus output stage of the *BD*

3.1.10
bias voltage
voltage source with high output impedance

3.1.11
bus minus
BM
bidirectional pin of the *BD*/*AS* to allow the *BD*/*AS* the access to the bus.

3.1.12
bus plus
BP
bidirectional pin of the *BD*/*AS* to allow the *BD*/*AS* the access to the bus.

3.1.13
branch
component within *active star topologie*s

NOTE A *branch* can be built of a *point-to-point* connection, a *linear bus* or a *passive star*.

3.1.14
byte start sequence
BSS
pre-defined sequence of two bits (logical: 10) which is sent in front of each byte

3.1.15
bus guardian
BG
component which allows the node only to transmit during the pre-defined timing slots

3.1.16
bus state
status of the bus FlexRay communication

NOTE Several different states are visible due to the operating modes of the FlexRay system.

EXAMPLE

idle: there is no communication on the bus. Approximately 0 V differential voltage is measurable.
activity: there is an on-going communication on the bus. Approximately ±600 mV up to ±1 000 mV differential voltage is measurable, etc.

3.1.17
cascade
topology character

NOTE If a topology uses more than 1 *AS* the wording "*cascaded ASs*" is used.

3.1.18
common mode
mode in which two test points are handled simultaneously against ground

EXAMPLE

common mode input impedance of the *BD*´s bus pins *BP* and *BM* to ground.
common mode voltage on the bus: ½ (*uBP* + *uBM*)

3.1.19
communication path
branches CC interface and Intra Star Interface

3.1.20
connection network
components like CMC, termination resistors, *ESD* protection circuits, lines on the *PCB*, connectors, etc

NOTE When implementing a FlexRay system each *BD*/*AS* has to be plugged to a FlexRay *cable* via these components.

3.1.21
Data_0
bus-state "*activity*"" where a logical 0 is transmitted

3.1.22
Data_1
bus-state "*activity*"" where a logical 1 is transmitted.

3.1.23
differential mode
mode in which two test points are handled against each other

EXAMPLE

differential mode input impedance of the BD´s bus pins BP and BM to ground.
differential mode voltage on the bus: (*uBP* - *uBM*).
differential mode impedance of the FlexRay *cable*

3.1.24
dummy load
summary of loads that can be applied to components which are specified by easy-to-use measurement set-ups

EXAMPLE

dummy load at *BP* and *BM*: 40 Ω || 100 pF.
dummy load at *RxD*: 15 pF

3.1.25
eye-diagram
diagram that is visible when overlying edge synchronized measured bus signals

NOTE The shape of the eye allows specifying the bus-signals.

3.1.26
frame end sequence
FES
bit sequence that consists of two bits (01) and is sent at the end of each FlexRay data frame

NOTE The asymmetric delay budget is based on the end of a data frame:
in the worst case up to 10 consecutive identical bits can be seen.
BSS + 1 byte + *FES* = 10 00000000 01

3.1.27
functional class
grouping of various features that are implemented together

NOTE The *BD*/*AS* offers various technical features. To keep the resulting products testable and to offer them a good chance on the market it is required to implement various features only together.

3.1.28
generic bus driver
simulation model which is derived from the specification directly

NOTE The knowledge about real implementations is taken into consideration. The generic *BD* supports a receiver stage, a transmitter stage and optionally the *AS* routing behaviour.

3.1.29
idle
see "*bus state*".
Idle distinguishes 3 bus biasing states:
idle while all nodes are neither un-powered nor in a low power mode, thus all nodes are biasing the bus.
idle while all nodes are either un-powered or in a low power, thus none of the nodes is biasing the bus.
idle while some nodes are biasing the bus and others not.

3.1.30
leg
passive network that is involved in the calculation of *timing budget*

NOTE A topology is interpreted as a single path from a transmitter to a receiver that contains several passive networks. Each of these passive networks is named *leg*.

3.1.31
linear passive bus
FlexRay bus that consists of 2 terminated FlexRay nodes with one *cable* between

NOTE Additionally some un-terminated FlexRay nodes are plugged to the cable by *splices* and short *stubs*.

3.1.32
monolithic
see: *active star*.

NOTE This term is used to characterize various implementations on an *AS*. If the *AS* is *monolithic* implemented all specified components are included in a single device.

3.1.33
NoActivity
signal to the Central_Logic when this communication path is *idle* is detected (see also *Activity)*

3.1.34
non-monolithic
character of various implementations on an *AS*

NOTE This term is used to characterize various implementations on an *AS*. If the *AS* is *non-monolithic* implemented all specified components are not included in a single device, two devices are used at least. See "*active star*".

3.1.35
NotReceiveActive
communication path signals *NotReceiveActive* to the Central_Logic when a state is entered at that the *communication path* is idle or is actively transmitting data

3.1.36
parasitic capacity
capacity that appears although it is not technically necessary

EXAMPLE

pins of a device housing generate a capacity

3.1.37
parasitic resistance
resistance that appears although it is not technically necessary

3.1.38
passive net
all possible implementation of *AS branches*

NOTE This summarizes: point-to-point connections, linear busses and passive stars. They do not include *BD*/*AS*s.

3.1.39
passive star network
network consisting of passive stars

3.1.40
physical layer
component that includes all components between *TP0* and *TP5*

3.1.41
ReceiveActive
communication path signals *ReceiveActive* to the Central_Logic when a state is entered at that the incoming data stream is forwarded to other *communication paths*

3.1.42
receiver
device or entity that receives an information transfer originated by a transmitter

NOTE A term that is used in various ways based on the context.

EXAMPLE

BD´s input stage from the bus.
FlexRay *communication element* receiving node

3.1.43
receive enable not
RxEN
output pin at the *BD* to show the state of the bus

NOTE Two states are distinguished: *idle* or *activity*

3.1.44
serial peripheral interface
SPI
synchronously working hardware interface to exchange data among circuits mounted on a *PCB*

3.1.45
signal integrity
SI
procedures or requirements to *differential* bus signals to guarantee the faultless transmission of FlexRay *communication elements*

3.1.46
signal integrity voting
SI voting
procedure to determine *Sq* based on measured *bus* signals

3.1.47
specific line delay
propagation of a FlexRay signal per meter of a transmission line in ns/m

3.1.48
splice
any implementation of a connection-point where 3 or more transmission lines are plugged together

NOTE A *splice* may contain passive components to damp radiation

EXAMPLE

A *splice* in a linear bus allows to connect a stub to a FlexRay node.

3.1.49
signal quality
Sq
parameter to describe whether the required *signal integrity* of FlexRay signals on the bus is met

NOTE Pass or fail are the possible results.

3.1.50
stochastic jitter
jitter of data stream edges in the time domain due to e.g. radiation

NOTE The EPL-specification passes its appropriate consideration to the responsible system designer.

3.1.51
stub
component within *passive net*s

NOTE A *stub* consists of a single FlexRay *cable* connected to the centre of a passive star or to a linear bus (short: plugged to a *splice*).
The *stub* ends at the BD pins BP and BM within a FlexRay node.

3.1.52
termination
set-up of components between a BD and a *transmission line*

NOTE Mainly they are used to ensure *SI* and *EMC* requirements.

EXAMPLE

Resistors, capacitances, chokes etc.

3.1.53
termination area (of the cables)
assembly of FlexRay *cables* to *ECU*-connectors that require several procedures which disturb the geometric integrity of the FlexRay *cable*:
untwisted, unshielded and unsheathed *cable* segment,
twisted but unshielded or unsheathed *cable* segment.
Both segments together represent the termination area.

3.1.54
test plane
virtual or real places to get electrical signals and to determine their properties

NOTE The *test planes* are located on the path from a transmitter to a receiver.

3.1.55
topology
non-hierarchical flat geometric structure of the FlexRay system

NOTE A distributed FlexRay system consists of several components like nodes, busses, active and passive stars etc.

3.1.56
test plane 0
TP0
virtual time reference point that represents the digital output from the protocol machine with a perfect timing according the data link layer specification

3.1.57
test plane 1 flip flop (virtual)
TP1_FFi
transmitting CC's virtual test plane to visualize PLL jitter, clock skew and propagation delay of the flip flop

3.1.58
test plane 1 flip flop
TP1_FF
transmitting CC's internal test plane at 'Q' pin of last flip flop before output buffer

3.1.59
test plane 1 communication controller
TP1_CC
transmitting CC's output pin (TxD)

3.1.60
test plane 1 bus driver input
TP1_BD
test plane located at the transmitting *BD*'s input pin *TxD* directly

3.1.61
test plane 1 bus driver (virtual)
TP1_BDi
virtual test plane hidden in the transmitting *BD*'s output of its *TxD* logical state detection stage

3.1.62
test plane 1
TP1
test plane located at the transmitting *BD*'s output pins *BP* and *BM*

3.1.63
test plane 2
TP2
test plane located at the transmitting *ECU* connector's terminals to the wiring harness

3.1.64
test plane 3
TP3
test plane located at the receiving *ECU* connector's terminals from the wiring harness

3.1.65
test plane 4
TP4
test plane located at the receiving *BD's* input pins *BP* and *BM*

3.1.66
test plane 4 bus driver (virtual)
TP4_BDi
virtual test plane hidden in the receiving *BD*'s output of its differential bus signal logical level detection stage

3.1.67
test plane 4 bus driver
TP4_BD
receiving BD's output pin (RxD)

3.1.68
test plane 4 communication controller
TP4_CC
test plane located at the receiving *CC*'s input pin *RxD*

3.1.69
test plane 4 communication controller (virtual)
TP4_CCi
virtual test plane hidden in the receiving *CC*'s output of its *RxD* logical state detection stage

3.1.70
test plane 4 flip flop
TP4_FF
receiving CC's internal test plane at 'D' pin of first flip flop after input buffer

3.1.71
test plane 4 flip flop (virtual)
TP4_FFi
receiving CC's virtual test plane to visualize PLL jitter, clock skew and propagation delay of the flip flop

3.1.72
test plane 5 communication controller
TP5_CC
clock input to CC

3.1.73
test plane 5
TP5
virtual test plane that represents the input of the decoding algorithm with a perfect timing according the data link layer specification

3.1.74
test plane 11
TP11
test plane located at the transmitting *AS* device's output pins *BP* and *BM*

3.1.75
test plane 12
TP12
test plane located at the transmitting *AS ECU* connector's terminals to the wiring harness

3.1.76
test plane 13
TP13
test plane located at the receiving *AS ECU* connector's terminals from the wiring harness

3.1.77
test plane 14
TP14
test plane located at the receiving *AS* device's input pins *BP* and *BM*

3.1.78
transmission line
FlexRay *cable* or a line on a PCB when their properties to transmit electrical signals are focused

3.1.79
transmission start sequence
TSS
bit sequence that is sent in front of each FlexRay data frame or CAS/MTS symbol. The *TSS* is necessary for a *BD* and an *AS* to detect *activity* on the bus. A *BD* and an *AS* is allowed to shorten or lengthen the *TSS*.

3.1.80
transmitter
term that is used in various ways based on the context

EXAMPLE

BD´s output stage to the bus.
FlexRay traffic transmitting node

3.1.81
wiring harness
all components inside the component "vehicle wiring harness" to transmit FlexRay *communication elements*

NOTE This includes connectors to plug *ECU*s, in-line connectors, *cables*, *splices* etc.

3.2 Abbreviated terms

AC	alternating current
APM	autonomous power moding
AS	active star
AS_BGI	active star – bus guardian interface
AS_IVR	active star – internal voltage regulator
AS_VRC	active star – voltage regulator control
ASP	abstract service primitive
BD	bus driver
BD_VRC	bus driver – voltage regulator control
BD_BGCI	bus driver – bus guardian control interface
BD_IVR	bus driver – internal voltage regulator
BD_LLA	bus driver – logic level adaptation
BG	bus guardian
BGE	bus guardian enable
BM	bus minus
BP	bus plus
C	capacitor
CC	communication controller
CE	communication element
CHI	controller host interface
CMC	common mode choke
DUT	device under test
ECU	electronic control unit
EMC	electromagnetic compatibility
EN	optional/product specific mode control signals of the bus driver
ERRN	error not output pin of the *BD*/*AS* This pin allows the *BD*/*AS* signalling error events or/and errors.
I/R	interruption
Idle_LP	bus state in case all nodes (and active stars) are in a low power mode

INH — inhibit output pin of the *BD*/*AS*
INH signals on one hand the *BD*/*AS* state and allows on the other hand to control the states of a voltage regulator.

INH1 — inhibit 1 output signal of the bus driver / active star

INTN — interrupt not

IUT — implementation under test

LWU — local wakeup

PCO — point of control and observation

PDU — protocol data unit

PL — physical layer

PS — passive star

RWU — remote wakeup

RxD — receive data signal from the bus driver

RxEN — receive data enable not signal from the bus driver

S/C — short-circuit

SCSN — SPI chip select not input

SI — signal integrity

SOVS — system operating variable space

SPI — serial peripheral interface

Sq — signal quality

STBN — standby not
Input pin at the *BD* to control its power modes

SUT — system under test

SV — supervisor

TCP — test coordination procedure

TP — test plane

TSS — transmission start sequence

TxD — transmit data signal to the bus driver

TxEN — transmit data enable not signal
Output pin at the *CC* and input pin at the *BD*. The pin allows the *CC* to control the states which are generated by the *BD*. Two states are distinguished: *idle* or *activity*.

U_{GS} — ground shift voltage

WAKE local wakeup input signal of the bus driver

WU wakeup

3.3 Symbols

R_T Resistor to terminate a transmission line

X don't care. This term is used when the state of a signal is not relevant.

V_{BAT} supply voltage (battery)
Voltage of the vehicle battery measurable at *BD*´s pins.

V_{CC} supply voltage (+5 V)

V_{DIG} supply voltage for the digital I/O ports
This term is used in two ways, *BD*´s pin to connect the logical 1 reference voltage and voltage value of the logical 1 reference voltage.

V_{IO} supply voltage for the digital I/O ports
This term is used in two ways, *BD*´s pin to connect the logical 1 reference voltage and voltage value of the logical 1 reference voltage.

$V_{StarSupply}$ supply voltage of the active star
Can be derived from V_{BAT} and/or V_{CC}

4 Document reference according to OSI model

Figure 1 depicts the FlexRay document reference according to OSI model.

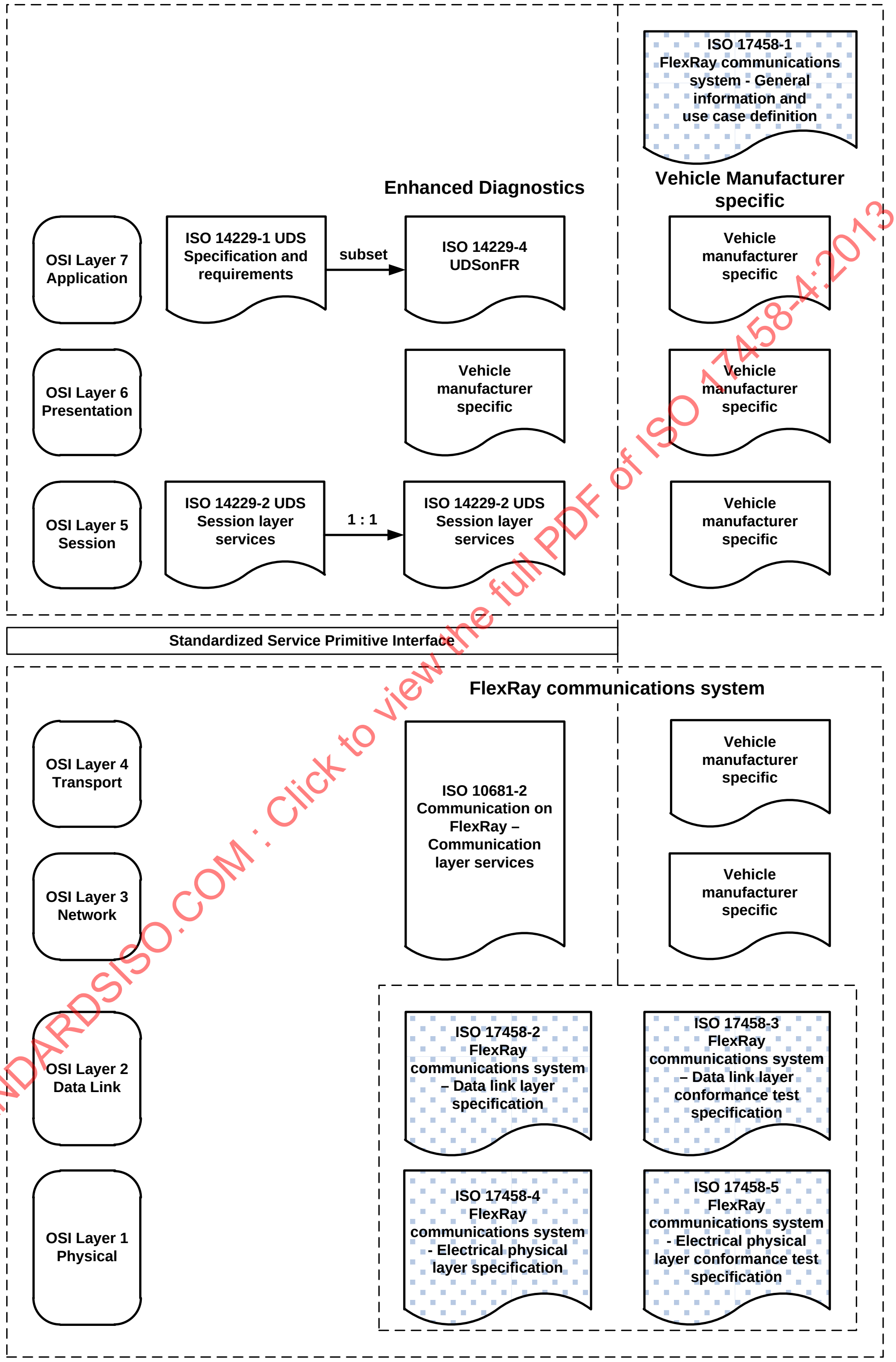


Figure 1 — FlexRay document reference according to OSI model

5 Conventions

5.1 General

ISO 17458, ISO 10681 and ISO 14229-4 are based on the conventions specified in the OSI Service Conventions (ISO/IEC 10731) as they apply for physical layer, protocol, network & transport protocol and diagnostic services.

5.2 Notational and parameter prefix conventions

Each FlexRay parameter is prefaced by two prefixes. The prefixes are applied in the following way:

<variable> ::= <prefix_1> <prefix_2> Name

<prefix_1> ::= a | c | v | g | p | z

<prefix_2> ::= d | l | n | s | u

Table 2 defines the values for prefix 1.

Table 2 — Prefix 1

Naming Convention	Information Type	Description
a	Auxiliary Parameter	Auxiliary parameter used in the definition or derivation of other parameters or in the derivation of constraints.
c	Protocol Constant	Values used to define characteristics or limits of the protocol. These values are fixed for the protocol and cannot be changed.
v	Node Variable	Values that vary depending on time, events, etc.
g	Cluster Parameter	Parameter that shall have the same value in all nodes in a cluster, is initialized in the *POC:default config* state, and can only be changed while in the *POC:config* state.
p	Node Parameter	Parameter that may have different values in different nodes in the cluster, is initialized in the *POC:default config* state, and can only be changed while in the *POC:config* state.
z	Local SDL Process Variable	Variables used in SDL processes to facilitate accurate representation of the necessary algorithmic behaviour. Their scope is local to the process where they are declared and their existence in any particular implementation is not mandated by the protocol.
—	—	*prefix_1* can be omitted for physical layer parameters.
NOTE This table is mirrored from ISO 17458-2, where the binding definitions are made.		

Table 3 defines the values for prefix 2.

Table 3 — Prefix 2

Naming Convention	Information Type	Description
d	Time Duration	Value (variable, parameter, etc.) describing a time duration, the time between two points in time.
l	Length	Physical length of e.g. a cable
n	Amount	Number of e.g. stubs
s	Set	Set of values (variables, parameters, etc.).
u	Voltage	Differential voltage between two conducting materials (e.g. copper wires)
NOTE The prefixes "l", "n" and "u" are defined binding here. For all other prefixes refer to ISO 17458-2.		

5.3 Important preliminary notes

5.3.1 Bus speed

The FlexRay communication system was specified focusing on a data rate of 10 Mbit/s.

This physical layer shall only be used for data rates in the range from 2,5 Mbit/s to 10 Mbit/s.

NOTE The 500 ppm crystal is used to allow electrical physical layer including one active star at 10 Mbit/s. The 1 500 ppm crystal is used to estimate the worst case clock accuracies etc. at any baud rate in ISO 17458-2.

5.3.2 Conformance tests

The conformance test for physical layer devices as specified in this specification is defined in ISO 17458-5.

For the static test cases of the conformance test every EPL parameter shall be pointed out in the BD/AS data sheet by using the EPL-naming conventions (optionally according to in-house naming convention) and the EPL measurement conditions.

In case other than the EPL parameter names are used, the data sheet shall contain a comparison table including the parameter names (EPL versus product) and the values. A proposal for such a table is given in ISO 17458-5.

5.3.3 Conformance test of FlexRay communication controllers

The test of the CC interface to the physical layer as specified in Clause of this part of ISO 17458 is part of the protocol conformance test.

6 Communication channel basics

6.1 Objective

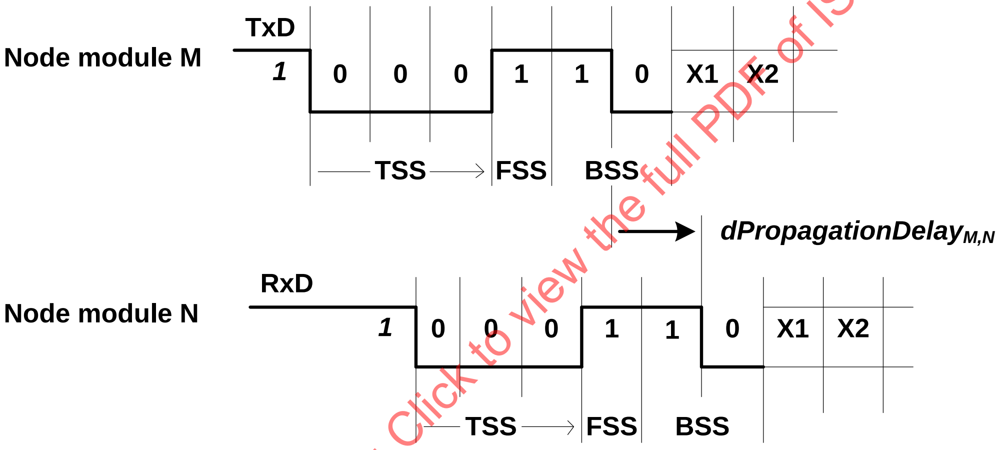
The electrical physical layer provides among other things an implementation of a FlexRay communication channel. This subclause defines an abstract of the physical properties of the communication channel.

Any physical layer that behaves according to these basics provides a valid FlexRay communication channel.

6.2 Propagation delay

Binary data streams transmitted from node module M are received at node module N with the propagation delay $dPropagationDelay_{M,N}$. The propagation delay shall be measured from the falling edge in the first Byte Start Sequence (BSS; see ISO 17458-2) in the transmit (TxD, TP1_BD) signal of node module M to the corresponding falling edge in the receive (RxD, TP4_BD) signal of node module N.

Figure 2 depicts the propagation delay.



Key

BSS	Byte start sequence
FSS	Frame start sequence
TSS	Transmission start sequence
TxD	Transmission
RxD	Reception

Figure 2 — Propagation delay

The actual propagation delay that occurs between two node modules M and N depends mainly on the topology of the path.

Table 4 defines the propagation delay.

Table 4 — Propagation delay

Name	Description	Min	Max	Unit
$dPropagationDelay_{M,N}$	Propagation delay from TP1_BD [a] of node module M to TP4_BD [a] of node module N	—	2 450	ns

[a] For definition of "TP1_BD" and "TP4_BD", see Clause 10.

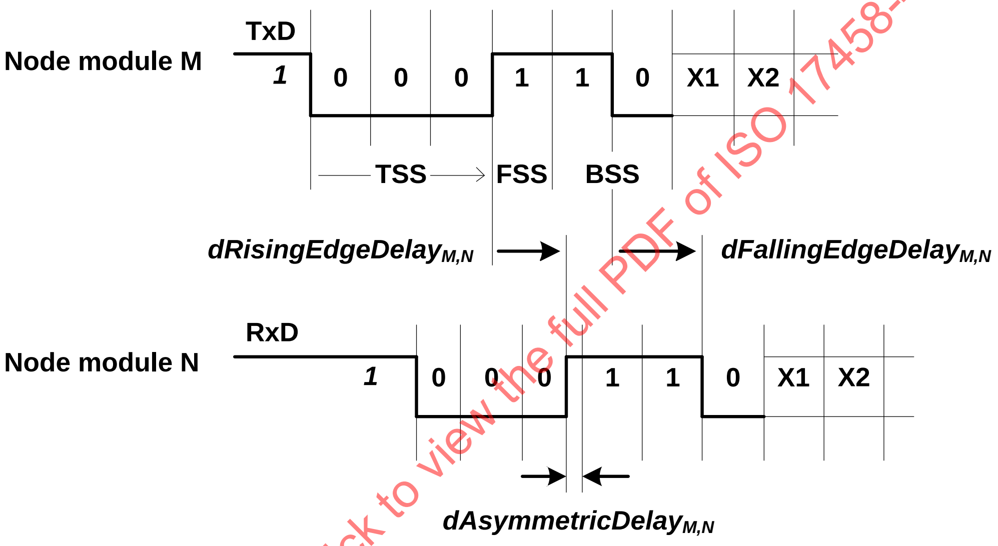
6.2.1 Asymmetric delay

As defined above the propagation delay is defined with in relation to the first negative edge after the TSS in the binary data stream.

Due to the limitations of the FlexRay decoder module the channel plus the sending and receiving bus driver shall not introduce a static asymmetric delay that exceeds a certain level.

Definitions of maximum asymmetric delay portions can be found in 10.5. For further considerations see Annex A.

Figure 3 depicts the asymmetric propagation delay.



Key

BSS Byte start sequence

FSS Frame start sequence

TSS Transmission start sequence

TxD Transmission

RxD Reception

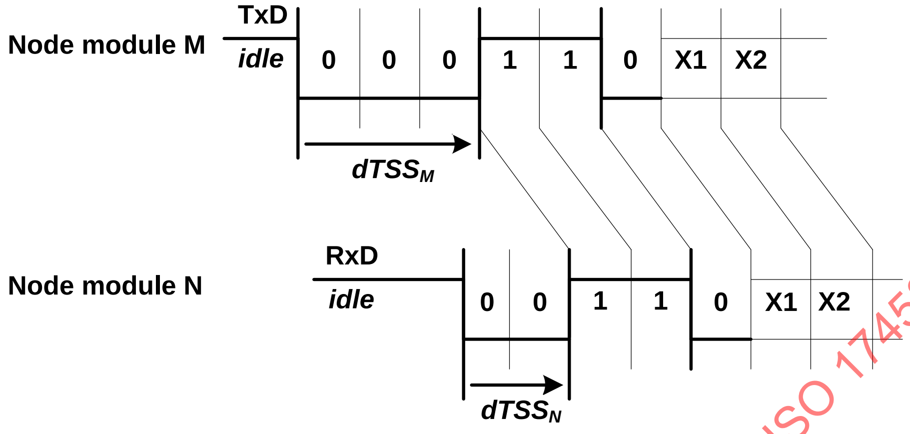
Figure 3 — Asymmetric propagation delay

$$dAsymmetricDelay_{M,N} = dRisingEdgeDelay_{M,N} - dFallingEdgeDelay_{M,N}$$

In case the rising edge is late, relative to the falling edge, the resulting asymmetry has a positive sign.

6.3 Frame TSS length change

The channel may truncate the TSS (see ISO 17458-2), but also may slightly lengthen the TSS. The interval by which the TSS length is changed from a transmitting node module M to a receiving node module N is denoted as $dFrameTSSLengthChange_{M,N}$. The effect of Frame TSS length change is shown in Figure 4.



Key

TxD Transmission

RxD Reception

Figure 4 — Frame TSS length change

The length change is calculated as the difference of the duration of TSS at the receiver and duration of TSS at the sender: $dFrameTSSLengthChange_{M,N} = dTSS_N - dTSS_M$. Thus positive values would indicate that the TSS was lengthened.

The absolute maximum value of $dFrameTSSLengthChange_{M,N}$ needs to be less than the maximum configurable value of the protocol parameter *gdTSSTransmitter*. The effect of TSS length change sums up of different portions, which are contributed by active stars and the activity detection in the receiving bus drivers.

Table 5 defines the frame TSS length change.

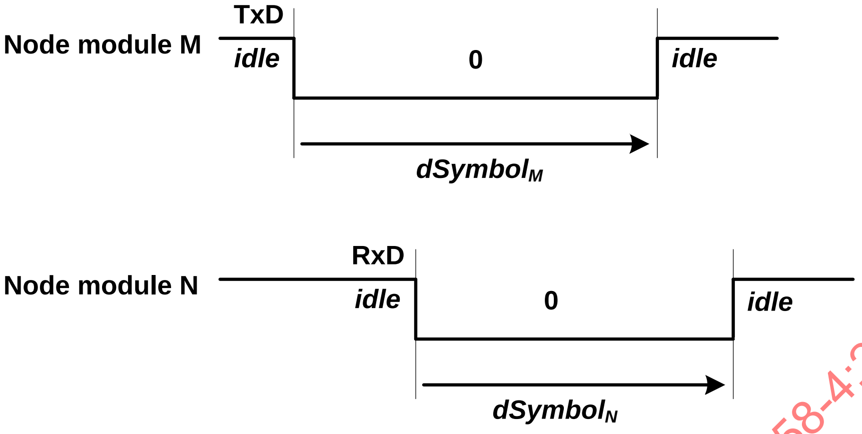
Table 5 — Frame TSS length change

Name	Description	Min	Max	Unit
$dFrameTSSLengthChange_{M,N}$	TSS Length change from TP1_BD [a] of node module M to TP4_BD [a] of node module N	-1300	50	ns
NOTE The TSS length change depends on the number of active stars in the path from node M to node N. More detailed information is given in Annex A.				
[a] For definition of "TP1_BD" and "TP4_BD", see Clause 10.				

6.4 Symbol length change

Quite similar to the length change of the TSS the length of symbols is changed while travelling through the physical layer. Besides the length change at the beginning by the activity detection time a lengthening at the end by the idle detection time occurs. More detailed information is given in Annex A.

Figure 5 depicts the symbol length change.



Key

TxD Transmission

RxD Reception

Figure 5 — Symbol length change

The length change is calculated as the difference of the duration of the symbols at the receiver and duration of the symbol at the sender: $dSymbolLengthChange_{M,N} = dSymbol_N - dSymbol_M$.

Table 6 defines the symbol length change.

Table 6 — Symbol length change

Name	Description	Min	Max	Unit
$dSymbolLengthChange_{M,N}$	Change of length of a symbol on path from TP1_BD [a] of node module M to TP4_BD [a] of node module N	-925	1 125	ns
NOTE A negative value means that the symbol is shortened; a positive value means the symbol is lengthened.				
[a] For definition of "TP1_BD" and "TP4_BD", see Clause 10.				

6.5 FES1 length change

The last two bits in a FlexRay frame are called FES (Frame End Sequence). The last bit (FES1) is logical HIGH. This period of the FES1 is likely to be lengthened by active stars. For detailed information see 13.3. Besides the prolongation of the FES1 there is the chance that ringing occurs. For further information about ringing after frame and symbol end see Annex A.

6.6 Collisions

FlexRay is designed to perform communication without collisions. I.e. the nodes do not arbitrate on the channel and collisions do not happen during normal operation. However, during the startup phase of the protocol, collisions on the channel may happen. The electrical physical layer does not provide a means to resolve those collisions.

In case of collisions of communication elements on the bus (at least two nodes are transmitting different data simultaneously) it cannot be predicted what signal the nodes will receive. The received bus signal can also change within one bit time.

Table 7 defines the data signal collision on the bus.

Table 7 — Data signal collision on the bus

Transmitter 1	Transmitter 2	Resulting bus signal
Data_0	*Data_0*	*Data_0*
Data_0	*Data_1*	*Data_0* or *Data_1* or *Idle*
Data_1	*Data_0*	*Data_1* or *Data_0* or *Idle*
Data_1	*Data_1*	*Data_1*
Idle	*Data_0/Data_1*	*Data_0/Data_1*
Data_0/Data_1	*Idle*	*Data_0/Data_1*
NOTE For the definitions of *Data_0*, *Data_1 and Idle* see Clause 6.		

6.7 Stochastic jitter

6.7.1 Introduction

Injection of RF fields results in a certain jitter portions seen in the RxD signal at receiving nodes. These different portions have been investigated and the results for systems with two active stars per channel are documented in the following subclauses. These values are not subject to the physical layer conformance test.

6.7.2 Stochastic jitter on data edges

Jitter on edges in the RxD signal, which are different from first transition from HIGH to LOW (start of frame) and the last transition from LOW to HIGH (the end of a frame), shall be considered in the course of system evaluation. See Annex A for further information about the allowable EMC jitter in specific network topologies.

6.7.3 Stochastic jitter on TSS length change

Jitter on the TSS length might lengthen or shorten the TSS additionally to the length change as described in 6.3. Further information is given in Annex A.

6.7.4 Stochastic jitter on symbol length change

The summation of jitter on the falling and rising edges of symbols might lead to deviations of the symbol length change as described in 6.4. Further information is given in Annex A.

6.8 Wakeup patterns

6.8.1 Overview

Independent from the data rate at least two wakeup symbols constitute a wakeup pattern. Such patterns shall wake bus drivers that implement the option ‘BD voltage regulator control’ and active stars that are in a low power mode.

6.8.2 Standard wakeup pattern

For remote wakeup in FlexRay systems, a wakeup pattern is sent via the bus as described in ISO 17458-2. The FlexRay wakeup pattern consists of at least two FlexRay wakeup symbols.

The wakeup symbol is defined as a phase of *Data_0* followed by a phase of *Idle*.

A valid remote wakeup event is the reception of at least two consecutive wakeup symbols via the bus.

A remote wakeup event occurs from bus drivers or active stars perspective when any sequence of

{ *Data_0*, *Idle*, *Data_0*, *Idle* }

that starts after *Idle* and has a timing according to Figure 6 is received.

The receiver shall detect wakeup patterns with the timing:

dWU_{Phase0} > 4 µs, dWU_{Phase1} > 4 µs, dWU_{Phase2} > 4 µs, dWU_{Phase3} > 4 µs, dWU_{Phase4} > 4 µs and *dWU* < 49 µs.

The dWU consists of the minimum value for the detection timeout of the Data_0 phase $dWU_{0Detect}$ (which is 1 µs) and the minimum of the wakeup acceptance timeout $dWU_{Timeout}$ (which is 48 µs). A detailed description of the wakeup mechanism is given in 12.11.3.

Figure 6 depicts the valid signal for wakeup pattern recognition at receivers.

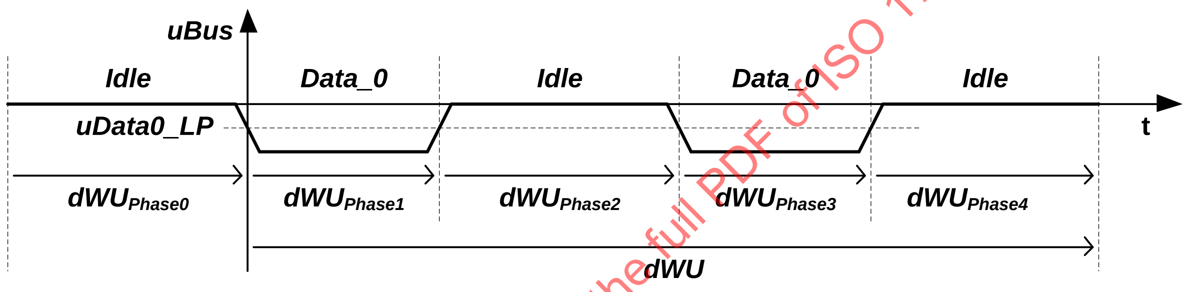


Figure 6 — Valid signal for wakeup pattern recognition at receivers

6.8.3 Alternative wakeup patterns

Other patterns as the above mentioned will also let the wakeup state machine (see 12.11.3) initiate a wakeup.

In the WUDOP ISO 17458-2 wakeup pattern the *Idle* phases of the standard wakeup pattern are replaced by *Data_1* phases. The timing requirements do not change. Such patterns can advantageously be used during the symbol window.

Figure 7 depicts the alternative wakeup pattern recognition at receivers.

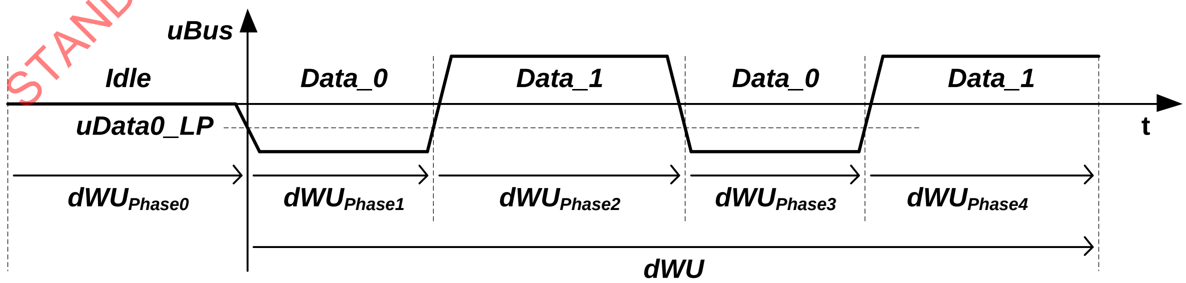


Figure 7 — Alternative wakeup pattern recognition at receivers

7 Principle of FlexRay networking

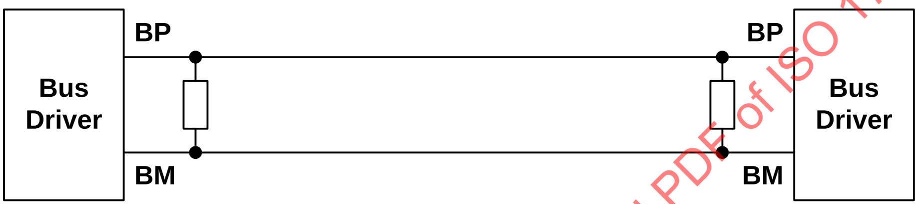
7.1 Objective

This Clause shows the basic operation principle of FlexRay networks.

7.2 Interconnection of nodes

The FlexRay electrical physical layer provides a differential voltage link (= bus) between a transmitting and one or more receiving communication modules. The differential voltage is measured between two signal lines, denoted BP (Bus Plus) and BM (Bus Minus) as defined in 7.3. The fundamental mechanism of the bidirectional differential voltage link is shown below. The bidirectional link between any two node modules requires a transmitter and receiver circuit, which are integrated in so called bus drivers.

Figure 8 depicts the principle of a differential voltage link.



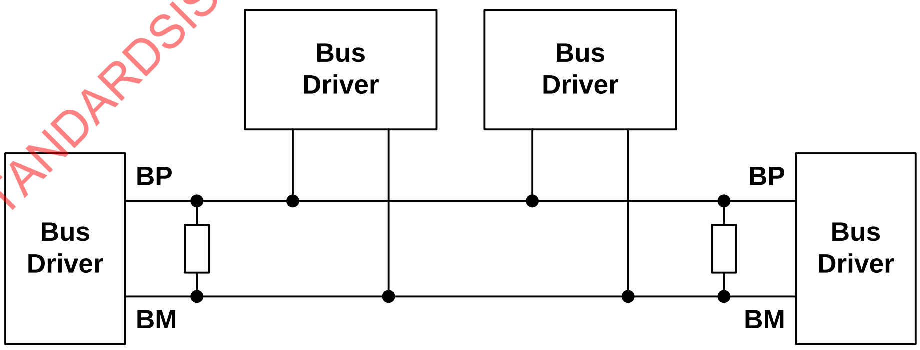
Key

BM Bus plus

BP Bus minus

Figure 8 — Principle of a differential voltage link

This structure, which is named ‘point-to-point connection’ in Clause 9, can be extended with further bus drivers that are connected to the differential voltage link as depicted in Figure 9. A dual wire cable implements the differential voltage link. With each communication module one bus driver is added to the system, as shown in Figure 9.



Key

BM Bus minus

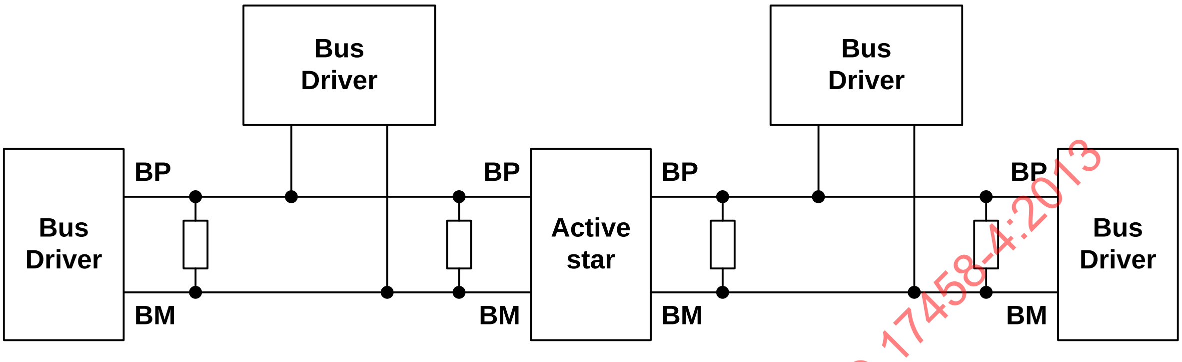
BP Bus plus

Figure 9 — Principle of a linear passive bus

The complete variety of possible topologies is defined in Clause 9.

Furthermore, the bus can also comprise active stars, which are working in principle as bidirectional repeaters. The functionality of active stars is specified in Clause 13.

Figure 10 depicts the principle of an active star network.



Key

BP Bus Plus

BM Bus Minus

Figure 10 — Principle of an active star network

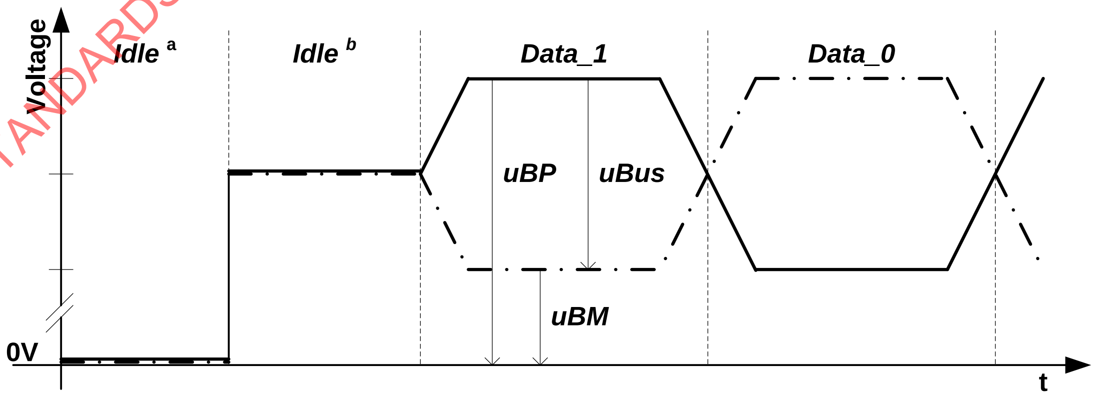
7.3 Electrical signalling

7.3.1 Overview

The bus may assume three different bus states, denoted as *Data_0*, *Data_1* and *Idle*.

A principle voltage level scheme is depicted in the following figure. The bus wires are denoted as BP and BM. Consequently the voltages on the wires (measured to ground) are denoted *uBP* and *uBM*. The differential voltage on the bus is defined as *uBus* = *uBP* - *uBM*.

Figure 11 depicts the electrical signalling.



a In case all nodes (and active stars) are in a low power mode

b in case no node (and no active star) is in a low power mode

Figure 11 — Electrical signalling

7.3.2 Bus state: Idle

To leave the bus in *Idle* state, no current is actively driven to BP or to BM. The connected bus drivers are biasing both BP and BM to a certain voltage level depending on their operating mode (see Table 49), i.e. in case all nodes (and active stars, if connected) are in a low power mode no bias voltage is applied to the bus wires. In case no node (and no active star, if connected) is in a low power mode the nominal bias voltage is 2 500 mV.

In case some of the nodes are in a low power mode and others are not, the resulting bias voltage on the bus wires will be less than 2 500 mV.

7.3.3 Bus state: Data_1

To drive the bus to *Data_1* at least one BD forces a positive differential voltage between BP and BM.

7.3.4 Bus state: Data_0

To drive the bus to *Data_0* at least one BD forces a negative differential voltage between BP and BM.

Figure 12 depicts the differential electrical signalling.

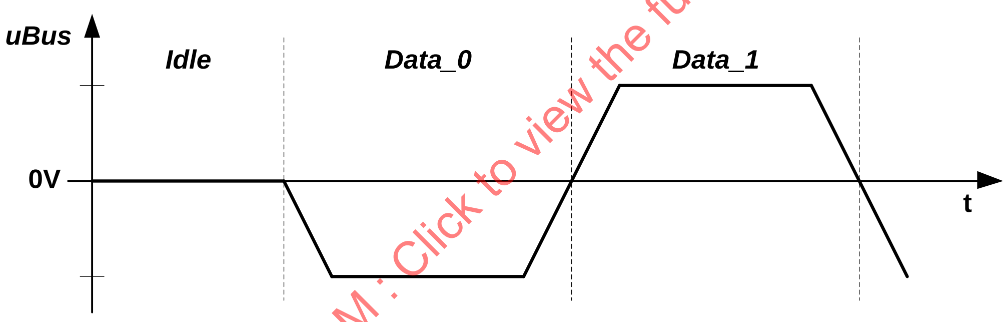


Figure 12 — Differential electrical signalling

8 Network components

8.1 Objective

This Clause introduces some basic network components that are used to build up FlexRay networks.

8.2 Cables

The objective of this subclause is to specify the required cable characteristics, but not to define a selection of cable types. The medium in use for FlexRay busses may be unshielded as well as shielded cables, as long as they provide the characteristics defined in Table 8.

Table 8 — Cable characteristics

Name	Description	Min	Max	Unit
Z_0	Differential mode impedance at 10 MHz [a]	80	110	Ω
T'_0	Specific line delay	3,4	10	ns / m

a See Annex A.

Cable attenuation and delay depend on temperature and frequency, but might also depend on more environmental conditions. The system integrator has to select the cable so that the receiver requirements at TP4 are fulfilled.

8.3 Connectors

This specification does not prescribe certain connectors for FlexRay systems. However, any electrical connector used in FlexRay busses shall meet the constraints defined in Table 9.

Table 9 — Connector parameters

Name	Description	Min	Max	Unit
$R_{DCContact}$	Contact resistance (including crimps)	—	50	mΩ
$Z_{Connector}$	Impedance of connector	70	200	Ω
$l_{Coupling}$	Length coupling connection [a]	—	150	mm
dContactInterruption [b]	Duration of contact interruption. Contact resistance $R_{DCContact} > 1\ \Omega$	—	100	ns

NOTE See further recommendations about connectors in Annex A.

a this parameter defines the length of the connectors including the termination areas of the cables.

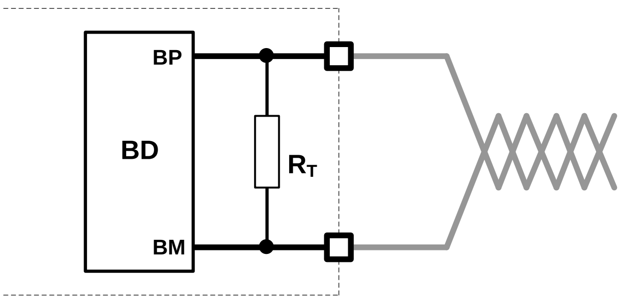
b this requirement is to be generally understood as a quality issue and has no direct link with the timing performance of FlexRay.

8.4 Cable termination

8.4.1 Terminated cable end

The simplest way to terminate the cable at an ECU consists of a single termination resistor between the bus wires BP and BM. Other termination possibilities are shown in Annex A.

Figure 13 depicts the terminated cable end.



Key

BD Bus driver

BM Bus minus

BP Bus plus

R_T Termination resistance

Figure 13 — Terminated cable end

In following subclauses, ECUs that have this kind of termination are symbolized with the following icon.

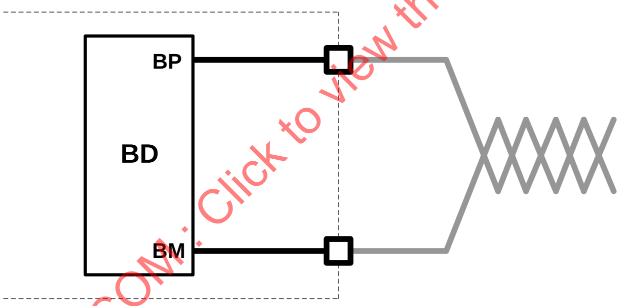
Figure 14 depicts the symbol for a terminated cable end.

Figure 14 — Symbol for a terminated cable end

8.4.2 Un-terminated cable end

At an un-terminated cable end, no resistive element is connected between the bus wires.

Figure 15 depicts the un-terminated cable end.



Key

BD Bus driver

BM Bus minus

BP Bus plus

Figure 15 — Un-terminated cable end

In the following subclauses, ECUs that have this kind of termination are symbolized with the following icon.

Figure 16 depicts the symbol for an un-terminated cable end.

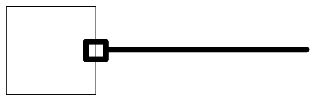


Figure 16 — Symbol for an un-terminated cable end

8.5 Termination concept

This specification does not prescribe a certain termination concept. Application specific solutions have to be applied. Some more general recommendations about cable termination can be found in Annex A.

8.6 Common mode chokes

This specification does not prescribe a certain common mode choke for FlexRay systems. However, any common mode choke used in FlexRay systems shall meet the following constraints over the entire temperature range as specified in 15.7.

Table 10 defines the common mode choke parameters.

Table 10 — Common mode choke parameters

Name	Description	Min	Max	Unit
R_{CMC}	Resistance (per line)	—	2	Ω

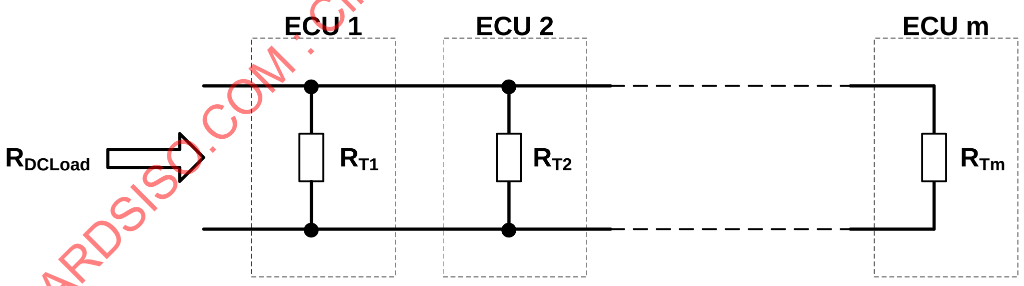
See further recommendations about common mode chokes in Annex A.

8.7 DC bus load

The DC load a BD sees between the bus wires is R_{DCLoad}.

A network equivalent DC circuit is as follows:

Figure 17 depicts the DC bus load.



Key

ECU Electronic control unit / FlexRay node

R_{DCLoad} Resistance of the DC bus load

R_T Termination resistance

Figure 17 — DC bus load

The schematic does not include parasitic resistances from common mode chokes (R_{CMC}), connectors ($R_{Connector}$) and the series resistance of the wiring (R_{Wire}), since those shall be neglected in the following calculation:

The formula to calculate the overall DC bus load is shown in Equation 1.

$$R_{DCLoad} = \left(\sum_{m} \frac{1}{R_{Tm}} \right)^{-1} \quad (1)$$

where

R_{DCLoad} is the DC bus load;

R_{Tm} is the termination resistance of ECU m.

Table 11 defines the DC bus load limitation.

Table 11 — DC bus load limitation

Name	Description	Min	Max	Unit
R_{DCLoad}	DC bus load	40	55	Ω

Mind that the termination resistance R_{Tm} is usually a termination resistor in parallel to the BD's receiver common mode input resistance (see 12.9.5). The termination resistor might also be applied outside the ECU, e.g. at a network splice. In case of an un-terminated cable end, according to 8.4.2., the resistance R_{Tm} represents only the BD's receiver common mode input resistance.

Some exemplary termination concepts for different bus structures are described in Annex A. All termination concepts have to consider the DC bus load limitation as defined here.

9 Network topology

9.1 Objective

This Clause introduces possible bus structures, their names and parameters. The layout of busses has to follow the constraints that are explained in this Clause. Application examples and recommendations are given in Annex A.

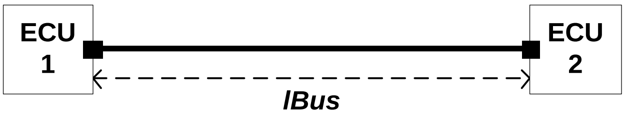
Dual channel applications, a main feature of FlexRay, are discussed at the end of this Clause.

All FlexRay topologies are 'linear', which means that they are free from rings or closed loops respectively.

A termination concept has to be found for each topology implementation individually. General hints can be found in Annex A. Whether a topology/termination combination composes a valid FlexRay network, or not, has to be judged according to the signal integrity requirements as given in Clause 11.

9.2 Point-to-point connection

The point-to-point configuration is shown in Figure 18. It represents the simplest bus and can be regarded as the basic element for the construction of more complex busses. For simplicity, the two-wire bus is shown as one thick line in the figures of this document.



Key

ECU Electronic control unit / FlexRay node

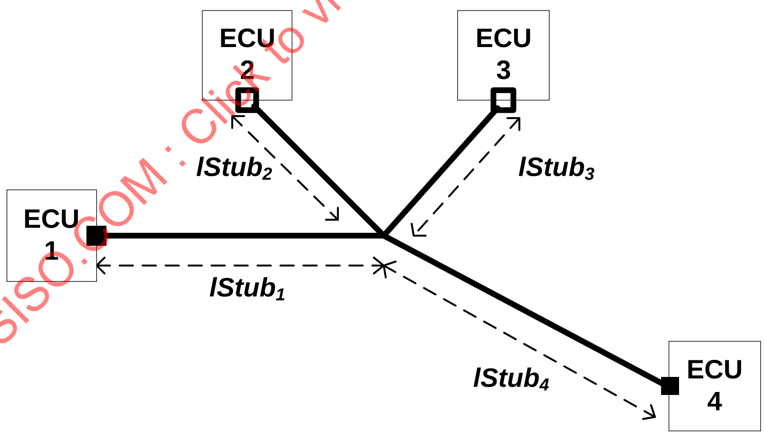
Figure 18 — Point-to-point connection

Practical limitations for *lBus* depend on factors like cable type and EMC disturbances.

Examples of practical values are given in Annex A, where also consideration about EMC robustness can be found in a separate subclause.

9.3 Passive star

For connecting more than two ECUs a passive star structure can be used, which is a special case of a linear passive bus that is described in the following subclause. At a passive star all ECUs are connected to a single splice. The principle of a passive star network is shown in Figure 19.



Key

ECU Electronic control unit / FlexRay node

Figure 19 — Example of a passive star

Table 12 defines the parameters of a passive star.

Table 12 — Parameters of a passive star

Name	Description	Min	Max	Unit
nSplice	Number of splices [a]	1	1	—
[a] If *nSplice* is 0, then refer to 9.2, if *nSplice* is greater than 1, then refer to 9.4.				

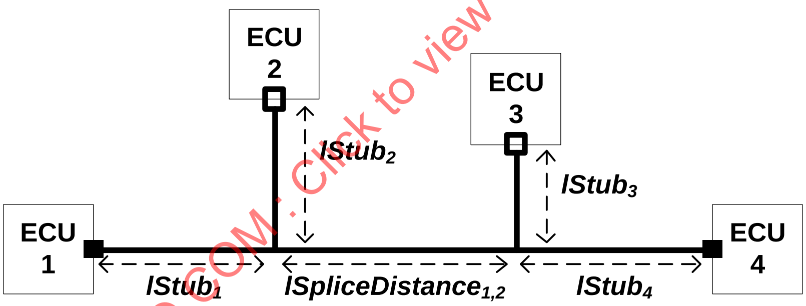
Practical limitations for *nStub* and $lStub_N$ depend on each other and depend also on other factors like cable type and termination concept; i.e. a passive star with *nStub* = 22 and each *lStub* = 12 m for each stub is likely not to be operable.

Examples of practical values are given in Annex A, where also consideration about EMC robustness can be found in a separate subclause.

9.4 Linear passive bus

A structure without rings and without active elements is called "linear passive bus". The number of stubs is *nStub*. The length of a stub is $lStub_i$. The bus distance between two splices is denoted as $lSpliceDistance_{M,N}$. More than one stub may end at one splice. The number of splices is *nSplice*.

Figure 20 depicts the example of a linear passive bus.



Key

ECU Electronic control unit / FlexRay node

Figure 20 — Example of a linear passive bus

Table 13 defines the parameters of a linear passive bus structure.

Table 13 — Parameters of a linear passive bus structure

Name	Description	Min	Max	Unit
nSplice	Number of splices [a]	2	—	—
[a] If *nSplice* is 0, then refer to 9.2, if *nSplice* is 1, then refer to 9.3.				

The parameters $lStub_i$, with i = 1 … *nStub*, are limited implicitly by the requirements of signal integrity.

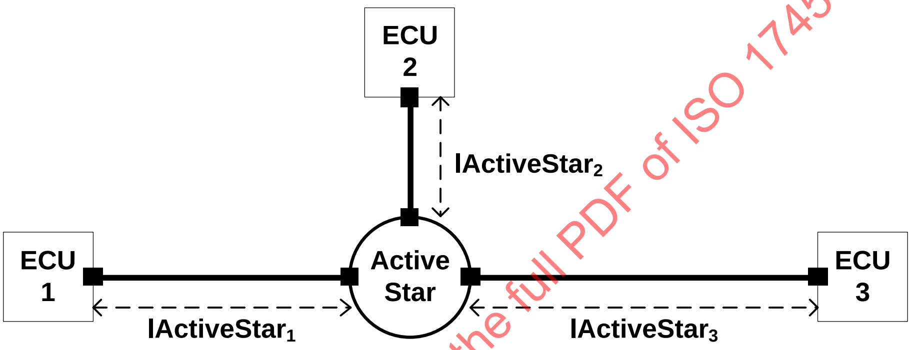
Limitations for *nStub*, *nSplice*, $lSpliceDistance_{M,N}$ and $lStub_i$ depend on each other and further factors, like the chosen termination concept and cable type.

Examples of practical values are given in Annex A, where also consideration about EMC robustness can be found in a separate subclause.

9.5 Active star network

The active star network uses point-to-point connections between active stars and ECUs. The number of branches at an active star is *nActiveBranches*. The length of a branch is $lActiveStar_n$. The active star to which the ECUs are connected has the function to transfer data streams on one branch to all other branches. Since the active star device has a transmitter and receiver circuit for each branch, the branches are actually electrically decoupled from each other. The active star is specified in detail in Clause 13.

Figure 21 depicts the example of an active star network.



Key

ECU Electronic control unit / FlexRay node

Figure 21 — Example of an active star network

Table 14 defines the limitations of active star networks.

Table 14 — Limitations of active star networks

Name	Description	Min	Max	Unit
nActiveBranches	Number of branches at an active star	2	—	—

An active star with only two branches may be considered as a degenerated star, a relay or hub for increasing overall bus length. Another reason for applying such active stars might be to take advantage of the fault containment behaviour of the active star between two linear passive busses. See Clause 13 for detailed information about the active star.

A branch of an active star may also be connected to a linear passive bus or a passive star. For these kinds of bus structures and their restrictions see 9.3. and 9.4.

A branch of an active star may also be connected to a second active star. For these kinds of bus structures and their restrictions see 9.6.

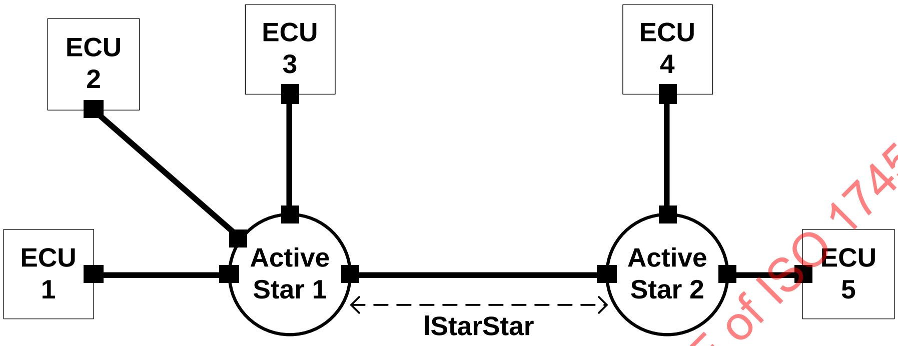
Examples of practical values are given in Annex A, where also consideration about EMC robustness can be found in a separate subclause.

9.6 Cascaded active stars

Active stars can be cascaded in systems that operate with 2,5 Mbit/s and 5 Mbit/s. This means two active stars are connected to each other with a point-to-point connection. A data stream that is sent from an ECU M to an ECU N passes $nStarPath_{M,N}$ active stars while being conveyed on the bus.

Chosen topologies shall remain in the asymmetric delay acceptance range of the decoder (see Annex A and configuration constrains in ISO 17458-2).

Figure 22 depicts the example of a bus with cascaded active stars.



Key

ECU Electronic control unit / FlexRay node

Figure 22 — Example of a bus with cascaded active stars

Table 15 defines the limitations of topologies with active stars.

Table 15 — Limitations of topologies with active stars

Name	Description	Min	Max	Unit
$nStarPath_{M,N}$	Number of active stars on the signal path from an ECU M to an ECU N 2,5 Mbit/s and 5 Mbit/s	0	2	—
	Number of active stars on the signal path from an ECU M to an ECU N 10 Mbit/s	0	1 [a]	—
a Active stars are not possible since the asymmetric delay is too high. See Annex A.				

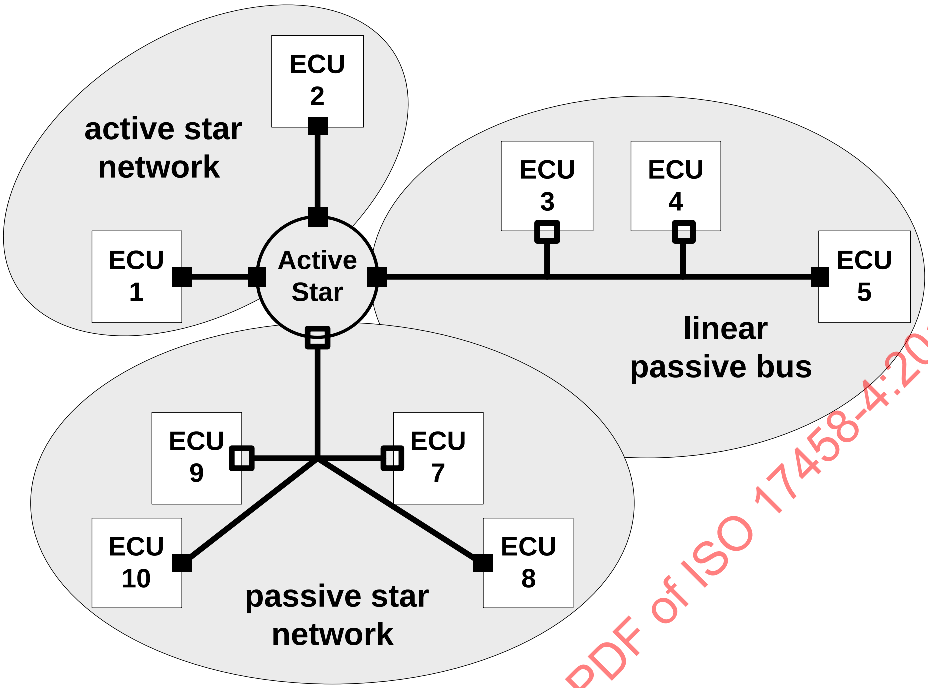
Practical limitations for *lStarStar* depend on factors like cable type and EMC disturbances.

Examples of practical values are given in Annex A, where also consideration about EMC robustness can be found in a separate subclause.

9.7 Hybrid topologies

In active star networks, one or more branches of the active star may be built as a linear passive bus or as a passive star. Considerations about signal asymmetries and about EMC robustness can be found in Annex A.

Figure 23 depicts the example of a hybrid bus structure.



Key

ECU Electronic control unit / FlexRay node

Figure 23 — Example of a hybrid bus structure

9.8 Dual channel topologies

FlexRay communication modules offer the possibility to serve up to two channels. This may be used to increase bandwidth and/or introduce a redundant channel in order to increase the level of fault tolerance. For further details see ISO 17458-2.

It is advisable to investigate and minimize the differences in the maximum propagation delays that occur on the two channels. See application hint about propagation delay in Annex A.

Furthermore the dual channel approach does not influence the BD definition.

10 Asymmetric delay budget

10.1 Objective

This Clause describes the specified [1] behaviour of the asymmetric delay on the way from a transmitting node to a receiving node via a dedicated FlexRay topology. The decoding procedure in the communication controller requires limiting the asymmetric delay (shifting of consecutive edges in the time domain) in a system.

1) The specification of the resulting requirements to the BD and CC is concretized in the corresponding chapters.

10.2 Basic topology for asymmetric delay budget

As basis for the definition of the asymmetric delay budget an active star network is used.

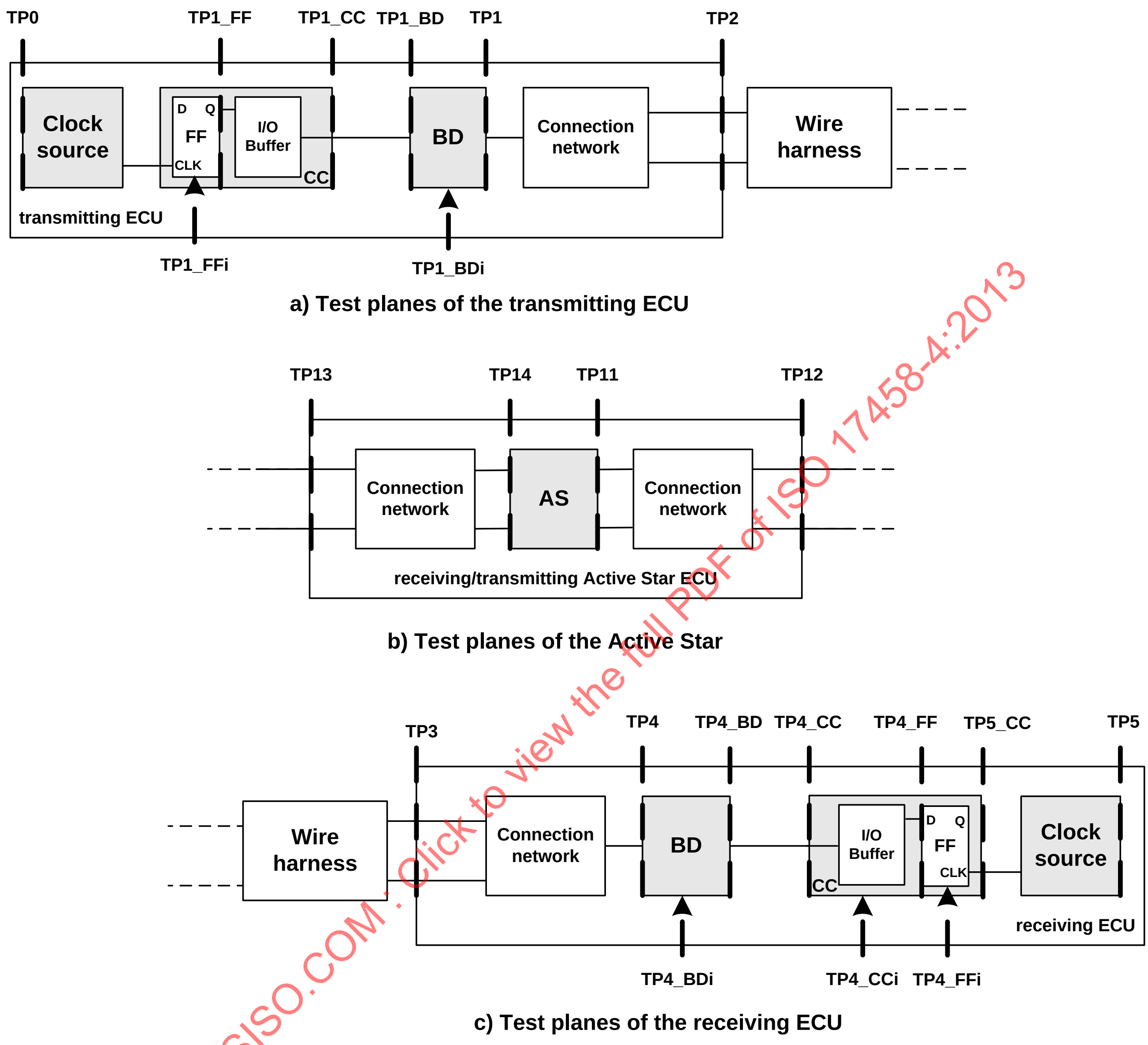
From the data communication point of view an active star network consists of several components in a row:

- A transmitting ECU consisting of:
  a clock source, a CC, a BD and a connection hardware (e.g. CMC, connector, etc) to a first point-to-point network
- A first point-to-point network
- A retransmitting active star ECU consisting of:
  a connection hardware to a first point-to-point network, the active star device and a connection hardware to a second point-to-point network
- A second point-to-point network
- A receiving ECU consisting of:
  a connection hardware to a second point-to-point network, a BD, a CC and a clock source.

10.3 Definition of Test Planes

Various test planes are defined to derive test and measurement sceneries easily. The defined test planes are valid in any topology.

Figure 24 depicts the test planes in an active star network.



Key

AS Active Star

BD Bus driver

ECU Electronic control unit / FlexRay node

FF Flip flop

TP Test plane

Figure 24 — Test planes in an active star network

Table 16 defines the test planes.

Table 16 — Test planes

Test plane	Description
TP0	Virtual time reference point.
TP1_FFi	Transmitting CC's virtual test plane to visualize PLL jitter, clock skew and propagation delay of the FlipFlop.
TP1_FF	Transmitting CC's internal test plane at 'Q' pin of last FlipFlop before output buffer
TP1_CC	Transmitting CC's output pin (TxD)
TP1_BD	Transmitting BD's input pin (TxD).
TP1_BDi	Transmitting BD's internal virtual test plane after detecting the logical state of the input signal.
TP1	Transmitting BD's output pins.
TP2	Transmitting ECU connector's terminals to the wiring harness.
TP13	Receiving AS ECU connector's terminals from the wiring harness.
TP14	Receiving AS devices input pins.
TP11	Transmitting AS device's output pins.
TP12	Transmitting AS ECU connector's terminals to the wiring harness.
TP3	Receiving ECU connector's terminals from the wiring harness.
TP4	Receiving BD's input pins.
TP4_BDi	Receiving BD's internal virtual test plane after detecting the logical state of the input signal.
TP4_BD	Receiving BD's output pin (RxD).
TP4_CC	Receiving CC's input pin (RxD).
TP4_CCi	Receiving CC's internal virtual test plane after detecting the logical state of the input signal.
TP4_FF	Receiving CC's internal test plane at 'D' pin of first FlipFlop after input buffer
TP4_FFi	Receiving CC's virtual test plane to visualize PLL jitter, clock skew and propagation delay of the FlipFlop.
TP5_CC	Clock input to CC
TP5	Virtual test plane at the input of the decoding algorithm.

10.4 Requirements to the asymmetric delay budget

The asymmetric delay shifts two consecutive edges against or away from each other. Each component (e.g. the transmitting BD) requires its portion (manufacturing tolerances, junction temperature, ageing etc.). Adding up all of these portions and subtracting the result from the decoder's asymmetric delay robustness gives a margin. This resulting margin can be used e.g. to ensure robustness against RF influences.

The decoder's asymmetric delay robustness shall be greater than the sum of all asymmetric delays of the entire network (see also Table 21).

10.5 Definition of maximum asymmetric delay portions

Three different types of values are considered in the following calculation:

Table 17 defines the types of values used in the following calculations.

Table 17 — Types of values used in the following calculations

Type	Description
Specified values	Values are required by this specification.
Educated guess	Values are estimated based on best engineers practice.
Derived values	Values are based on calculations by using specified boundary conditions.

To keep the description simple the portions of the asymmetric delay budget are noted by values only. Parameters with names and test conditions are introduced inside the corresponding subclauses.

FlexRay offers several possibilities for building robust networks. Also the active star network example in this subclause offers some alternative approaches.

An active star can be built in two ways:

a) The active star is a monolithic device.

b) The active star is non-monolithic and consists of more than one device.

Finally the asymmetric delay is considered on the following pages from two different point of views:

a) influence to the shortening of a single bit

b) influence to the sampling and synchronization of the decoder

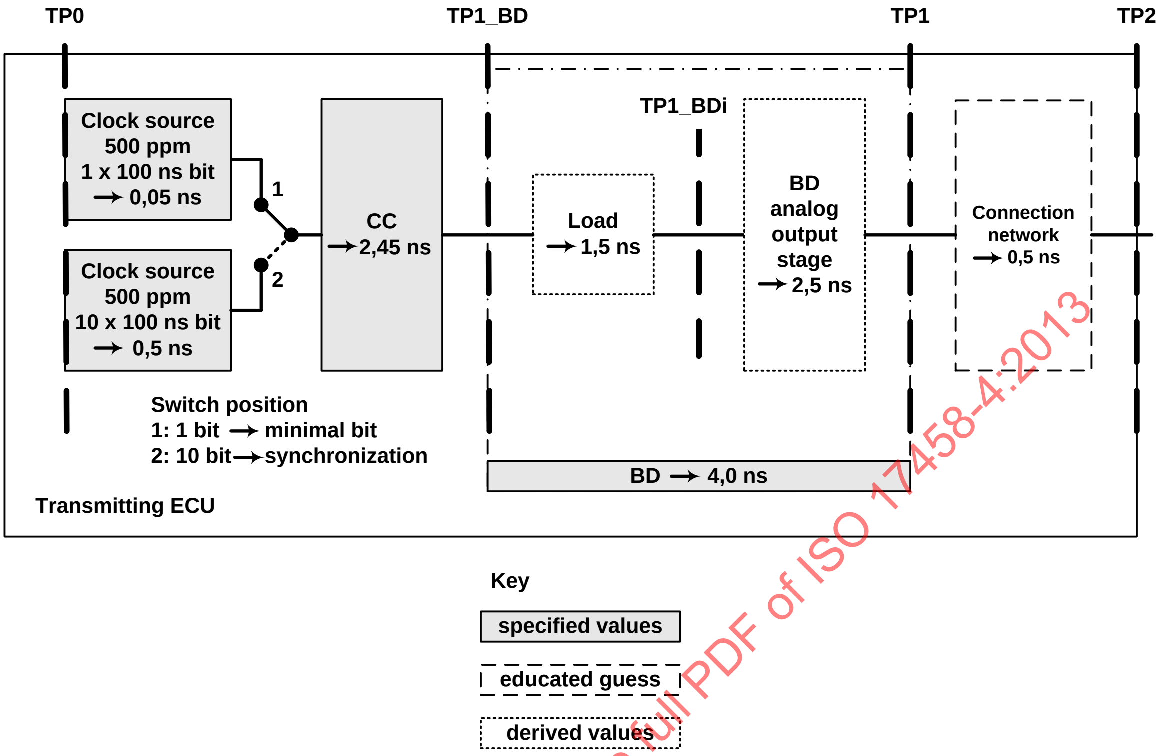
The asymmetric delay in the active star network consists of several portions:

Table 18 defines the asymmetric delay budget TP0 to TP2.

Table 18 — Asymmetric delay budget TP0 to TP2

Amount ns	Portion	Description
N × 0,05	Clock source	The specified tolerance of 500 ppm generates this portion regarding the duration of N bits at 10 Mbit/s. Lower datarates lead to bigger portions.
2,45	CC	The transmitting CC is allowed to vary the duration of a single nominal 100 ns bit by ±2,45 ns as specified in 14.2.3.
4,0	BD	The transmitting BD is allowed to vary the duration between two consecutive edges up to ±4,0 ns (TP1_BD → TP1) when the CC drives 25 pF load on its TxD pin as specified in 12.9.2. The 4 ns portion may be separated for further theoretical considerations into two portions: a) 1,5 ns represents the BD's digital detection of the CC's output signal caused by edge to pass the specified logical level thresholds. b) 2,5 ns represents the BD's analog output stage asymmetry.
0,5	Connection network	The connection network is estimated to change the duration between two consecutive edges by at most ±0,5 ns. A test set-up to measure this portion is not specified.
NOTE The worst case asymmetry from TP0 to TP2 sums up to 7,0 ns for one bit and to 7,45 ns for a period of ten bits at 10 Mbit/s at a load of 25 pF on TxD.		

Figure 25 depicts the asymmetric delay budget (TP0 to TP2).



BD Bus driver

CC Communication controller

TP Test plane

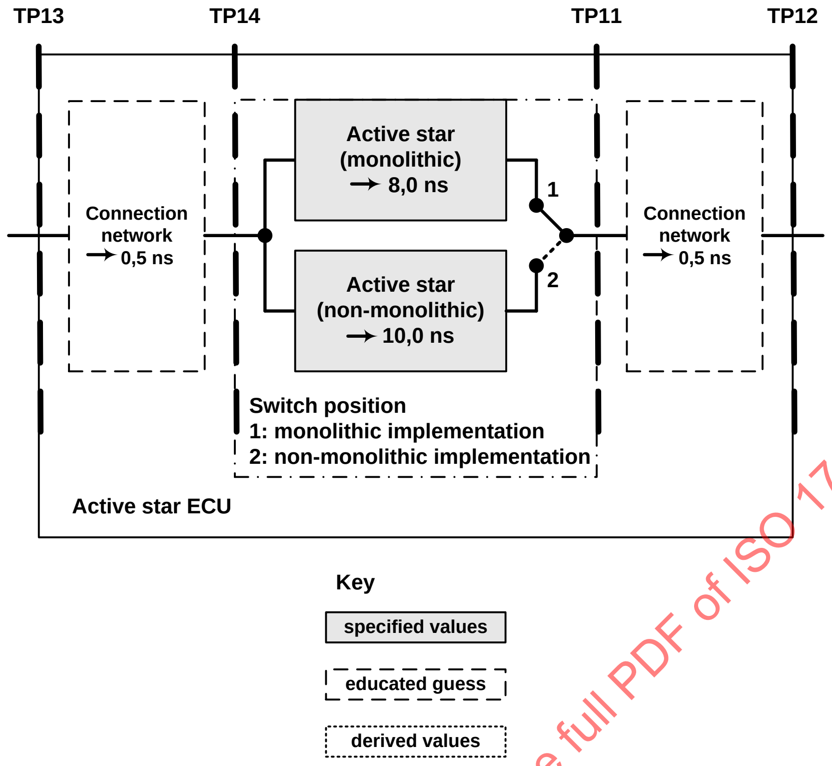
Figure 25 — Asymmetric delay budget (TP0 to TP2)

Table 19 defines the asymmetric delay budget (TP13 to TP12).

Table 19 — Asymmetric delay budget (TP13 to TP12)

Amount	Portion	Description
0,5 ns	Connection network	The connection network is estimated to change the duration between two consecutive edges by at most ±0,5 ns. A test set-up to measure this portion is not specified.
8,0 ns (10,0 ns)	AS device	The AS is allowed to vary the duration between two consecutive edges up to ±8,0 ns (monolithic implementation) or ±10,0 ns (non-monolithic implementation) (TP14 → TP11): as specified in 13.3.2.
0,5 ns	Connection network	The connection network is estimated to change the duration between two consecutive edges by at most ±0,5 ns. A test set-up to measure this portion is not specified.
NOTE The worst case asymmetry from TP13 to TP12 sums up to 9,0 ns (11,0 ns).		

Figure 26 depicts the asymmetric delay budget (TP13 to TP12).



Key

TP Test plane

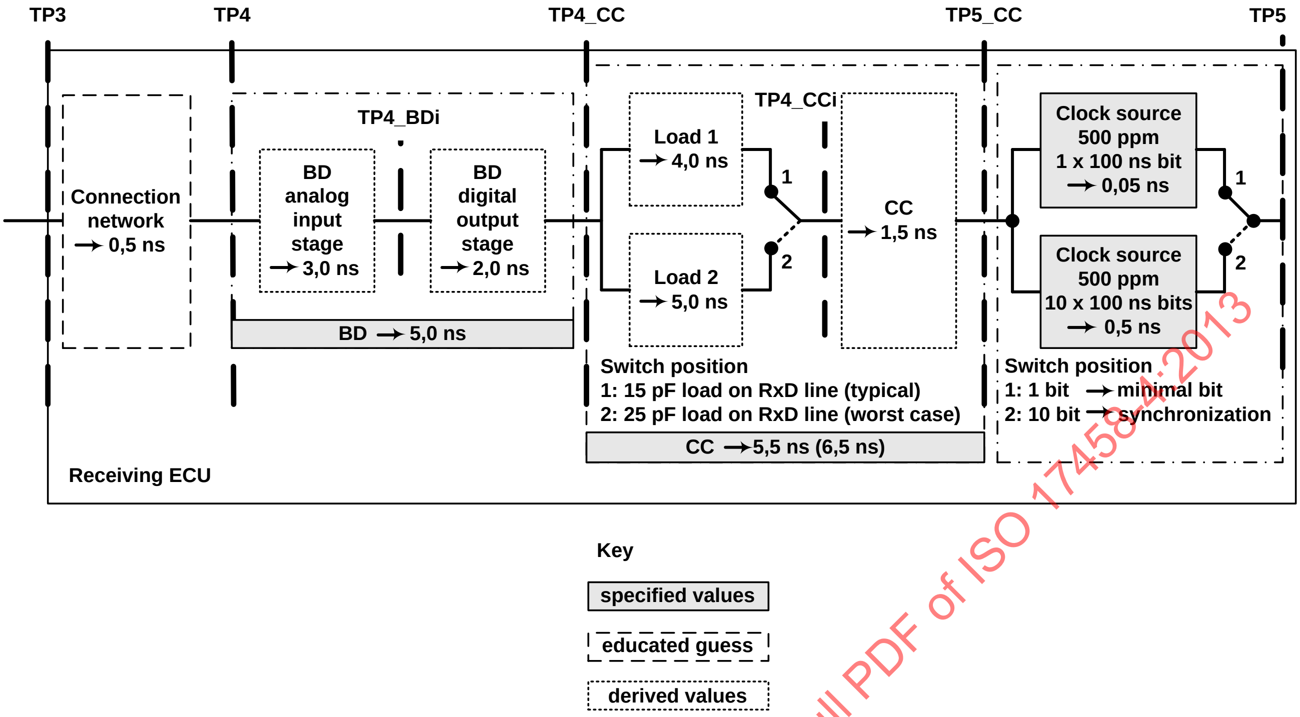
Figure 26 — Asymmetric delay budget (TP13 to TP12)

Table 20 defines the asymmetric delay budget (TP3 to TP5).

Table 20 — Asymmetric delay budget (TP3 to TP5)

Amount	Portion	Description
0,5 ns	Connection network	The connection network is estimated to change the duration between two consecutive edges by at most ±0,5 ns. A test set-up to measure this portion is not specified.
5,0 ns	BD	The receiving BD is allowed to vary the duration between two consecutive edges up to ±5,0 ns (TP4 → TP4_CC) as specified in 12.9.6. The 5 ns portion may be separated for further theoretical considerations into two portions: a) 3,0 ns represents the BD's analog input stage asymmetry. b) 2,0 ns represents the BD's digital output stage asymmetry.
5,5 ns (6,5 ns)	CC	The receiving CC is allowed to detect the duration between two consecutive edges with a deviation up to ± 5,5 ns (± 6,5 ns) (TP4_CC → TP5_CC) when the BD drives 15 pF (25 pF) load on its RxD pin as specified in 14.2.5. The 5,5 ns portion may be separated for further theoretical considerations into two portions: a) 4,0 ns (5,0 ns) represents the CC's digital detection of the BD's output signal caused by edge to pass the specified logical level thresholds. b) 1,5 ns This portion represents the CC's remaining asymmetry.
N × 0,05 ns	Clock source	The specified tolerance of 500 ppm generates this portion regarding the duration of N bit at 10 Mbit/s. Lower data rates lead to bigger portions.
NOTE The worst case asymmetry from TP3 to TP5 sums up to 11,05 ns for one bit and to 11,5 ns for a period of ten bits at 10 Mbit/s at a load of 15 pF on RxD.		

Figure 27 depicts the asymmetric delay budget (TP3 to TP5).



BD Bus driver

CC Communication controller

TP Test plane

Decoder's asymmetric delay robustness:

10 bit = 37,5 ns (independent of crystal)
1 bit = 36,5 ns (500 ppm crystal at 10 Mbit/s)

Figure 27 — Asymmetric delay budget (TP3 to TP5)

Table 21 defines the decoder's asymmetric delay robustness.

Table 21 — Decoder's asymmetric delay robustness

Amount	Portion	Description
37,5 ns	CC	The decoding procedure (fifth of eight samples per bit) allows a variation of ±3 sample periods or ±37,5 ns in a 10 Mbit/s system at TP5 in general. This variation has to be guaranteed at two consecutive edges bordering a period of ten bits.
36,5 ns	CC	Based on the 37,5 ns requirement above for a period of ten bits the duration of a single nominal 100 ns bit may vary up to ±36,6 ns at TP5. For details see Annex A.

Adding up all worst case portions (from TP0 to TP5, including one monolithic active star) ends in a maximal asymmetric delay (regarding 10 bits at 10 Mbit/s), which is less than the decoder's tolerance. A margin of 9,55 ns is available.

EXAMPLE

Decoder's asymmetric delay robustness:	37,50 ns
Sum of asymmetric delays of the entire network:	-27,95 ns
Available margin:	9,55 ns

Further exemplary calculations for other topologies are given in Annex A.

10.6 Other networks

All the other networks such as:

— passive star

— linear passive bus

— cascaded active stars

— hybrid topologies

can be designed by combining the following exemplary variations:

— Adapting the communication speed.

— Damping EMC influences.

— Limiting the cable length and/or the cable damping.

— Using components which have a better performance than the above specified values.

— Using implementations which support optimized "educated guess figures".

For further information see Annex A.

11 Signal integrity

11.1 Objective

There are two possibilities to assess the differential voltage on the wiring harness (*uBus*) and its alternation on its way from the transmitter to the receiver. One possibility is based on the timings of the bus driver or active star, which are specified in detail in Clause 12 and Clause 13, and is called 'masks test'. The other possibility is based on the timing requirements of the decoder in the receiving communication controller and makes use of 'eye-diagrams'. The latter ones are described in Annex A, while the 'masks' for the tests are described in this Clause.

Figure 28 gives an overview of the relationship of eyes and masks.

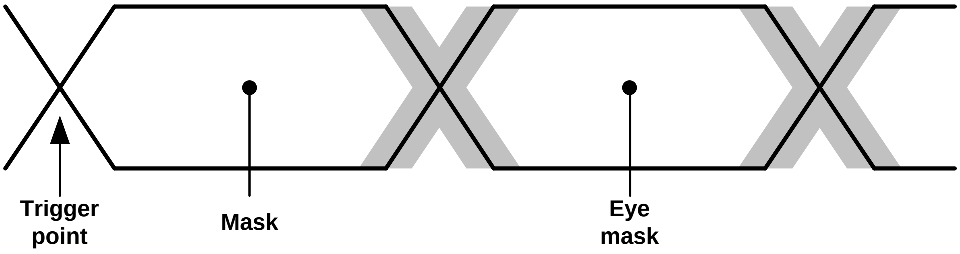


Figure 28 — Relation from eye to mask

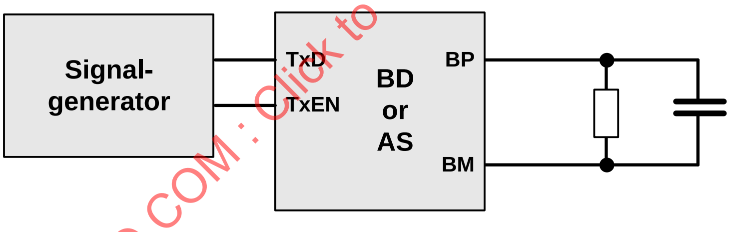
Eyes result from an offline overlay of traces of *uBus* that are synchronized at the zero volts crossing during the falling edge in each BSS, while during a mask test the traces of *uBus* are overlaid and synchronized with every zero volts crossing.

11.2 Mask test at TP1 / TP11

11.2.1 Overview

For FlexRay conform transmission a bus driver or active star shall send a differential voltage signal that meets the requirements given in 12.9. This behaviour is verified with a measurement on TP1 that is done with a 'load dummy' that consists of a resistor $R_{LoadDummy}$ equal to 40 Ω and a $C_{LoadDummy}$ equal to 100 pF in parallel.

Figure 29 depicts the test setup for measurements at TP1 / TP11.



Key

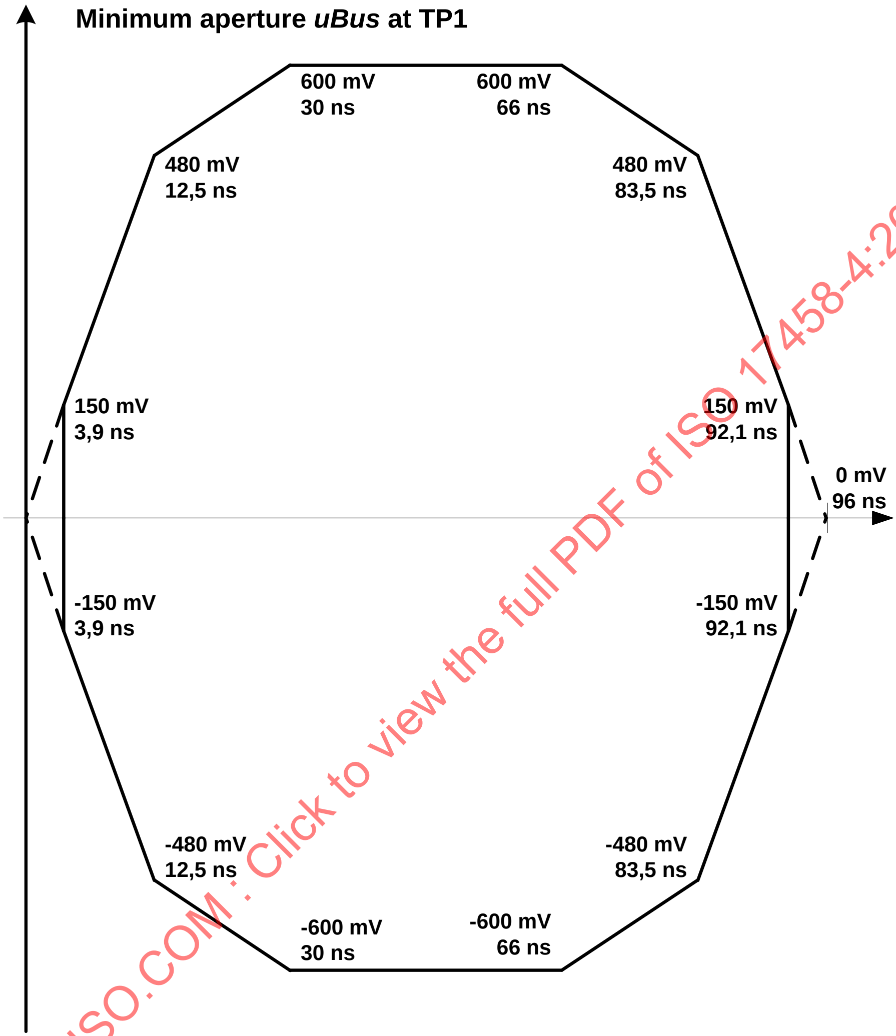
AS	Active star
BD	Bus driver
BM	Bus plus
BP	Bus minus
TxD	Transmit Data
TxEN	Transmit Enable

Figure 29 — Test setup for measurements at TP1 / TP11

The bus driver or active star under test shall be controlled by a signal generator on TxEN and TxD, where the signal on TxD signal has a sum of rise and fall times up to 9 ns (20 % to 80 % of uV_{DIG}) and a perfect bit duration of 100,0 ns.

11.2.2 Standard TP1 Mask

A FlexRay bus driver shall meet the mask as given in Figure 30 with the test load as defined in 11.2.1. The signal trace of *uBus* shall be captured by triggering on every zero volts crossing (rising and falling) of *uBus*, while TxEN is on logical low.



NOTE The dotted lines are only auxiliary lines to show where the slopes would cross the zero line.

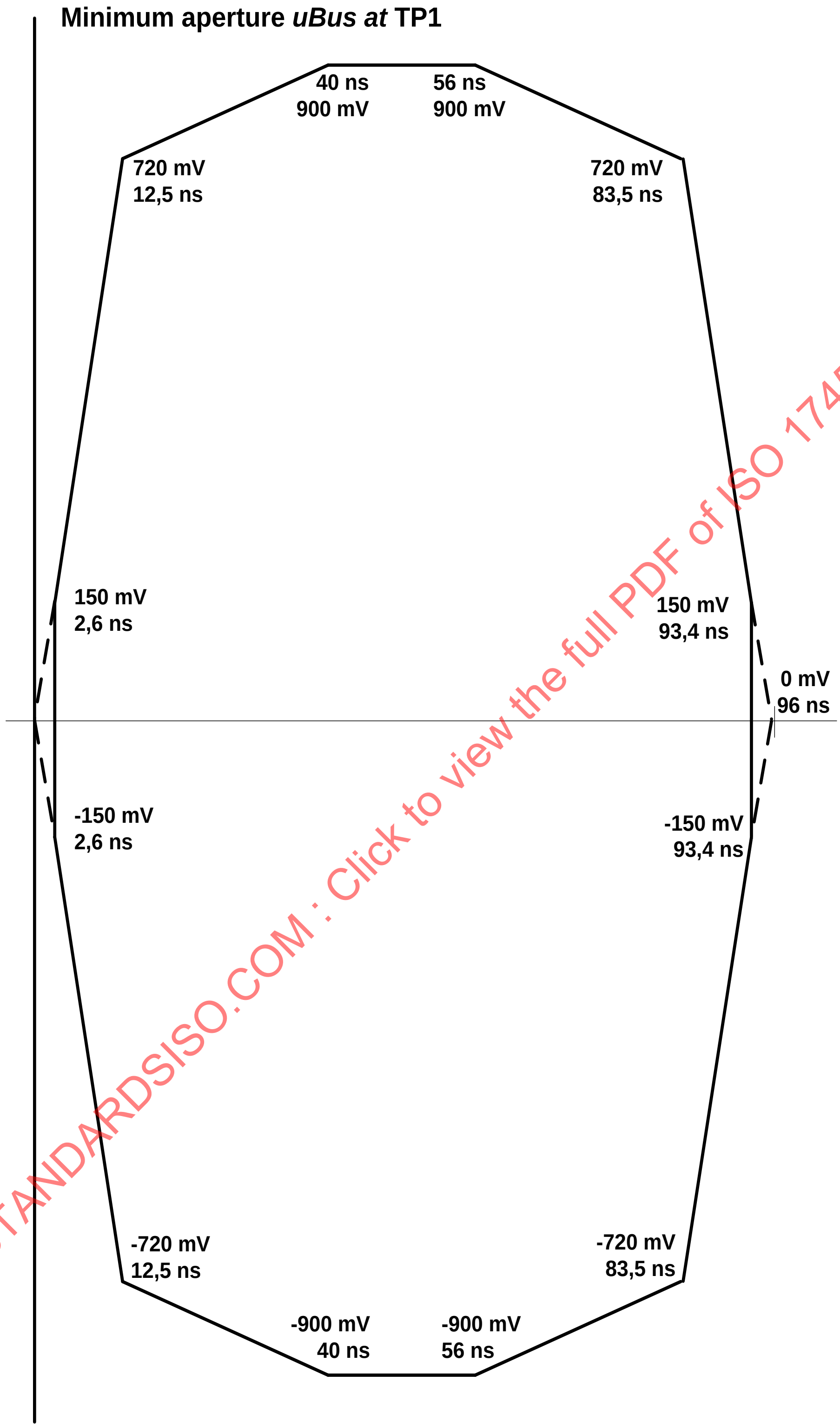
Figure 30 — Required waveform at TP1

11.2.3 TP1 mask for functional class "Bus driver increased voltage amplitude transmitter"

A FlexRay bus driver that implements the functional class "Bus driver increased voltage amplitude transmitter" shall meet the mask as given in Figure 31 under the test conditions as defined in 11.2.1.

The signal trace of *uBus* shall be captured by triggering on every zero volts crossing (rising and falling) of *uBus*, while TxEN is on logical low.

Figure 31 depicts the required waveform at TP1 for functional class "Bus driver increased voltage amplitude transmitter".



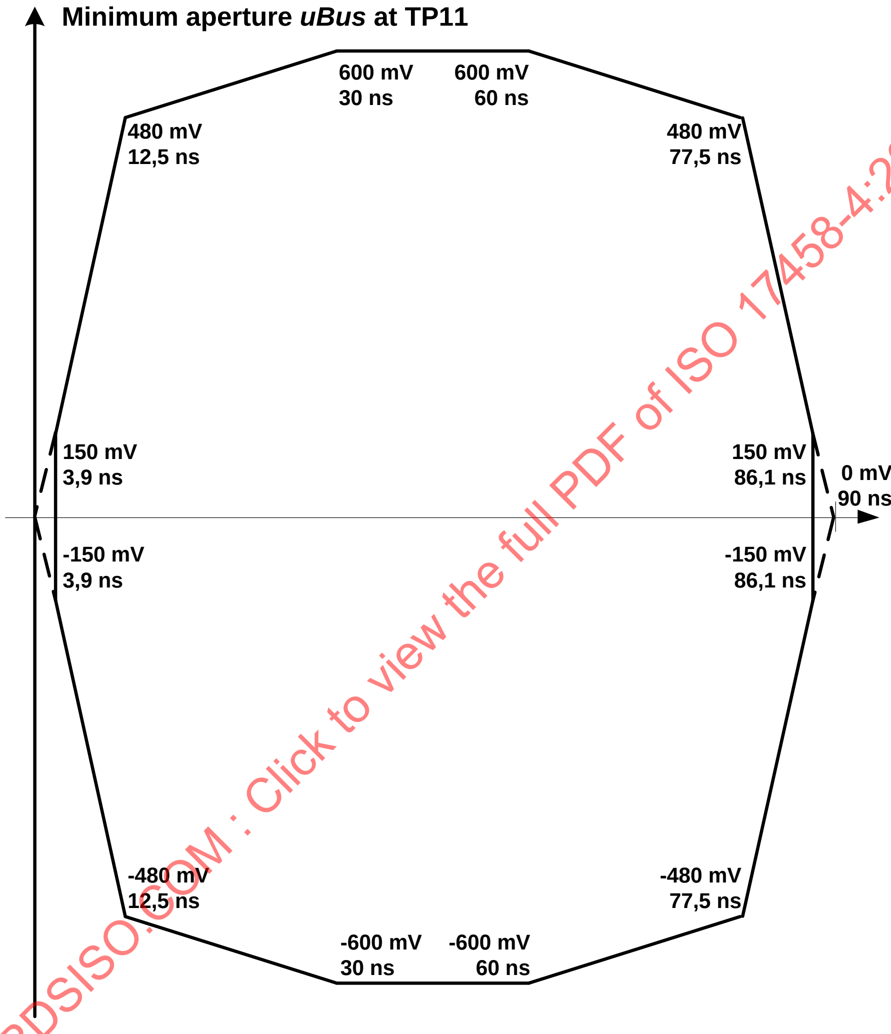
NOTE The dotted lines are only auxiliary lines to show where the slopes would cross the zero line.

Figure 31 — Required waveform at TP1 for functional class "Bus driver increased voltage amplitude transmitter"

11.2.4 Standard TP11 Mask

A FlexRay active star shall meet the mask as given in Figure 32 with the test load as defined in 11.2.1. The signal trace of *uBus* shall be captured by triggering on every zero volts crossing (rising and falling) of *uBus*, while TxEN is on logical low.

Figure 32 depicts the required waveform at TP11.



NOTE The dotted lines are only auxiliary lines to show where the slopes would cross the zero line

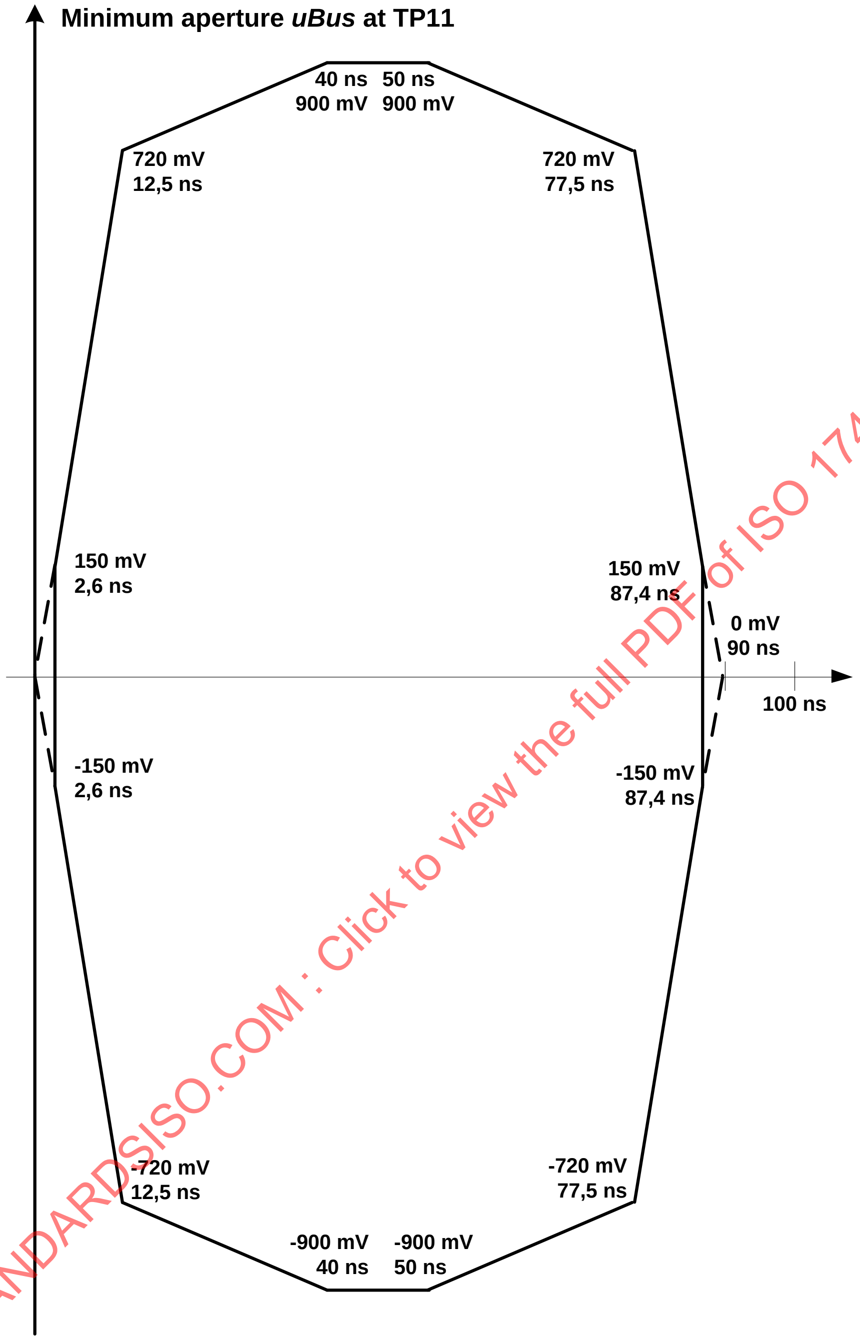
Figure 32 — Required waveform at TP11

11.2.5 TP11 mask for functional class "Active star increased voltage amplitude transmitter"

A FlexRay active star that implements the functional class "Active star increased voltage amplitude transmitter" shall meet the mask as given in Figure 33 under the test conditions as defined in 11.2.1.

The signal trace of *uBus* shall be captured by triggering on every zero volts crossing (rising and falling) of *uBus*, while TxEN is on logical low.

Figure 33 depicts the required waveform at TP11 for functional class "Active star increased voltage amplitude transmitter".



NOTE The dotted lines are only auxiliary lines to show where the slopes would cross the zero line.

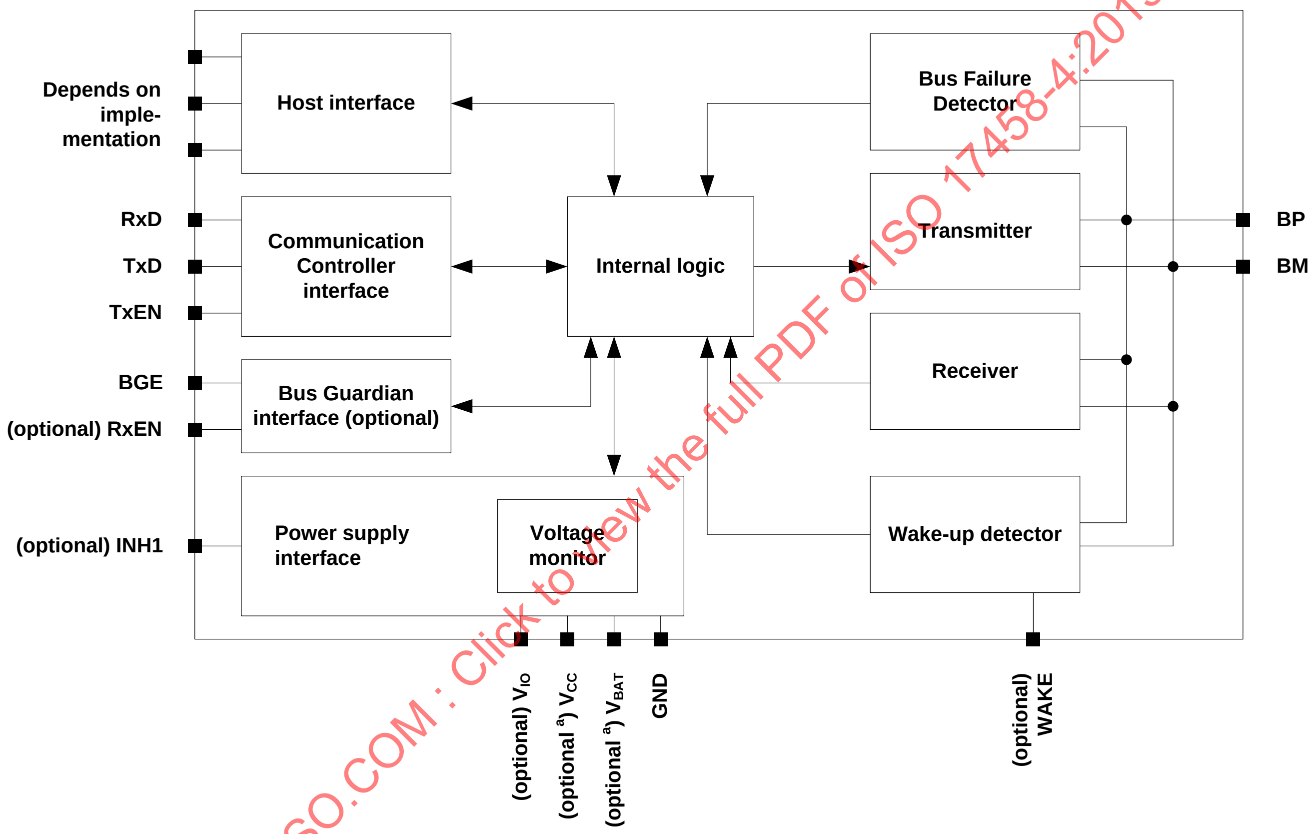
Figure 33 — Required waveform at TP11 for functional class "Active star increased voltage amplitude transmitter"

12 Electrical bus driver

12.1 Overview

The electrical bus driver (BD) realizes the physical interface between FlexRay node module and the channel. The BD provides a differential transmit and receive capability to the bus, allowing the node module bidirectional time multiplexed binary data stream transfer. Apart from the transmit and receive function, the BD provides means for low power management, supply voltage monitoring (under-voltage-detection) as well as bus failure detection and represents a ESD-protection barrier between the bus and the ECU.

Figure 34 depicts the exemplary bus driver block diagram.



Key

BGE	Bus guardian enable	TxEN	Transmit enable not
BM	Bus minus	V_{BAT}	Battery voltage [a]
BP	Bus plus	V_{CC}	Supply voltage [a]
GND	Connection to system ground	V_{IO}	Digital I/O voltage
RxD	Receive data	INH1	Bus Driver Inhibit 1 output
TxD	Transmit data	WAKE	Wakeup input

[a] At least one of the pins V_{CC} and V_{BAT} have to be implemented.

Figure 34 — Exemplary bus driver block diagram

12.2 Operation modes

12.2.1 General

The electrical BD supports a set of operation modes, which are described in this Clause. The operation modes *BD_Normal* and *BD_Standby* are mandatory to implement. Two optional modes, which are *BD_Sleep* and *BD_ReceiveOnly*, are described and further product specific modes may be supported.

12.2.2 BD_Normal mode

The BD is able to send and receive data streams on the bus.

Not_Sleep is signalled on INH1 in case this interface is present, see 12.7.3.

The bus pins are biased, see 12.9.5.

12.2.3 BD_Standby mode

The *BD_Standby* mode is a low power mode.

The BD is not able to send or receive data streams to/from the bus.

The BD could be able to detect wakeup events (optional, see 12.10 and 12.11).

The power consumption is reduced compared to *BD_Normal*.

Not_Sleep is signalled on INH1 in case this interface is present, see 12.7.3.

The bus pins are terminated to GND via receiver common mode input resistance.

12.2.4 BD_Sleep mode (optional)

This option belongs to the functional classes "Bus driver voltage regulator control" and "Bus driver internal voltage regulator".

The *BD_Sleep* mode is a low power mode.

The BD is not able to send or receive data streams to/from the bus.

The BD's wakeup monitoring functions are operational.

The power consumption is reduced compared to *BD_Normal*.

Sleep is signalled on INH1.

The bus pins are terminated to GND via receiver common mode input resistance.

12.2.5 BD_ReceiveOnly mode (optional)

The BD is able to receive data streams on the bus, but not able to transmit.

Not_Sleep is signalled on INH1 in case this interface is present.

The bus pins are biased, see 12.9.5.

12.2.6 BD_Off

The BD is unsupplied.

The BD is not able to send or receive data streams to/from the bus.

The BD's wakeup monitoring functions (if implemented) are not operational.

The digital outputs behave according to 15.2.

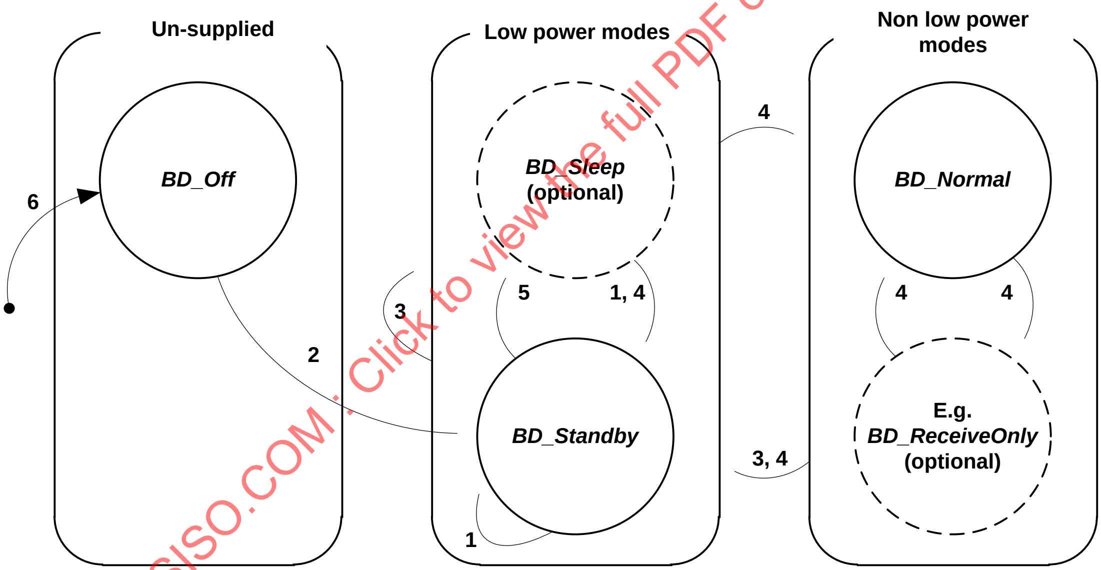
Bus pins are in high-resistance state, see Table 50.

12.3 Operation mode transitions

12.3.1 Overview

Mode transitions happen upon commands from the host via the bus driver - host interface, detection of wakeup events or due to undervoltage conditions.

Figure 35 depicts the exemplary state diagram.



NOTE   See Table 22 for operation mode transition definitions

Figure 35 — Exemplary state diagram

Table 22 defines the operation mode transition table.

Table 22 — Operation mode transition table

Transition	Reason for transition	further BD behaviour after transition
1	Detection of a wakeup event [a]	Undervoltage detection timers are restarted, if undervoltage conditions remain present.
2	Power on - Supply voltage(s) rise above power on threshold [a]	—
3	Detection of undervoltage condition (transition according to 12.3.2)	See 12.3.3.
4	Host command [b]	—
5	Detection of V_{BAT} or V_{DIG} undervoltage condition or host command (if *BD_Sleep* is implemented)	Ignore EN input, while in *BD_Sleep*
6	Power off - Supply voltage(s) fall below power on threshold [a] – transition can start from any other mode.	—

[a] A bus driver shall react on a power-on/off and wakeup events latest within 100 µs.

[b] In case the host commands a non-low power mode while only V_{CC} is in undervoltage the BD shall enter *BD_Standby*. In case V_{BAT} or V_{DIG} is in undervoltage *BD_Sleep* cannot be left via host command.

Table 23 defines the summary of supply voltage conditions.

Table 23 — Summary of supply voltage conditions

uV_{BAT} [a]	uV_{CC}	BD can enter …	Wakeup detection is …
≥ 5,5 V	Not implemented	All operation modes	Mandatory
Not implemented	Normal operating range	All operation modes	Mandatory (if wakeup detector is implemented)
≥ 7 V	Undervoltage or unsupplied	Low power modes	Mandatory [b]
≥ 7 V	Normal operating range	All operation modes	Mandatory
< 7 V, but not in undervoltage	Normal operating range	All operation modes	Not mandatory
Undervoltage or unsupplied	Normal operating range	Low power modes	Not mandatory
Undervoltage or unsupplied or not implemented	Undervoltage	Low power modes	Not mandatory
Undervoltage	Undervoltage or unsupplied or not implemented	Low power modes	Not mandatory
Unsupplied or not implemented	Unsupplied or not implemented	*BD_Off*	Not possible

[a] Mind that uV_{BAT} is the voltage on the BD's pin and uV_{ECU} the voltage applied from the vehicle battery to the ECU connector.

[b] Detection of remote wakeup (see 12.11) and via WAKE pin (see 12.10) required even with V_{CC} and V_{DIG} concurrently in undervoltage conditions.

12.3.2 Mode transitions due to detection of undervoltage conditions

Expiration of an undervoltage timer forces the BD to a low power mode:

- In case the V_{BAT} and/or V_{DIG} undervoltage detection timer expires *BD_Sleep* shall be entered, if implemented, otherwise *BD_Standby*.
- In case the V_{CC} undervoltage detection timer expires, while the BD is not in *BD_Sleep*, *BD_Standby* shall be entered.
- No mode change is initiated, when an undervoltage detection timer expires, while the BD is in *BD_Sleep*.

12.3.3 Mode transitions in case of undervoltage recovery

The behaviour in case of recovery from undervoltage(s) shall be implemented as follows:

- In case the BD has a BD – host interface according to option A (hard wired) the BD shall change to the mode, as requested by the host interface, when possible according to 12.6.2.
- In case the BD has a BD – host interface according to option B (SPI) the BD shall not change the mode with recovery from undervoltage.

12.3.4 Mode transitions due to detected wakeup events

BD_Standby shall be entered.

Undervoltage detection timers are reset and restarted, if undervoltage conditions remain present.

12.3.5 Power on event

The BD shall recognize the event of becoming sufficiently supplied via V_{BAT} (if implemented) or via V_{CC} (if implemented) after being not powered and enter *BD_Standby*.

12.3.6 Power off event

In case the supply voltage(s) fall below the product specific power–on threshold the BD shall enter *BD_Off* mode.

12.4 Bus driver – communication controller interface

12.4.1 General

The interface between the BD and CC comprises three digital electrical signals. There are two inputs to the BD from the CC (TxD and TxEN), and one output from the BD to the CC (RxD).

The CC uses the TxD (Transmit Data) signal to transfer a binary data stream to the BD for transmission onto the channel. The TxEN (Transmit Data Enable Not) signal is used by the CC to signal whether the data on TxD is valid or not. A timeout *dBDTxActiveMax* needs to be implemented to ensure that the transmitter cannot be enabled permanently. Furthermore a BD shall never start a transmission with a *Data_1*, therefore activation of the transmitter via the TxEN signal shall not be possible as long as TxD is still on logical high.

Appropriate timing of TxD and TxEN at the end of transmission is ensured by ISO 17458-2.

Table 24 defines the maximum length of transmitter activation.

Table 24 — Maximum length of transmitter activation

Name	Description	Min	Max	Unit
dBDTxActiveMax	Maximum length of transmitter activation	650	2 600	µs

The maximum length of a communication element that can be sent is limited to the minimum value of *dBDTxActiveMax*. For calculation of length of an encoded frame see ISO 17458-2.

12.4.2 RxD - behaviour

The BD uses the RxD during *BD_Normal* mode to transfer a received binary data stream to the CC. When in a low power mode the RxD signals the recognition of a wakeup event.

Table 25 defines the resulting RxD signal from BD to CC.

Table 25 — Resulting RxD signal from BD to CC

BD operation mode	Signal on bus wires	WU [a]	RxD [b]
BD_Normal & BD_ReceiveOnly	*Idle*	X [c]	high
	Data_0	X	low
	Data_1	X	high
BD_Standby & BD_Sleep	X	detected	low
	X	not detected	high
= All other =	X	X	Product specific

[a] WU = wakeup event; see 12.10 and 12.11.

[b] The output voltages for logical high and low states are defined in Clause 15.

[c] X = don't care

12.4.3 TxD/TxEN behaviour in case a bus driver - bus guardian interface is implemented

Table 26 defines the signalling on bus wires in dependency of BD input states.

Table 26 — Signalling on bus wires in dependency of BD input states

BD operation mode	TxEN	BGE [a]	TxD	Resulting signaling on the bus
BD_Normal	high	X [b]	X	*Idle*
	X	low	X	*Idle*
	low	high	low	*Data_0*
	low	high	high	*Data_1*
Low power modes	X	X	X	*Idle*

[a] The BGE signal belongs to the bus driver - bus guardian interface.

[b] X = don't care

12.4.4 TxD/TxEN - behaviour in case a bus driver - bus guardian interface is not implemented

Table 26 defines the signalling on bus wires in dependency of BD input states.

Table 27 — Signalling on bus wires in dependency of BD input states

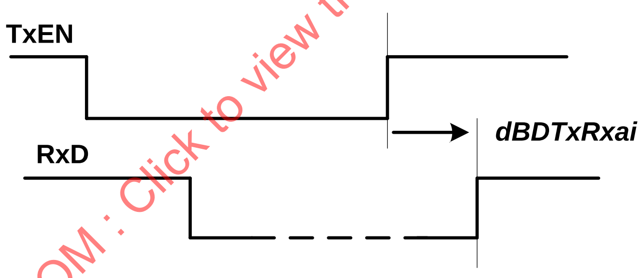
BD operation mode	TxEN	TxD	Resulting signaling on the bus
BD_Normal	high	X [a]	*Idle*
	low	low	*Data_0*
	low	high	*Data_1*
Low power modes	X	X	*Idle*

[a] X = don't care

12.4.5 TxEN – RxD loopback

The time until RxD indicates idle after the end of a transmission needs to be limited in order to ensure that the wakeup protocol mechanism works properly.

Figure 36 depicts the idle-loop delay timing.



Key

RxD Receive data

TxEN Transmit enable not

Figure 36 — Idle-loop delay timing

Table 28 defines the idle-loop delay timing.

Table 28 — Idle-loop delay timing

Name	Description	Min	Max	Unit
dBDTxRxai	Idle-Loop delay [a]	—	325	ns

[a] *dBDTxRxai* is sum of *dBDTxai* (see Table 46) and *dBDRxai* (see Table 54) under the constraint both values cannot be at their maximum at the same time.

12.4.6 Electrical characteristics

12.4.6.1 RxD

The RxD signal of a BD shall meet the definition in Table 29.

Table 29 — RxD signal rise and fall times

Name	Description	Min	Max	Unit
$dBDRxD_{R15} + dBDRxD_{F15}$	Sum of rise and fall time at 15 pF load [a]	—	13	ns
$\mid dBDRxD_{R15} - dBDRxD_{F15} \mid$	Difference of rise and fall time at 15 pF load	—	5	ns
$dBDRxD_{R25} + dBDRxD_{F25}$	Sum of rise and fall time at 25 pF load [a]	—	16,5	ns
$\mid dBDRxD_{R25} - dBDRxD_{F25} \mid$	Difference of rise and fall time at 25 pF load	—	5	ns

[a] 20 % to 80 % of uV_{DIG}. A datasheet for the BD shall state maximum rise and fall time on RxD separately.

It shall be verified by a simulation of the BD that the sum of the rise and fall time at TP4_CC does not exceed the above specified maximum for 25 pF load in case the load is a standard lossless transmission line (with an impedance of 50 Ω and a propagation delay of 1 ns) plus a capacitor of 10 pF to ground instead of being only 25 pF (see Figure 27).

Table 30 defines the RxD signal timing at receiving CC.

Table 30 — RxD signal timing at receiving CC

Description	Condition	Min	Max	Unit
RxD signal sum of rise and fall time at TP4_CC	between 20 % and 80 % uV_{DIG} at 10 pF load at the end of a 50 Ω, 1 ns microstripline	—	16,5	ns
RxD signal difference of rise and fall time at TP4_CC	between 20 % and 80 % uV_{DIG} at 10 pF load at the end of a 50 Ω, 1 ns microstripline	—	5	ns

NOTE The compliance to this maximum needs to be verified by simulation during the design process of the BD. The datasheet shall state a note that this is performed according to this part of ISO 17458 and the entire temperature range of the device has been taken into account. The result of the simulation has to be provided to customer on demand.

12.4.6.2 TxD

The TxD input of a BD shall meet the definition shown in Table 31.

Table 31 — TxD input characteristics

Name	Description	Min	Max	Unit
C_BDTxD	Input capacitance on TxD pin	—	10	pF
uBDLogic_1	Threshold for detecting logical high [a]	—	60	%
uBDLogic_0	Threshold for detecting logical low [a]	40	—	—

[a] Relative to uV_{DIG}, (see 15.3) a hysteresis is not required.

12.5 Bus driver – bus guardian interface (optional)

NOTE This option belongs to the functional classes "Bus driver - bus guardian interface" and "Active Star – bus guardian interface"

The BG is an optional component in a FlexRay node; therefore, the interface to the BG at the BD is also optional. The interface comprises two digital electrical signals: The BGE (Bus Guardian Enable), which is mandatory for this interface, is one input into the BD allowing a BG or a similar supervision unit to disable the transmitter and the RxEN (Receive Enable Not), which is optional, one output from the BD.

The timing characteristics of these signals have been specified in 12.9.

The control function performed by the BGE signal is described in 12.4.3. The BD signals with RxEN (if implemented) whether the communication channel is *Idle* or not.

Table 32 defines the resulting RxEN signal from BD to BG.

Table 32 — Resulting RxEN signal from BD to BG

BD operation mode	Signal on bus wires	WU [a]	RxEN [b]
BD_Normal & *BD_ReceiveOnly*	*Idle*	X	high
	Data_0	X	low
	Data_1	X	low
BD_Standby & *BD_Sleep*	X	detected	low
	X	not detected	high
= All other =	X	X	Product specific

[a] WU =Wakeup event; see 12.10 and 12.11.

[b] The output voltages for logical high and low states are defined in Clause 15.

12.6 Bus driver – host interface

12.6.1 Overview

This interface shall enable the host to control the operation modes of the BD and to read status and diagnosis information from the BD. The bus driver – host interface can be realized either using hard-wired signals or a Serial Peripheral Interface (SPI).

12.6.2 Hard wired signals (Option A)

12.6.2.1 Operation mode control

The interface between the BD and the host comprises of at least two mandatory signals. STBN (Standby NOT) is an input from the host to the BD and ERRN (Error NOT) is an output from the BD to the host.

Table 33 defines the resulting operation mode, when only STBN control input is realized.

Table 33 — Resulting operation mode, when only STBN control input is realized

STBN	Resulting operation mode[a]
high	*BD_Normal*
low	*BD_Standby*
[a] In case no undervoltage conditions overrules the host command.	

Optionally, an EN (Enable) input can be implemented to control further modes.

NOTE This option belongs to the functional classes "Bus driver voltage regulator control" and "Bus driver internal voltage regulator".

Table 34 defines the resulting operation mode, when STBN and EN mode control inputs are realized.

Table 34 — Resulting operation mode, when STBN and EN mode control inputs are realized

STBN	EN	Resulting operation mode[a]
high	high	*BD_Normal*
high	low	*BD_ReceiveOnly*
low	high [b]	*BD_Sleep*
low	low	*BD_Standby*
[a] In case no undervoltage conditions overrules the host command.		
[b] In case the BD has entered *BD_Sleep* it shall not react with a mode change on edges on EN.		

The BD shall perform the mode change within a time span of *dBDModeChange* after the respective edge in STBN or EN, if not prevented by an undervoltage condition.

Table 35 defines the mode transition time.

Table 35 — Mode transition time

Name	Description	Min	Max	Unit
dBDModeChange	Mode transition time after host command	—	100	µs

12.6.2.2 Signalling on ERRN

12.6.2.2.1 Overview

The ERRN signal shows the error status when *BD_Normal* is commanded and shows the wakeup status when *BD_Standby* or *BD_Sleep* (if implemented) is commanded. In *BD_ReceiveOnly* (if implemented) either the wakeup source or the error status is signalled on ERRN, see Table 38 and Figure 37.

Figure 37 depicts the different signalling on ERRN in *BD_ReceiveOnly*.

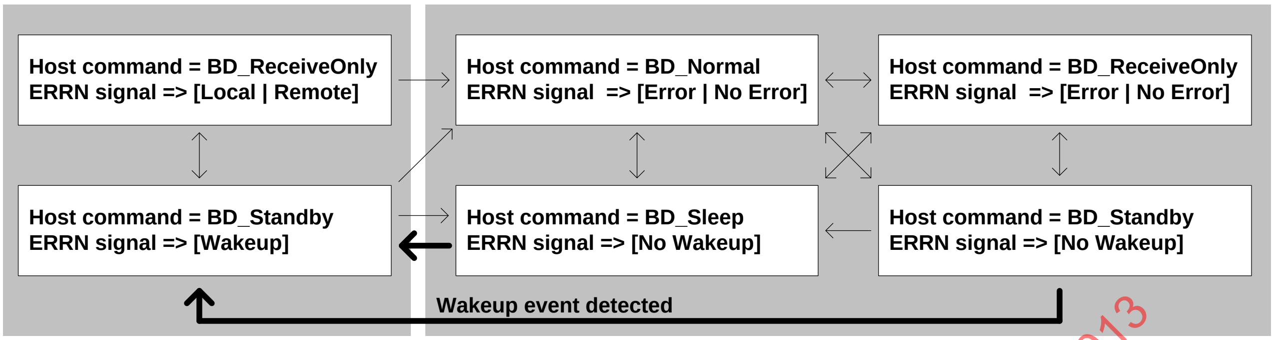


Figure 37 — Different signalling on ERRN in BD_ReceiveOnly

The ERRN signal shall react after detection of an error condition (see 12.12) or after a requested mode change (e.g. to show the wakeup source) within $dReactionTime_{ERRN}$.

It is product specific whether the ERRN returns (when all error conditions have gone) automatically to HIGH or needs to be reset by the host. In case no host action is required by the device the ERRN shall not change its state more than once in a period of $dBDERRN_{Stable}$. Thus detection of errors or recovery of errors may be signalled delayed or not be signalled at all, if the states change faster than this period.

Table 36 defines the mode transition time.

Table 36 — Mode transition time

Name	Description	Min	Max	Unit
$dBDERRN_{Stable}$	Error signaling time on ERRN pin	1	10	µs
$dReactionTime_{ERRN}$	Reaction time on ERRN pin	—	100	µs

12.6.2.2.2 Signalling on ERRN, when only STBN control input available

When a low power mode is commanded via STBN, wakeup events shall be signalled and when a non-low power mode is commanded via STBN errors shall be signalled.

Table 37 defines the signalling on ERRN, when only STBN control input is available.

Table 37 — Signalling on ERRN, when only STBN control input is available

STBN	Condition	Resulting ERRN signal [a]
Error indication		
high	No active failure [b]	high
high	Active failure [b]	low
Wakeup indication		
low	No wakeup detected	high
low	Wakeup detected	low

[a] The output voltages for logical high and low states are defined in 15.2.

[b] Active failure means that one or more of the mandatory error detection mechanisms and/or at least one of the product specific error detection mechanisms (if applicable) have detected an error previously.

12.6.2.2.3 Signalling on ERRN, when STBN and EN are available

Table 38 defines the signalling of failure modes, when STBN and EN mode control inputs are realized.

Table 38 — Signalling of failure modes, when STBN and EN mode control inputs are realized

STBN	EN	Condition	Resulting ERRN signal [a]
Error indication			
high	high	No active failure [b]	high
high	high	Active failure [b]	low
high	low	No active failure [b] and EN has been set to HIGH after previous wakeup	high
high	low	Active failure [b] and EN has been set to HIGH after previous wakeup	low
Wakeup source indication			
high	low	Previous wakeup was initiated local and EN has not been set to HIGH after previous wakeup	high
high	low	Previous wakeup was initiated remote and EN has not been set to HIGH after previous wakeup	low
Wakeup indication			
low	X	No wakeup detected	high
low	X	Wakeup detected	low

[a] The output voltages for logical high and low states are defined in 15.2.

[b] Active failure means that one or more of the mandatory error detection mechanisms and/or at least one of the product specific error detection mechanisms (if applicable) have detected an error previously.

12.6.3 Serial peripheral interface (SPI) (Option B)

In case the interface between the BD and the host comprises of a serial peripheral interface, this interface shall meet the electrical characteristics as described in Clause 15.

Additionally, the BD shall have an interrupt line. The signal name shall be INTN.

Set conditions: The INTN signal shall be switched to logical low when errors occur and also when they recover. In case of reception of wakeup events the INTN shall also be switched to logical low. More product specific events can be signalled.

Reset conditions: The INTN shall only be reset with a correct access to the corresponding error or interrupt register.

The data provided at the SPI interface is product specific.

It shall be possible to command the BD into any of its operation modes and to learn about the error status via the SPI interface.

The BD shall perform the mode change within a time span of $dBDModeChange_{SPI}$ after the rising edge on SCSN, if not prevented by an undervoltage condition.

Table 39 defines the mode transition time.

Table 39 — Mode transition time

Name	Description	Min	Max	Unit
$dBDModeChange_{SPI}$	Mode transition time after host command	—	100	µs
$dBDReactionTime_{SPI}$	Time from detection of an event to falling edge of INTN	—	200	µs

In case the functional class "Bus driver internal voltage regulator" is implemented (only V_{BAT}, no V_{CC} supply) and the device is not in *BD_Off* mode and V_{IO} is not in undervoltage, then the SPI shall be accessible in any operation mode.

In case the functional class "Bus driver internal voltage regulator" is not implemented and V_{CC} is neither in undervoltage nor unsupplied and V_{IO} (if implemented) is not in undervoltage, then the SPI shall be accessible in any operation mode.

12.7 Bus driver – power supply interface

12.7.1 Overview

The interface between the bus driver and the power supply comprises at least two pins, which are the ground connection (GND) and a supply pin, either V_{CC} or V_{BAT}. Furthermore this interface may comprise an optional inhibit output (INH1); see 12.13.

A power supply input "V_{CC}" may be implemented, which shall be connected to a low voltage supply with nominal 5 V. The minimum and maximum allowable voltages on V_{CC} are product specific.

A power supply input "V_{BAT}" may be implemented, which can be directly connected to the vehicle battery (e.g. nominal 42 V) in order to supply the BD, when a V_{CC} input is not supplied or not implemented. The minimum and maximum allowable voltages on V_{BAT} are product specific.

Moreover, there are dependencies to the functional classes "BD voltage regulator control" and "BD internal voltage regulator", see 12.13. Find more information about low voltage conditions in Annex A.

12.7.2 V_{CC} supply voltage monitoring

In case a power supply input V_{CC} is implemented the voltage on the V_{CC} pin shall be monitored. The BD shall autonomously switch to a low power mode when the V_{CC} supply voltage falls below a product specific threshold, which shall be above 4 V. See also 12.3.

Table 40 defines the V_{CC} undervoltage detection parameters.

Table 40 — V_{CC} undervoltage detection parameters

Name	Description	Min	Max	Unit
$dBDUVV_{CC}$	Undervoltage detection time	—	1 000	ms
$dBDRV_{CC}$	Undervoltage recovery time	—	10	ms
$uBDUVV_{CC}$	Undervoltage detection threshold [a]	4	—	V

[a] A hysteresis between detection and recovery threshold can be implemented.

12.7.3 V_{BAT} supply voltage monitoring

In case a power supply input V_{BAT} is implemented the voltage on the V_{BAT} pin shall be monitored. The BD shall autonomously switch to a low power mode when the V_{BAT} supply voltage falls below a product specific threshold, which shall be between 4 V and 5,5 V. See also 12.3.

Table 41 defines the V_{BAT} undervoltage detection parameters.

Table 41 — V_{BAT} undervoltage detection parameters

Name	Description	Min	Max	Unit
$dBDUVV_{BAT}$	Undervoltage detection time	—	1 000	ms
$dBDRV_{BAT}$	Undervoltage recovery time	—	10	ms
$uBDUVV_{BAT}$	Undervoltage detection threshold [a]	4	5,5	V

[a] A hysteresis between detection and recovery threshold can be implemented.

12.7.4 Inhibit output (optional)

This option belongs to the functional classes "Bus driver voltage regulator control" and "Bus driver internal voltage regulator".

Optionally, the bus driver power supply interface may have an inhibit output signal (INH1) that is meant to control an external voltage regulator. The BD signals *Sleep* to the power supply, when leaving the INH1 pin floating and signals *Not_Sleep*, when driving the INH1 pin to battery voltage level.

Table 42 defines the inhibit pin characteristics.

Table 42 — Inhibit pin characteristics

Name	Description	Min	Max	Unit
$uINH1_{Not\_Sleep}$	Voltage on inhibit pin, when signaling *Not_Sleep* at 200 µA load	uV_{BAT} – 1 V	—	V
$iINH1_{Leak}$	Absolute leakage current while signaling *Sleep* [a]	—	10	µA
Prerequisite for all table values: $uV_{BAT} \geq 5,5$ V				
[a] Leakage current can be tested by applying a 100 kΩ to INH1 and checking for | *uINH1* | < 1 V.				

12.8 Bus driver - level shift interface (optional)

12.8.1 Overview

This option belongs to the functional class "Bus driver logic level adaptation".

Optionally, a level shift input V_{IO} can be implemented in order to apply a reference voltage uV_{DIG} for all digital inputs and all digital outputs. In case such reference voltage is available, then $uV_{DIG} = uV_{IO}$, otherwise $uV_{DIG} = uV_{CC}$. For more information, see Clause 15.

12.8.2 V_{IO} voltage monitoring

In case a level shift input "V_{IO}" is implemented the voltage on the V_{IO} pin shall be monitored. The BD shall autonomously switch to a low power mode when the V_{IO} voltage falls below a product specific threshold, which shall be above 2 V, see also 12.3.

Table 43 defines the V_{IO} undervoltage detection parameters.

Table 43 — V_{IO} undervoltage detection parameters

Name	Description	Min	Max	Unit
$dBDUVV_{IO}$	Undervoltage detection time	—	1 000	ms
$dBDRV_{IO}$	Undervoltage recovery time	—	10	ms
uUV_{IO}	Undervoltage detection threshold [a]	2	—	V
[a] A hysteresis between detection and recovery threshold can be implemented.				

12.9 Bus driver - bus interface

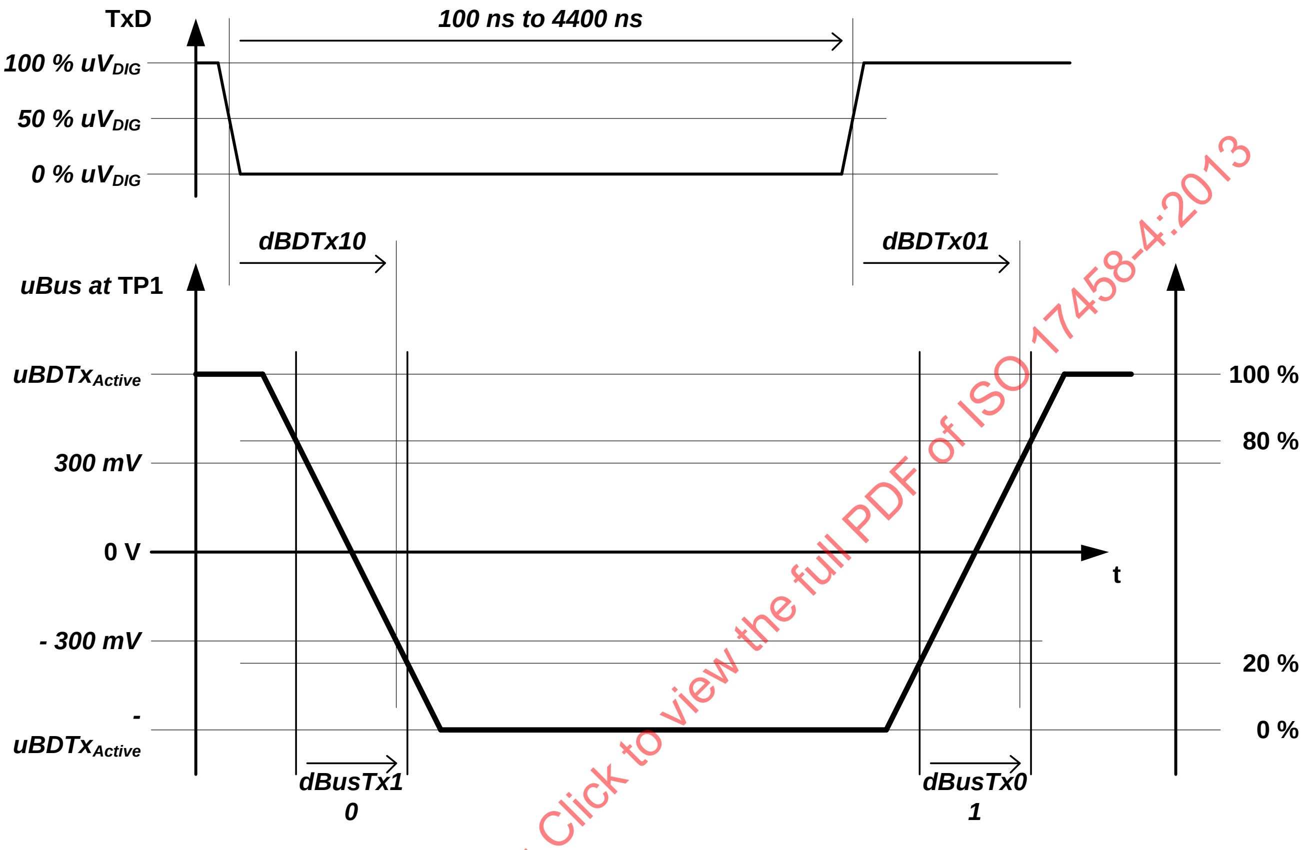
12.9.1 Overview

The interface from the BD to the bus comprises two mandatory functional blocks, which are the receiver and the transmitter. The transmitter can only be activated during *BD_Normal* mode. The receiver shall receive communication elements, when not in a low power mode and maintain the receive function also while the transmitter is active (loop-back). Apart from this the receiver is responsible for biasing the bus in dependence of the power mode, see Table 49. One optional functional block is the ‘remote wakeup event detector’, which is described in 12.11.

12.9.2 Transmitter characteristics

The transmitter delay is defined as the time span for transferring the information of the digital TxD signal (binary data stream) to the analog information (data stream) on the bus as depicted in the following figure.

Figure 38 depicts the transmitter characteristics.



Key

TxD Transmit data

Figure 38 — Transmitter characteristics

Figure 38 is valid while TxEN is a logical low and BGE a logical high (if a BGE signal is available).

The mask test at TP1 shall also be met.

The following table summarizes the transmitter output characteristics that shall be guaranteed, when the TxD signal is constant for 100 ns to 4 400 ns before the first edge and also in case the test is performed with the opposite polarity.

Table 44 defines the transmitter characteristics.

Table 44 — Transmitter characteristics

Name	Description	Min	Max	Unit
$uBDTx_{active}$	Absolute value of *uBus*, while sending [a]	600	2 000	mV
$uBDTx_{idle}$	Absolute value of *uBus*, while Idle [a] [b]	0	30	mV
dBDTx10	Transmitter delay, negative edge [c] [d]	—	75	ns
dBDTx01	Transmitter delay, positive edge [c] [d]	—	75	ns
dBDTxAsym	Transmitter delay mismatch [c] [e] | *dBDTx10* - *dBDTx01* |	—	4	ns
dBusTx10	Fall time differential bus voltage [d] (80 % → 20 %)	6	18,75	ns
dBusTx01	Rise time differential bus voltage [d] (20 % → 80 %)	6	18,75	ns
dBusTxDif	Difference between differential rise and fall time | *dBusTx10* - *dBusTx01* |	—	3	ns

[a] Load on BP/BM: [40..55] Ω || 100 pF.

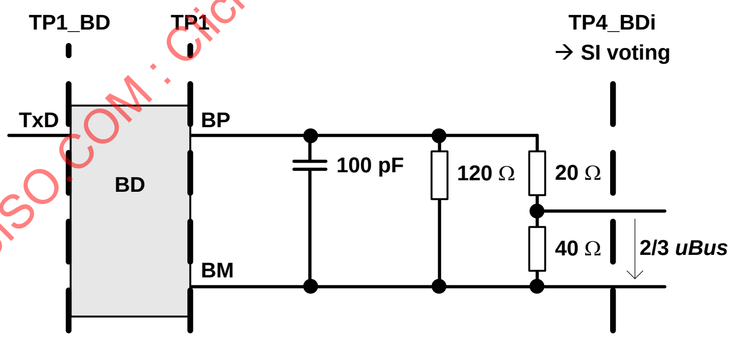
[b] *uBus* shall be measured with a limited bandwidth of 20 MHz before comparing with the limit of $uBDTx_{Idle}$.

[c] For all TxD signals with a sum of rise and fall time (20 % to 80 % uV_{DIG}) of up to 9 ns. See further constraints in Figure 8-5.

[d] Load on BP/BM: 40 Ω || 100 pF.

[e] *dBDTxAsym* shall be guaranteed for ±300 mV as well as for ±150 mV level of *uBus*

With Table 44 and Table 99 follows the system timing at transmitting BD depicted in Figure 39.



Key

BD Bus driver

BM Bus minus

BP Bus plus

TP Test plane

TxD Transmit data

NOTE Sum of rise and fall time on TxD ≤ 9 ns (20 % to 80 % of V_{DIG})

Figure 39 — System timing at transmitting BD

Table 45 defines the system timing at transmitting BD.

Table 45 — System timing at transmitting BD

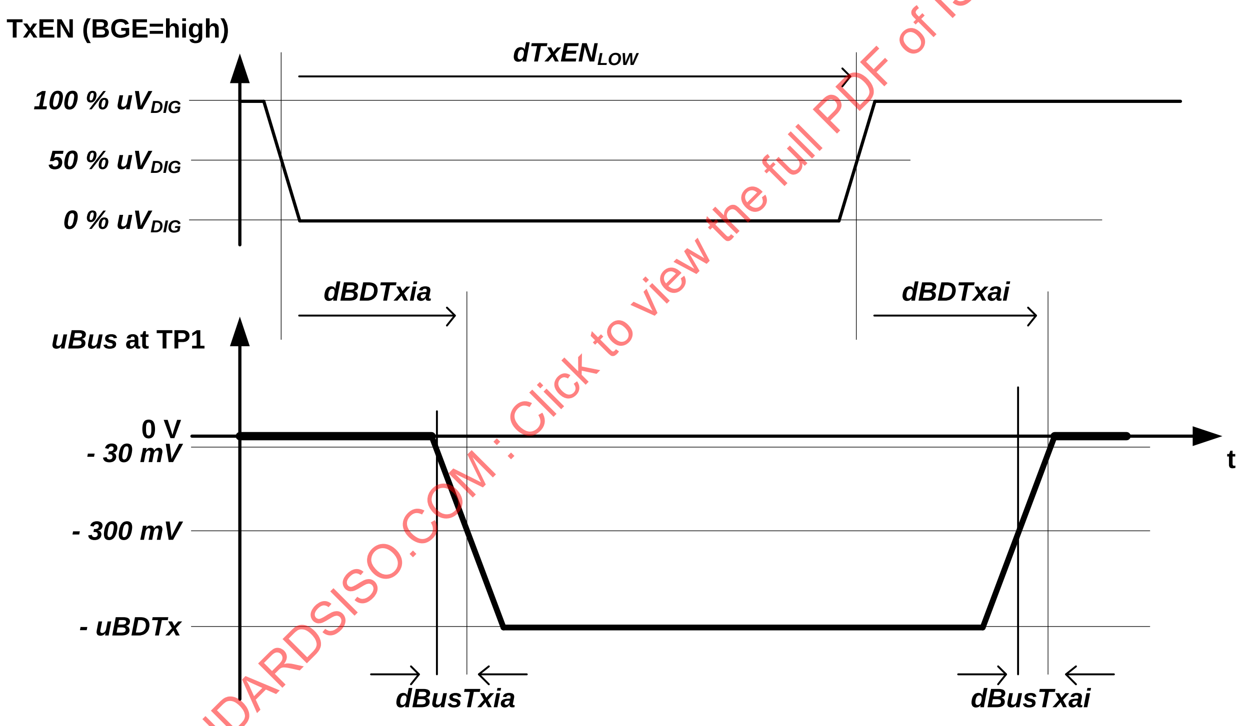
Description	Condition	Required
TP1_BD → TP4_BDi asymmetric delay	2/3 *uBus* voted by the SI-procedure [a] (point-to-point)	pass

[a] The SI-procedure is described in Annex A.

12.9.3 Transmitter behaviour at transition from idle to active and vice versa

The following figure shows the situation at the start and at the end of a transmission with TxD permanent on logical low. The activation of the transmitter via TxEN shall not be possible as long as TxD is on logical high.

Figure 40 depicts the transmitter characteristics at transition from idle to active and vice versa.



Key

BGE Bus guardian enable

TP Test plane

TxEN Transmit enable not

In case a BGE input is not present, behaviour is assumed similar to BGE on logical high level.

Figure 40 — Transmitter characteristics at transition from idle to active and vice versa

Table 46 defines the transmitter characteristics.

Table 46 — Transmitter characteristics

Name	Description	Min	Max	Unit
dBDTxia	Transmitter delay idle -> active	—	75	ns
dBDTxai	Transmitter delay active -> idle	—	75	ns
dBDTxDM [a]	Idle-active transmitter delay mismatch *dBDTxai - dBDTxia*	-50	50	ns
dBusTxia	Transition time idle -> active	—	30	ns
dBusTxai	Transition time active -> idle	—	30	ns
Load on BP/BM: 40 Ω || 100 pF. Equal to TP1 load conditions, see Clause 11.				
[a] This is analogy to the AS parameter *dStarSymbolLengthChange_TxD_Bus*.				

Table 47 defines the transmitter test signal constraint.

Table 47 — Transmitter test signal constraint

Name	Description	Min	Max	Unit
$dTxEN_{LOW}$	Time span of bus activity	550	650	ns

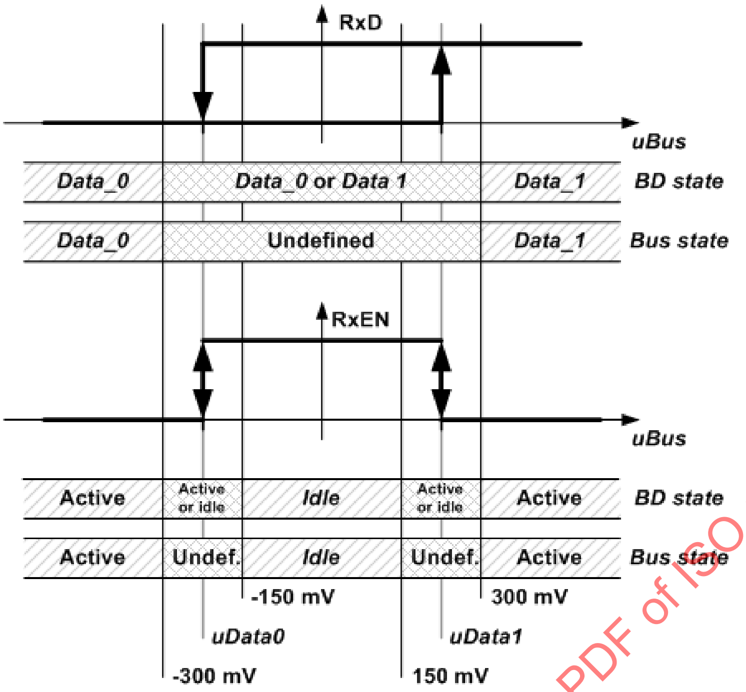
12.9.4 Receiver behaviour (in non-low power mode)

When *uBus* remains less than *uData0* for at least *dBDActivityDetection* after being in *Idle* state, the signals RxD and RxEN (if implemented) will be switched to a logical low state thus indicating that the bus is not in *Idle* state.

When *uBus* remains greater than *uData1* for at least *dBDActivityDetection* after being in *Idle* state, the signal RxEN (if applicable; see 12.5) will be switched to a logical low state, thus indicating that the bus is not in *Idle* state.

When the value of *uBus* remains greater than *uData0* and less than *uData1* for at least *dBDIdleDetection*, the signals RxD (and RxEN if applicable, see 12.5) will be switched to a logical high state, thus indicating that the bus is in *Idle* state.

Figure 41 depicts the RxD behaviour (after activity detection) and RxEN behaviour.



Key

RxD Receive data

RxEN Receive enable not

Figure 41 — RxD behaviour (after activity detection) and RxEN behaviour

The receiver has to distinguish whether *Data_0* or *Data_1* is signalled by the differential voltage *uBus*, after activity has been detected. The principle voltage level scheme is given in Clause 11 in this specification. The receiver can be seen in principle as a high-grade non-linear low pass filter followed by a comparator.

The following table summarizes the receiver characteristics. Additionally the signal diagrams in the subsequent sub clauses give detailed information about timing characteristics.

Table 48 defines the receiver behaviour.

Table 48 — Receiver behaviour

Name	Description	Min	Max	Unit
uData1	Receiver threshold for detecting *Data_1* [a]	150	300	mV
uData0	Receiver threshold for detecting *Data_0* [a]	-300	-150	mV
uData1 - | *uData0* |	Mismatch of receiver thresholds [b]	-30	30	mV
uCM	Common mode voltage range (with respect to GND) that does not disturb the receive function [c] [d]	-10	+15	V
dBDIdleDetection	Bus driver filter-time for idle detection	50	200	ns
dBDActivityDetection	Bus driver filter-time for activity detection	100	250	ns

[a] Prerequisite for detecting *Data_0* or *Data_1* is detection of activity previously. *Data_0* and *Data_1* shall be reliably detected with *uBus* in the range of up to ±3 000 mV.

[b] Test with (*uBP* + *uBM*)/2 = 2,5 V.

[c] *uCM* = (*uBP* + *uBM*)/2. To be tested on a receiving bus driver with a sending bus driver that has a ground offset voltage in the range of [-12,5 V ... +12,5 V] and sends a 50/50 pattern ISO 17458-5.

[d] The given Min. and Max. values are given the minimal range to be covered. The device might cover a larger common mode range.

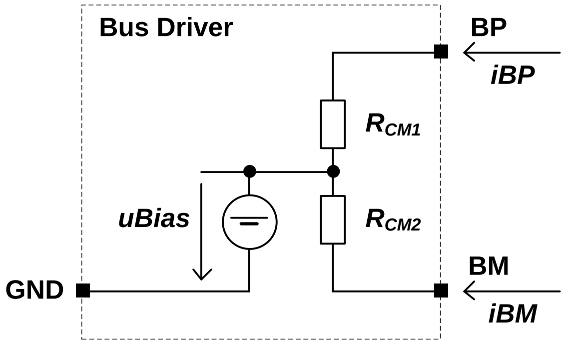
12.9.5 Receiver characteristics

The receiver circuit is responsible for biasing the bus and receiving data streams from the bus.

The minimum analog bit time to be considered is 70 ns, see Table 51.

The receiver's output is the RxD signal; its dependence on the signalling on the bus is given in Table 25.

The electrical equivalent circuit of the biasing part of a receiver is depicted in Figure 42.



Key

BM	Bus minus
BP	Bus plus
GND	System ground
iBM	Current flowing into BM
iBP	Current flowing into BP
uBias	Bus bias voltage[a]
R_{CM}	Input resistance of the common mode[a]

[a] See also Table 49.

Figure 42 — Bus wire biasing circuit – principle schematic

Currents flowing into the BD from the bus wiring harness via pin BP are denoted as *iBP* and those flowing into the BD via pin BM are denoted as *iBM*. The voltages on the pins are *uBP* and *uBM* with respect to GND, as introduced in Clause 7. Mind that currents flowing into the BD have a positive sign.

The required electrical characteristics are given in the following tables.

Table 49 defines the receiver characteristics.

Table 49 — Receiver characteristics

Name	Description	Min	Max	Unit
R_{CM1}, R_{CM2}	Receiver common mode input resistance [a]	10	40	kΩ
uBias	Bus bias voltage during non-low power modes [b]	1 800	3 200	mV
	Bus bias voltage during low power modes [b] [c]	-200	+200	mV
Prerequisite for all values is that BD is connected to GND and uV_{CC} = 5 V (if applicable) and uV_{BAT} ≥ 7 V (if applicable).				
[a] The receiver common mode input resistances on BP and BM can be measured by comparing the voltages *uBP* and *uBM* when unconnected and when connected to ground via 10 kΩ. [b] Load on BP/BM: [40..55] Ω || 100 pF. Nominal voltage of *uBias* is 2 500 mV in *BD_Normal* mode and 0 mV in low power modes. [c] The internal resistance of the *uBias* voltage source in lower power modes can be significantly higher than in non-low power modes.				

Table 50 defines the receiver characteristics (not powered / loss of ground).

Table 50 — Receiver characteristics (not powered / loss of ground)

Name	Description	Min	Max	Unit
iBP_{Leak}	Absolute leakage current, when in *BD_Off* [a]	—	25	µA
iBM_{Leak}	Absolute leakage current, when in *BD_Off* [a]	—	25	µA
$iBP_{LeakGND}$	Absolute leakage current, in case of loss of GND [b]	—	1 600	µA
$iBM_{LeakGND}$	Absolute leakage current, in case of loss of GND [b]	—	1 600	µA

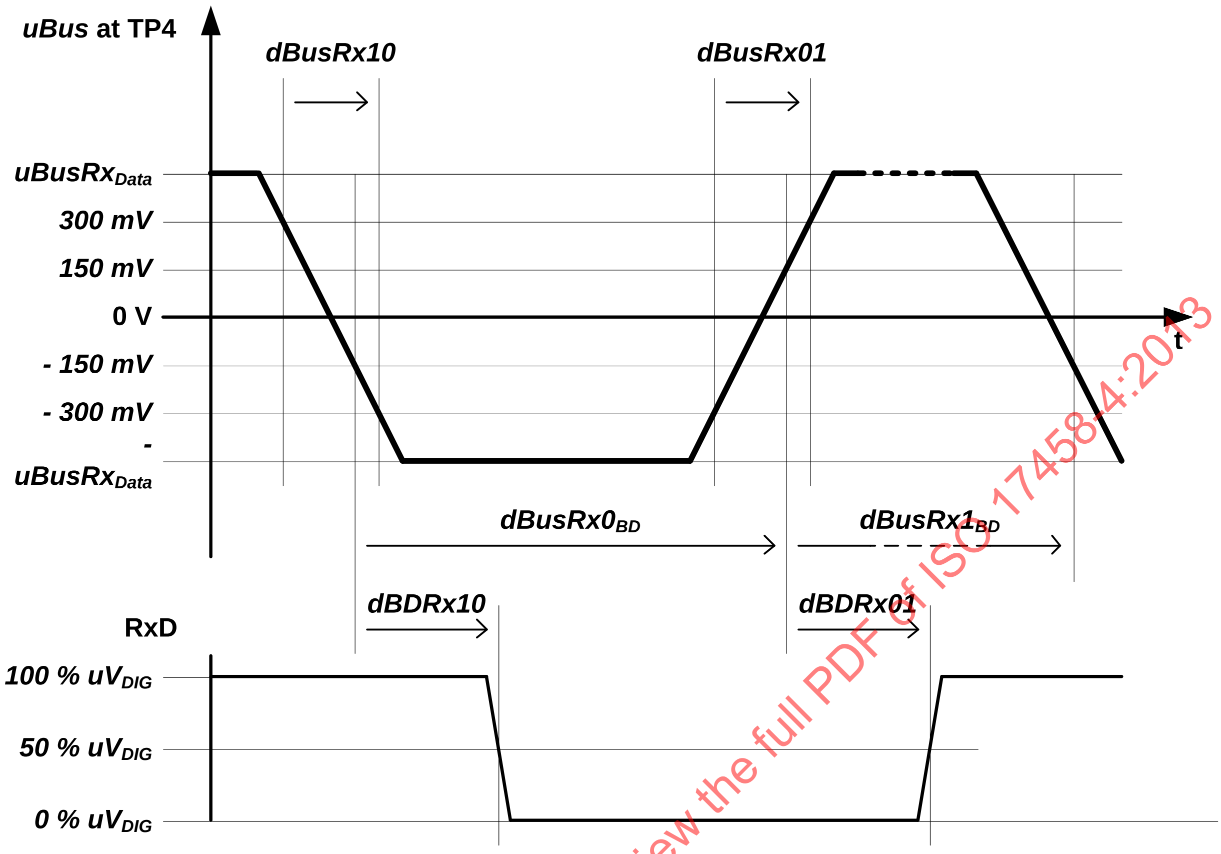
[a] Test conditions: *uBP* = *uBM* = 5 V, all other pins connected to GND. GND pin connected directly to 0 V.

[b] Test conditions: *uBP* = *uBM* = 0 V, all other pins connected via 0 Ω to 16 V.

12.9.6 Receiver timing characteristics

The receiver delay is defined as the time span for transferring the data stream (analog information) from the signal path (bus) to the binary data stream (digital RxD signal) as depicted in the following figure. The voltage notation refers to the definition of test planes as made in 10.3.

The receiver test signal for measuring the characteristics is described in Figure 43.



NOTE1 The voltage *uBus* shall be constant for [100..4 400] ns before the first edge.

NOTE2 The timing requirements shall also be met when testing with the opposite polarity.

Key

TP Test plane

Figure 43 — Receiver timing characteristics

Table 51 defines the receiver input signal for data recognition.

Table 51 — Receiver input signal for data recognition

Name	Description	Min	Max	Unit
$uBusRx_{Data}$	*uBus* at TP4	400	3 000	mV
dBusRx10	Transition time *Data_1* ⇒ *Data_0*	—	22,5	ns
dBusRx01	Transition time *Data_0* ⇒ *Data_1*	—	22,5	ns
$dBusRx0_{BD}$	Time span *Data_0* [a]	70	4 330	ns
$dBusRx1_{BD}$	Time span *Data_1* [a]	70	4 330	ns
[a] 200 ns (± 1 ns) ≤ $dBusRx1_{BD}$ + $dBusRx0_{BD}$ ≤ 4 400 ns (± 1 ns). This includes effects in 2,5 Mbit to 10 Mbit systems.				

The behaviour of the receiver when a signal according to Figure 43 and Table 51 is applied shall be as given in Table 52.

Table 52 — Receiver data timing requirements

Name	Description	Min	Max	Unit
dBDRx10	Receiver delay, negative edge [a]	—	75	ns
dBDRx01	Receiver delay, positive edge [a]	—	75	ns
dBDRxAsym	Receiver delay mismatch [a b] | *dBDRx10 – dBDRx01* |	—	5	ns

[a] Load on RxD: 25 pF – see also 12.4.

[b] *dBDRxAsym* shall be guaranteed for ±300 mV as well as for ±150 mV level of *uBus*.

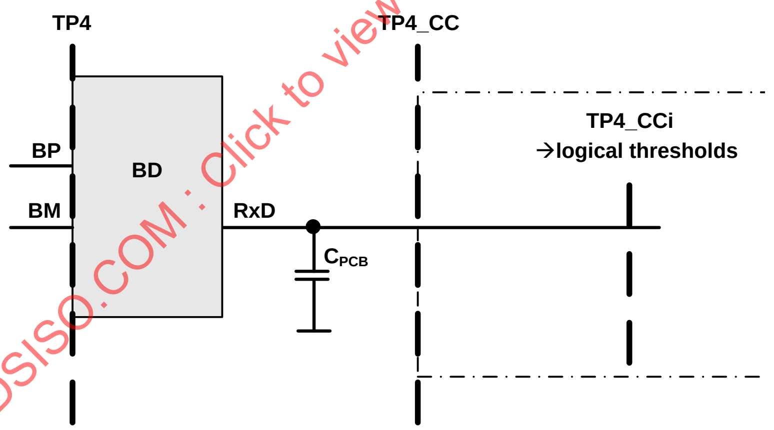
Further timing definitions for the RxD signal are given in 12.4.6.

The above given conditions for the receiver input test signal have the following implicit meaning:

The receiving BD requires that the shortest duration of a single bit shall not be shorter than at least 70 ns at the input (TP4). The system designer has to consider the information given in Clause 12.

From a system perspective it results from Table 29, Table 52 and Table 101:

Figure 44 depicts the system timing at receiving BD.



Key

BD Bus driver

BM Bus minus

BP Bus plus

C_{PCB} Represents the load on the pin that consists of the parasitic capacitance of the printed circuit board and the input pin capacitance of the CC.

RxD Receive data

TP Test plane

Figure 44 — System timing at receiving BD

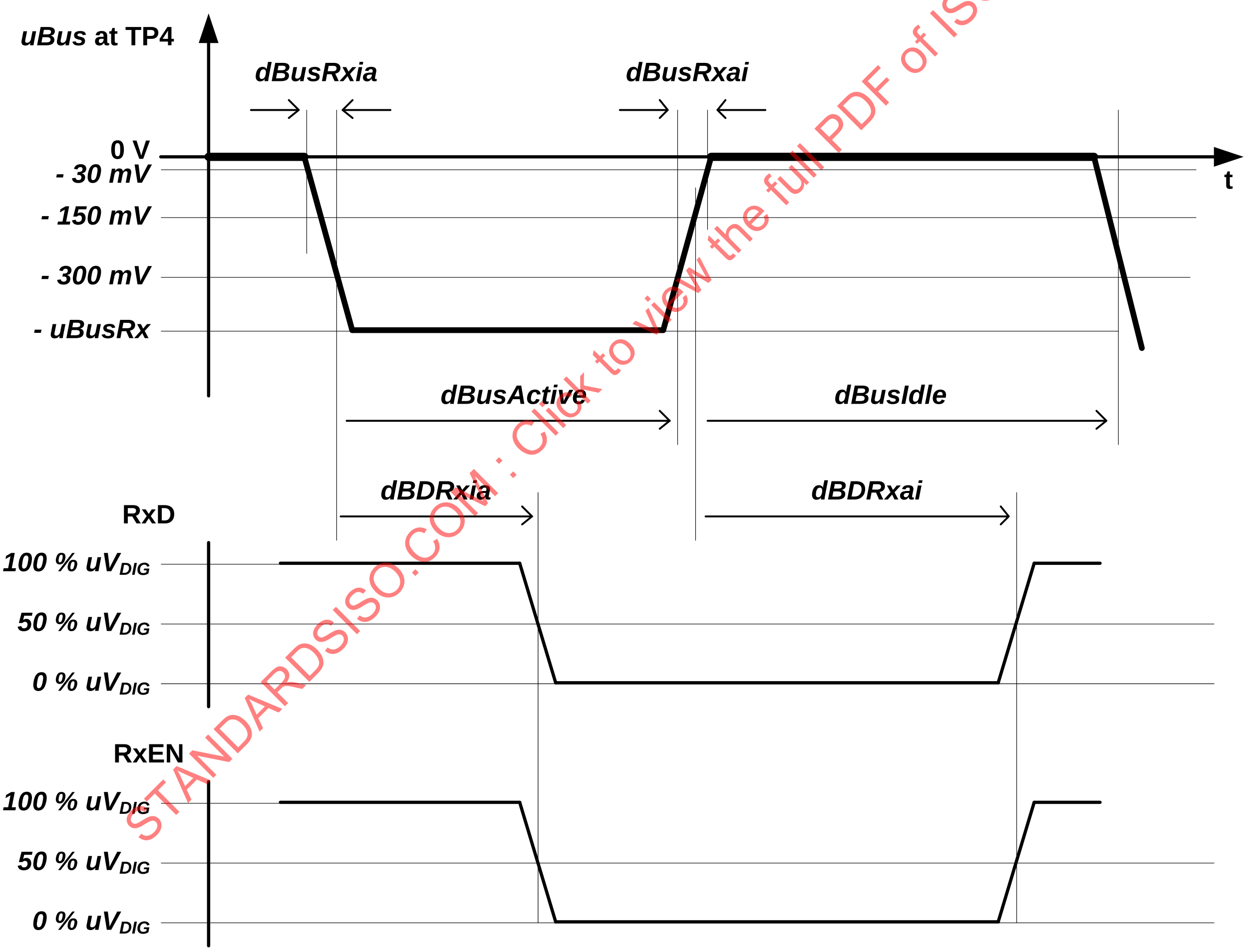
Table 53 defines the resulting receiver timing.

Table 53 — Resulting receiver timing

Description	Condition	Min	Max	Unit
asymmetric delay TP4 → TP4_CCi	measured at 40 % uV_{DIG} at 15 pF load	—	9	ns
	measured at 60 % uV_{DIG} at 15 pF load	—	9	ns
asymmetric delay TP4 → TP4_CCi	measured at 40 % uV_{DIG} at 25 pF load	—	10	ns
	measured at 60 % uV_{DIG} at 25 pF load	—	10	ns

12.9.7 Receiver behaviour at transition from idle to active and vice versa

Figure 45 depicts the receiver behaviour at transition from idle to active and vice versa.



Switching of RxD (and RxEN if applicable) shall be done with less than 10 ns skew.

Key

TP Test plane

Figure 45 — Receiver behaviour at transition from idle to active and vice versa

In case *dBusActive* is shorter than *dBDActivityDetection*, then RxEN shall stay on logical high level.

In case *dBusIdle* is shorter than *dBDIdleDetection*, then RxEN shall stay on logical low level.

Table 54 defines the receiver timing requirements.

Table 54 — Receiver timing requirements

Name	Description	Min	Max	Unit
dBDRxai	Bus driver idle reaction time	50	275	ns
dBDRxia	Bus driver activity reaction time	100	325	ns
These values are equal to *dBDIdleDetection* (or respectively *dBDActivityDetection*) plus a delay for BD's internal logic.				

The values in Table 54 shall be met under the conditions given in Table 55.

Table 55 defines the receiver input signal for activity / idle detection.

Table 55 — Receiver input signal for activity / idle detection

Name	Description	Min	Max	Unit
uBusRx	*uBus* at TP4 during test	400	3 000	mV
dBusRxia	Transition time *Idle* ⇒ *Data_0*	18	22	ns
dBusRxai	Transition time *Data_0* ⇒ *Idle*	18	22	ns
dBusActive	*Data_0* time for test	590	610	ns
dBusIdle	*Idle* time for test	590	610	ns

12.9.8 Receiver behaviour (in low power mode)

While in a low power mode the receiver output RxEN (if implemented) and RxD behave according to 12.4 and 12.5 – indicating wakeup events in case wakeup detectors are implemented and have detected a valid local or remote wakeup. The low power receiver does not need to distinguish between *Idle* and *Data_1*.

Figure 46 depicts the low power receiver behaviour.

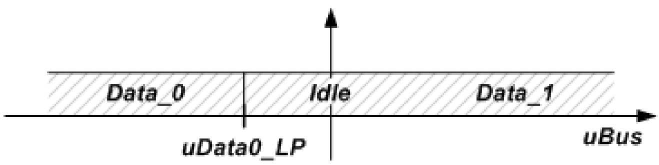


Figure 46 — Low power receiver behaviour

Table 56 defines the low power receiver behaviour.

Table 56 — Low power receiver behaviour

Name	Description	Min	Max	Unit
uData0_LP	Low power receiver threshold for detecting *Data_0*	-400	-100	mV
Prerequisite: V_{BAT} ≥ 7 V (if applicable, otherwise V_{CC} = 5 V) In case the BD implementation uses the full range up to -400 mV, then there is no margin to the minimum differential voltage on TP4.				

12.9.9 Bus driver - bus interface behaviour, when in *BD_Off* mode

In case no supply voltage is available, the electrical behaviour of the transmitter and receiver shall be like in a low power mode. However, the values for R_{CM1} and R_{CM2} may exceed the maximum value as given in Table 49.

Mind also the maximum leakage currents defined in Table 50.

12.9.10 Bus driver - bus interface behaviour under short-circuit conditions

The current flowing from the BD into the bus wires, when actively transmitting *Data_0* or *Data_1* shall be limited in case of short-circuits as given in Table 57.

Table 57 — Current limitations

Name	Description	Min	Max	Unit
$iBP_{BMShortMax}$, $iBM_{BPShortMax}$	Absolute maximum output current when BP shorted to BM – no time limit	—	60	mA
$iBP_{GNDShortMax}$, $iBM_{GNDShortMax}$	Absolute maximum output current when shorted to GND – no time limit	—	60	mA
$iBP_{-5VShortMax}$, $iBM_{-5VShortMax}$	Absolute maximum output current when shorted to –5 V – no time limit	—	60	mA
$iBP_{BAT27ShortMax}$, $iBM_{BAT27ShortMax}$	Absolute maximum output current when shorted to 27 V – no time limit	—	60	mA
$iBP_{BAT48ShortMax}$, $iBM_{BAT48ShortMax}$	Absolute maximum output current when shorted to 48 V [a] – no time limit	—	72	mA
$iBP_{BAT60ShortMax}$, $iBM_{BAT60ShortMax}$	Absolute maximum output current when shorted to 60 V for maximum 400 ms [a] [b]	—	90	mA
"shorted" means a connection with at most 1 Ω. For test purposes the short-circuit condition shall remain at least 1 500 µs.				
[a] These limitations are only valid for devices that are meant to be used in "42 V board net" systems.				
[b] 400 ms originated from load dump conditions.				

12.9.11 Bus driver - bus interface simulation model parameters

For the purpose of simulation, the BD's product datasheet shall give minimum, maximum and typical value for the equivalent output impedance (single ended) $R_{BDTransmitter}$, which is a parameter in the 'generic BD simulation model' as defined by the FlexRay consortium; see Annex A.

The formula to calculate the equivalent output impedance of the bus driver is shown in Equation 2.

$$R_{BDTransmitter} = 50\,\Omega \times (uBus_{100} - uBus_{40}) / (2{,}5 \times uBus_{40} - uBus_{100}) \quad (2)$$

where

$uBus_{40}$ is the differential output voltage on a load of 40 Ω || 100 pF, when driving a Data_1;

$uBus_{100}$ is the differential output voltage on a load of 100 Ω || 100 pF;

$R_{BDTransmitter}$ is the equivalent output impedance of the bus driver.

12.10 Bus driver – wakeup interface (optional)

12.10.1 General

This option belongs to the functional classes "BD voltage regulator control" and "Bus driver internal voltage regulator".

12.10.2 Wakeup via dedicated WAKE pin

The BD can have a WAKE input in the wakeup detector. The operating voltage on WAKE shall be the same as for V_{BAT}. A negative pulse on this pin shall be recognized as wakeup event, when the BD is in a low power mode. A positive pulse may optionally also be detected and recognized as a valid wakeup event.

Table 58 defines the timing constraint for wakeup pulse on the WAKE pin.

Table 58 — Timing constraint for wakeup pulse on the WAKE pin

Name	Description	Min	Max	Unit
dBDWakePulseFilter	Wake pulse filter time (spike rejection)	1	500	µs

The behaviour after detection of a wakeup event is specified in 12.3. For wakeup signalling mechanisms see 12.4 and 12.6.

12.10.3 Local wakeup operating requirements

The wakeup detector shall be operable if uV_{BAT} is equal to or greater than $uV_{BAT\text{-}WAKE}$ even if V_{CC} is not implemented or unsupplied. See also 12.3.

Table 59 defines the operating constraints for local wakeup.

Table 59 — Operating constraints for local wakeup

Name	Description	Min	Max	Unit
$uV_{BAT\text{-}WAKE}$	Minimum required voltage for detecting local wakeup events	—	7	V
$dBDWakeupReaction_{local}$	Reaction time after wakeup	—	100	µs

With a wakeup reaction time of a maximum 100 µs, the BD has to show a reaction latest 600 µs (=*dBDWakePulseFilter* + $dBDWakeupReaction_{local}$) after the initial edge of the wake pulse on the WAKE pin.

For wakeup signalling mechanisms see 12.4, 12.5 and 12.6.

12.11 Remote wakeup event detector (optional)

NOTE This option belongs to the functional class "Bus driver remote wakeup"

12.11.1 Wakeup with wakeup patterns independent of data rate

The remote wakeup event detector shall ensure that the BD is woken with the wakeup patterns as described in 6.8. The reaction of the BD of a remote wakeup event is defined in 12.3.

Wakeup detection upon reception of communication is favoured but not explicitly required. Consequently a BD may be woken-up by frames with payloads that differ from the payload that is defined in the following subclause, especially at data rates lower than 10 Mbit/s.

12.11.2 Wakeup with frames in 10 Mbit/s systems

NOTE Wakeup at lower speeds shall be done with "Wakeup During Operation Pattern (WUDOP)", see ISO 17458-2

It shall be possible to initiate a wakeup by receiving a frame sent with a speed of 10 Mbit/s and carrying the following 36 bytes payload content:

```
0xFF  0xFF  0xFF  0xFF  0xFF  0x00  0x00  0x00  0x00  0x00
0xFF  0xFF  0xFF  0xFF  0xFF  0x00  0x00  0x00  0x00  0x00
0xFF  0xFF  0xFF  0xFF  0xFF  0x00  0x00  0x00  0x00  0x00
0xFF  0xFF  0xFF  0xFF  0xFF  0xFF
```

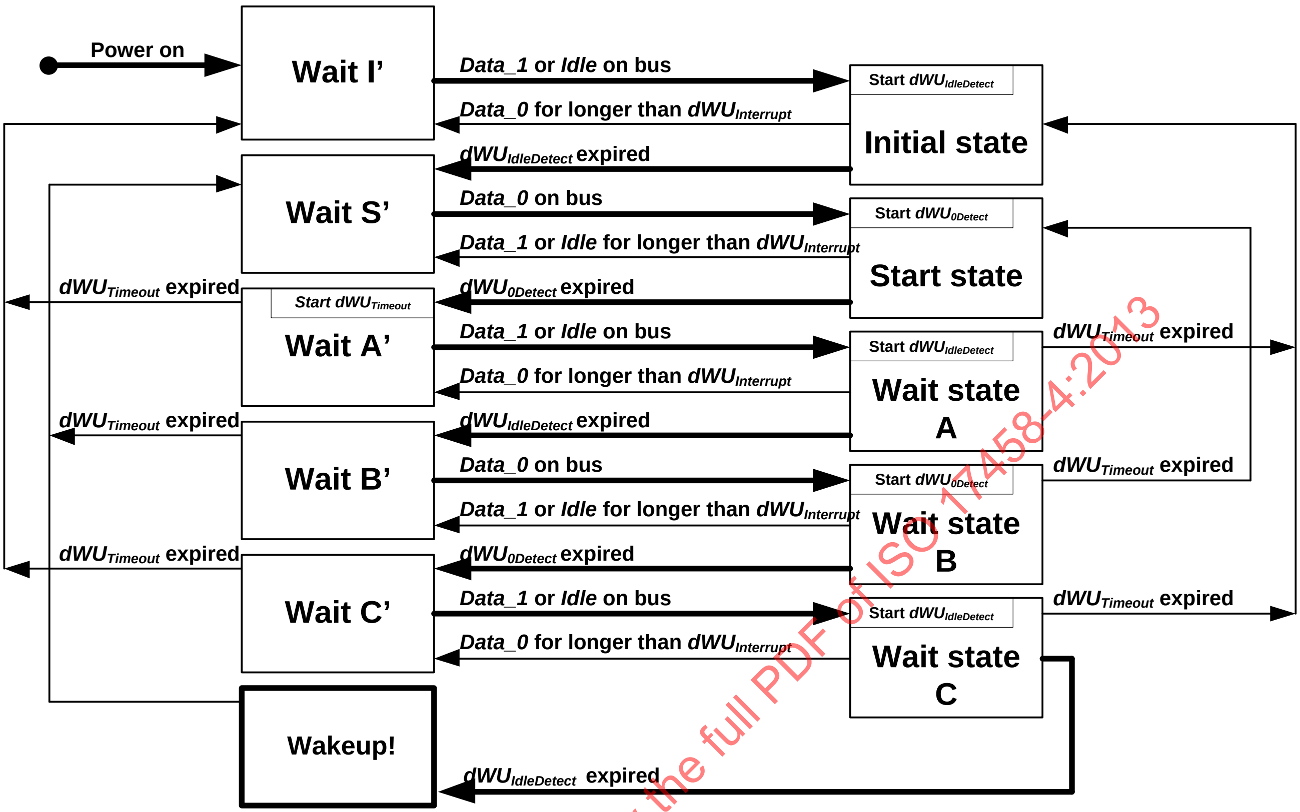
The reaction of the BD to a remote wakeup event is defined in 12.3.

12.11.3 Wakeup state machine

In order to ensure the behaviour as described above and the detection of the wakeup patterns as described in 6.8, the implementation of the bus driver shall follow the procedure of the state diagram in Figure 47, but the implementation may differ from this state diagram. The physical layer conformance test will test the behaviour with some ‘valid’ and some ‘non-valid’ wakeup patterns see ISO 17458-5.

The event driven state machine shall be active, when the BD is not in *BD_Off*. This ensures that no wakeup event is overlooked, in case the BD changes from a non-low power mode to a low power mode, while a wakeup pattern is sent. Entering the Wakeup! state initiates a wakeup event (see transition 1 in Figure 35) and is left immediately without further conditions.

Figure 47 depicts the wakeup state machine.



NOTE1 Start = Start at zero

NOTE2 The thick arrows indicate the nominal process of wakeup pattern detection.

Figure 47 — Wakeup state machine

Table 60 defines the wakeup state machine timings.

Table 60 — Wakeup state machine timings

Name	Description	Min	Max	Unit
$dWU_{0Detect}$	Acceptance timeout for detection of a *Data_0* phase in wakeup pattern	1	4	µs
$dWU_{IdleDetect}$	Acceptance timeout for detection of a *Idle* or *Data_1* phase in wakeup pattern	1	4	µs
$dWU_{Timeout}$	Acceptance timeout for wakeup pattern recognition	48	140	µs
$dWU_{Interrupt}$	Acceptance timeout for interruptions	0,13 [a]	1	µs

[a] The minimum value is only guaranteed, when the phase that is interrupted was continuously present for at least 870 ns.

12.11.4 Remote wakeup operating requirements

In case a V_{BAT} supply voltage input is implemented, the remote wakeup event detector shall be operable if uV_{BAT} is equal to or greater than $uV_{BAT\text{-}WAKE}$. See also 12.3.

Table 61 defines the operating constraints for remote wakeup.

Table 61 — Operating constraints for remote wakeup

Name	Description	Min	Max	Unit
$uV_{BAT\text{-}WAKE}$	Minimum required voltage for detecting remote wakeup events, when V_{CC} input implemented	—	7	V
$uV_{BAT\text{-}WAKE}$	Minimum required voltage for detecting remote wakeup events, when V_{CC} input not implemented	—	5,5	V
$dBDWakeupReaction_{remote}$	Reaction time after wakeup	—	100	µs

With a wakeup reaction time of a maximum 100 µs, the BD has to show a reaction latest 104 µs (= $dWU_{IdleDetect}$ + $dBDWakeupReaction_{remote}$) after the end of the second *Data_0* phase of the wakeup pattern.

The behaviour after detection of a wakeup event is specified in 12.3. For wakeup signalling mechanisms see 12.4 and 12.6.

12.12 Bus driver behaviour under fault conditions

12.12.1 Environmental errors

This paragraph sketches the behaviour of the BD under fault conditions resulting from the functional features that are specified in the foregoing subclauses of this subclause. See also 12.6 for error signalling and wake (source) signalling, which both are done competing via the ERRN signal, when host interface option A is implemented.

Table 62 defines the BD behaviour under fault conditions.

Table 62 — BD behaviour under fault conditions

Fault description	Behaviour at BP and BM	Behaviour at BD's digital interfaces
BD is without any supply voltage (*BD_Off* mode)	high impedance, see Table 50	See Table 104, last row
Undervoltage on all supply voltages, but not unsupplied	BD shall not force a differential voltage on BP/BM. [a]	Signaling on ERRN or INTN required as specified in 12.6
Undervoltage on V_{BAT} (uV_{CC} available)	BD shall not force a differential voltage on BP/BM. [a] Note BD may not be able to detect wakeup symbols.	Signaling on ERRN or INTN required as specified in 12.6
BD looses connection to channel (BP and BM interrupted)	BD shall detect the channel to be *Idle*, while its TxEN is on logical high.	RxD behaviour according to 12.4 is required.
BP line shorted to ground	BD shall internally limit the output current, see Table 57.	Signaling on ERRN or INTN required as specified in 12.6 in case it is not possible to send data on the bus. For bus failure detection see 12.12.5.
BP line shorted to supply voltage		
BM line shorted to ground		
BM line shorted to supply voltage		
BP line shorted to BM line		
Error or interrupt signaling line becomes interrupted	—	No detection by BD. If the ERRN or INTN does not react on a mode change as expected, the host can assume that the line is clamped. For INTN and ERRN behaviour see 12.6.
Error or interrupt signaling line is shorted to ground	—	
Error or interrupt signaling line is shorted to V_{IO} or V_{CC} voltage [b]	—	
TxD line becomes interrupted	BD outputs *Data_0*, when enabled via TxEN (and BGE, if applicable).	RxD behaviour according to 12.4 is required. For TxD and TxEN see Table 63.
TxEN line becomes interrupted	BD shall not force a differential voltage on BP/BM. [a]	
TxEN signal is permanently asserted [c]	After a timeout (see 12.4) expires the BD shall not force a differential voltage on BP/BM.	After timeout expires (see 12.4) signaling on ERRN or INTN required as specified in 12.6.
BD detects an over-temperature condition [c]	BD shall not force a differential voltage on	Signaling on ERRN or INTN required as

Fault description	Behaviour at BP and BM	Behaviour at BD's digital interfaces
	BP/BM. [a]	specified in 12.6.
One of two channel termination units becomes disconnected from the channel	Note: Depending on use case specifics the communication will drop out or might continue with a huge amount of errors.	—
Bus load too high (= Resistance R_{DCLoad} too low, see 8.7)	Note: Depending on use case specifics the communication will drop out or might continue with degraded performance.	—
Undervoltage on V_{IO}	BD shall not force a differential voltage on BP/BM. [a]	See 15.2.
Loss of ground [d]	BD shall internally limit the output current, see Table 50.	Product-specific behaviour.

a Biasing depends on the operation mode, see Table 49.

b Host will see ERRN = high in this special case, independent of presence of other errors.

c Detection only required when BD is in *BD_Normal* mode.

d 'Loss of ground' is when the GND pin is unconnected and none of the digital I/Os is forced to GND level.

12.12.2 Behaviour of unconnected digital input signals

In case one or more of the digital inputs are unconnected (or floating) the BD shall sense the inputs as defined in Table 63.

Table 63 — Logical input when unconnected

Signal	Logical input
TxD	low
TxEN	high
STBN [a]	low
EN [a]	low
BGE [b]	low

a If host interface according to option A is implemented, see 12.6.

b If bus driver – bus guardian interface is implemented, see 12.5.

This behaviour leads to a fail silent behaviour of the BD, when TxEN or BGE are floating. It also assures that the BD is forced into *BD_Standby* mode, when STBN and the EN input are floating. In case TxD is floating *Data_0* is sent, while the BD is enabled for transmission, thus the CCs in the receiving ECUs can detect that the bus is not in *Idle* state. The behaviour of unconnected digital input pins of a SPI is defined in 15.8.2.

12.12.3 Behaviour with dynamic low battery voltage

NOTE Only applicable for bus drivers that implement the functional class "Bus driver voltage regulator control"

In case the battery voltages shows a dynamic (temporal) breakdown, e.g. due to engine crank, a BD with a battery connection V_{BAT} shall not change the operation mode, when V_{CC} and V_{IO} (if applicable) are constantly on their lowest level that does not lead to an undervoltage detection according to the BD's datasheet. The BD shall not detect an undervoltage condition and shall not signal the occurrence of an error.

For typical applications it is assumed that a notch at V_{ECU} does not lead to a notch in V_{BAT} and also V_{CC} and V_{IO} are stable; see Annex A.

Figure 48 depicts the dynamic low battery voltage.

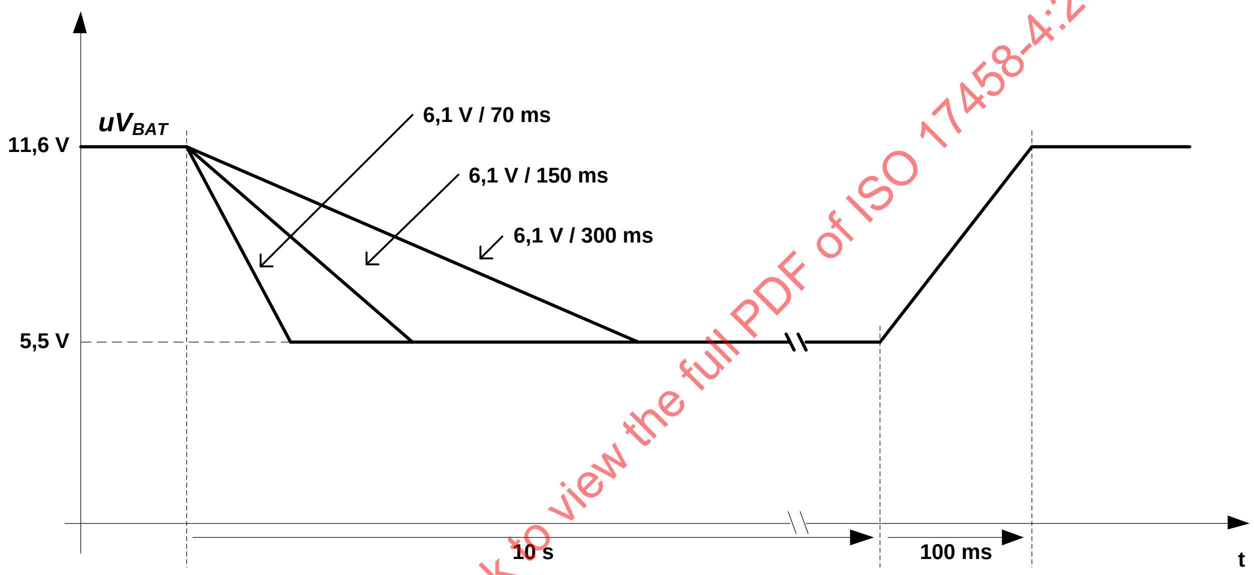


Figure 48 — Dynamic low battery voltage

12.12.4 Behaviour with dynamic low supply voltage

In case the supply voltage of a BD ramps up and down slowly and also in case there are two supply voltages ramping synchronously the BD shall react on undervoltage according to 12.3. In case V_{BAT} (if applicable) and V_{CC} (if applicable) are ramping down in undervoltage conditions, but not causing the BD to enter *BD_Off*, and ramping up again the BD shall not hang up, when V_{IO} (if applicable) is constantly supplied with the product specific minimum operating voltage according to the BD datasheet.

The BD shall be in *BD_Normal* at the end of the supply voltage notch, in case a BD-host interface according option A (hard-wired) is implemented and STBN and EN (if applicable) are constantly on logical HIGH level.

The BD shall be in *BD_Standby* at the end of the supply voltage notch, in case a BD-host interface according option B (SPI) is implemented, SCSN is constantly on logical HIGH level and *BD_Sleep* is not implemented.

The BD shall be in *BD_Sleep* at the end of the supply voltage notch, in case a BD-host interface according option B (SPI) is implemented, SCSN is constantly on logical HIGH level and *BD_Sleep* is implemented.

Four different scenarios have to be considered in case both V_{BAT} and V_{CC} supply inputs are implemented:

— Fast V_{BAT} voltage drop with 7,6/5 V/ms

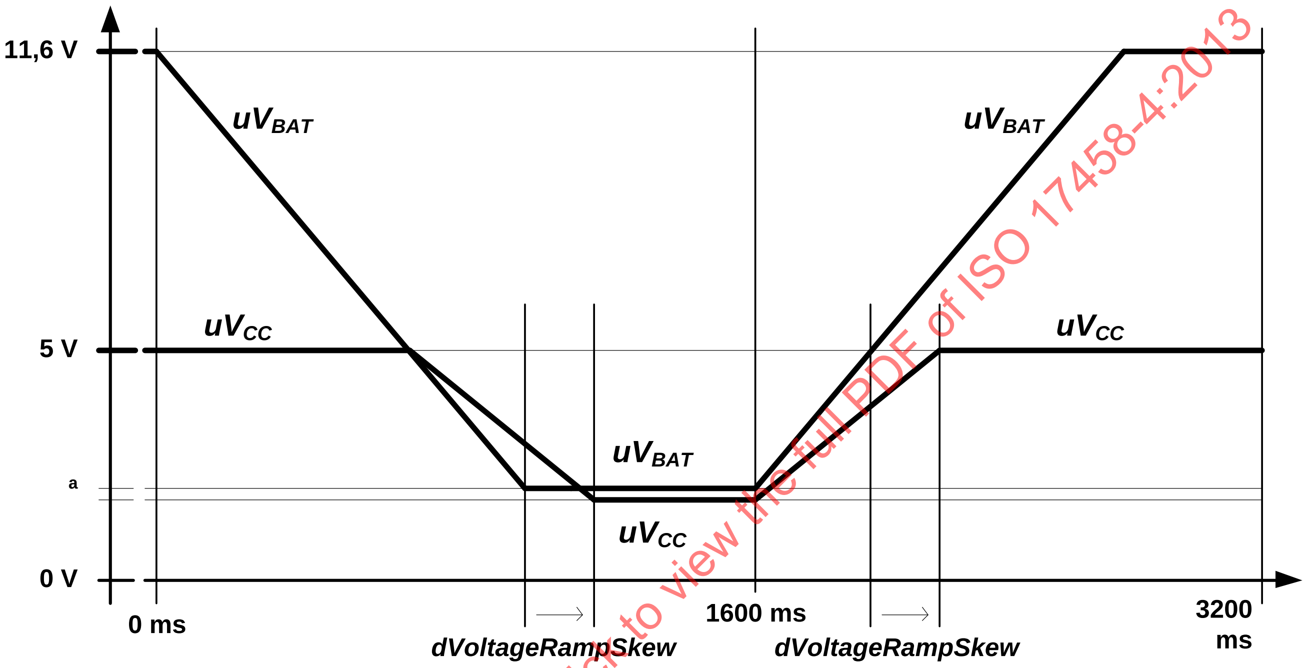
— Slow V_{BAT} voltage drop with 6,1/300 V/ms

combined with the variation

— $V_{CC} = V_{BAT}$, when $V_{BAT} \leq 5$ V (V_{CC} follows V_{BAT}; *dVoltageRampSkew* = 0 ms)

— $V_{CC} > V_{BAT}$, when $V_{BAT} < 5$ V (V_{CC} voltage falls/raises slower than V_{BAT} voltage; *dVoltageRampSkew* = 65 ms)

Figure 49 depicts the dynamic low supply voltage.



a The minimum voltage applied on V_{BAT} and on V_{CC} equals the product specific minimum undervoltage detection threshold voltage according to the devices datasheet.

Figure 49 — Dynamic low supply voltage

Table 64 defines the dynamic low supply voltage constraints.

Table 64 — Dynamic low supply voltage constraints

Name	Description	Min	Max	Unit
slV_{BAT}	Absolute slope of V_{BAT} voltage	0,02	1,52	V/ms
dVoltageRampSkew	Time skew in reaching end of slope	0	65	ms

The bus driver shall signal an undervoltage error latest 1 000 ms after *dVoltageRampSkew* has been started; see also Table 62. It is required that there is not back sourcing of V_{BAT} in case $uV_{CC} > uV_{BAT}$.

12.12.5 Bus failure detection

The BD shall provide a means to detect bus failures while actively sending. An internal error flag shall be updated latest with the rising edge on TxEN. Signalling of the error flag via ERRN or INTN is required according to 12.6. A single indication "bus failure detected" is sufficient to fulfil this FlexRay requirement. See also Table 62.

12.12.6 Over-temperature protection

The BD shall provide a means to monitor the junction temperature on the silicon die. If a certain product specific threshold is exceeded, the BD shall disable the transmitter in order to prevent further heating of the chip. When the over-temperature condition is no longer valid the transmitter shall be enabled at the next edge at TxEN. Entering a low power mode on over-temperature is not acceptable. The receive function shall be maintained as long as possible. The BD shall provide over-temperature information on the bus driver - host interface.

NOTE The over temperature protection is only meant as protection mechanism for the BD.

12.13 Bus driver functional classes

12.13.1 Overview

Each functional class combines a set of specified options, which have to be coexistent when the respective functional class is implemented. These functional classes can be implemented in order to enhance the set of functional features of FlexRay physical layer devices.

12.13.2 Functional class "Bus driver voltage regulator control"

This functional class requires the following options to be implemented in coexistence:

— "V_{CC}" power supply input; see 12.7

— "V_{BAT}" power supply input; see 12.7

— "INH1" output signal; see 12.7.3

— *BD_Sleep* mode; see 12.2.

— EN as second mode control pin, in case the host interface is not a SPI.

— Implementation of the functional class 'Bus driver remote wakeup'

Optionally, a WAKE input pin according to 12.10 may be implemented in this functional class.

12.13.3 Functional class "Bus driver - bus guardian interface"

This class requires the interface as described in 12.5.

12.13.4 Functional class "Bus driver internal voltage regulator"

This functional class requires the following options to be implemented:

— "V_{BAT}" power supply input; see 12.7

— "INH1" output signal, see 12.7

— *BD_Sleep* mode, see 12.2

— EN as second mode control pin, in case the host interface is not a SPI.

Optionally, a WAKE input pin according to 12.10 may be implemented in this functional class.

Optionally, the functional class "Bus driver logic level adaptation" may be implemented in this functional class.

Optionally, the functional class "Bus driver remote wakeup" may be implemented in this functional class.

Optionally, the group including following options may be implemented in this functional class.

This functional class requires that no "V_{CC}" supply input is present.

12.13.5 Functional class "Bus driver logic level adaptation"

This class requires the implementation of a bus driver level shift interface and requires that the thresholds of all digital inputs are controlled by this voltage as well as all digital outputs are related to this voltage level. See also 12.8 and Clause 15.

12.13.6 Functional class "Bus driver remote wakeup"

This class requires the implementation of the option "Remote wakeup event detector", see 12.11.

12.13.7 Functional class "Bus driver increased voltage amplitude transmitter"

This class does not require additional functions to be implemented. However, the minimum of $uBDTx_{Active}$ shall be 900 mV and thus different from the minimum value stated in Table 44. The mask test as defined in 11.2.3 needs to be fulfilled.

12.14 Bus driver signal summary

Table 65 defines the bus driver signal summary.

Table 65 — Bus driver signal summary

Signal	I/O	Description	Mandatory	Controllable	Observable
Bus driver – communication controller Interface					
TxEN	Input	Transmit data enable not	Yes	Yes	Not applicable
TxD	Input	Transmit data input	Yes	Yes	Not applicable
RxD	Output	Receive data output	Yes	Not applicable	Yes
Bus driver - host Interface (option A)					
STBN	Input	Mode control input	Yes [a]	Yes	Not applicable
EN	Input	Mode control input	No	If implemented	Not applicable
ERRN	Output	BD error condition indication	Yes [a]	Not applicable	If implemented
Bus driver - host Interface (option B)					
SCSN	Input	Chip Select input	Yes [b]	If implemented	Not applicable
SCK	Input	SPI clock input	Yes [b]	If implemented	Not applicable
SDI	Input	SPI data input	Yes [b]	If implemented	Not applicable
SDO	Output	SPI data output	Yes [b]	Not applicable	If implemented
INTN	Output	Interrupt	Yes [b]	Not applicable	If implemented
Bus driver - bus guardian Interface (optional)					
BGE	Input	BG enable input	No	If implemented	Not applicable
RxEN	Output	Receive data enable not output	No	Not applicable	If implemented
Bus driver - bus interface					
BP	Input/Output	Bus line Plus	Yes	Yes	Yes
BM	Input/Output	Bus line Minus	Yes	Yes	Yes
Bus driver - power supply interface (optional)					
INH1	Output	Control signal to power supply	No	Not applicable	Not applicable
other					
GND	—	Primary supply voltage ground	Yes	Yes	Not applicable
V_{CC}	—	Primary supply voltage input	Yes [c]	If implemented	Not applicable
V_{BAT}	—	Secondary supply voltage input	Yes [d]	If implemented	Not applicable
V_{IO}	—	IO-Level sensing input	No	If implemented	Not applicable
WAKE	Input	Local Wake input	No	If implemented	Not applicable

[a] Yes when option A is implemented

[b] Yes when option B is implemented

[c] mandatory, if V_{BAT} is not implemented

[d] mandatory, if V_{CC} is not implemented

13 Active Star

13.1 Overview

The basic functionality of the active star is to retransmit a data stream that is received on one branch to all other branches as indicated in Figure 50.

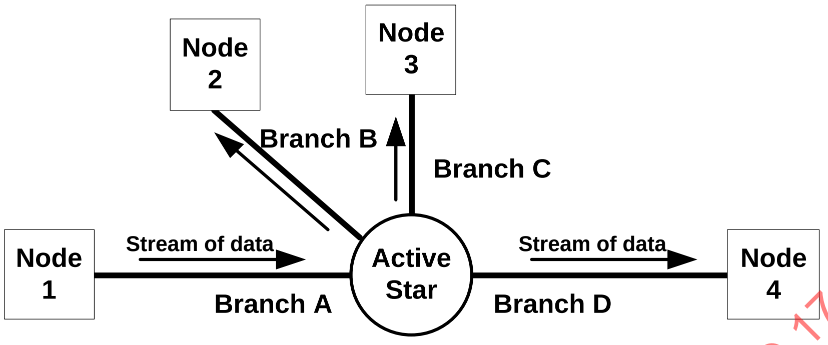


Figure 50 — Active Star transfer functionality

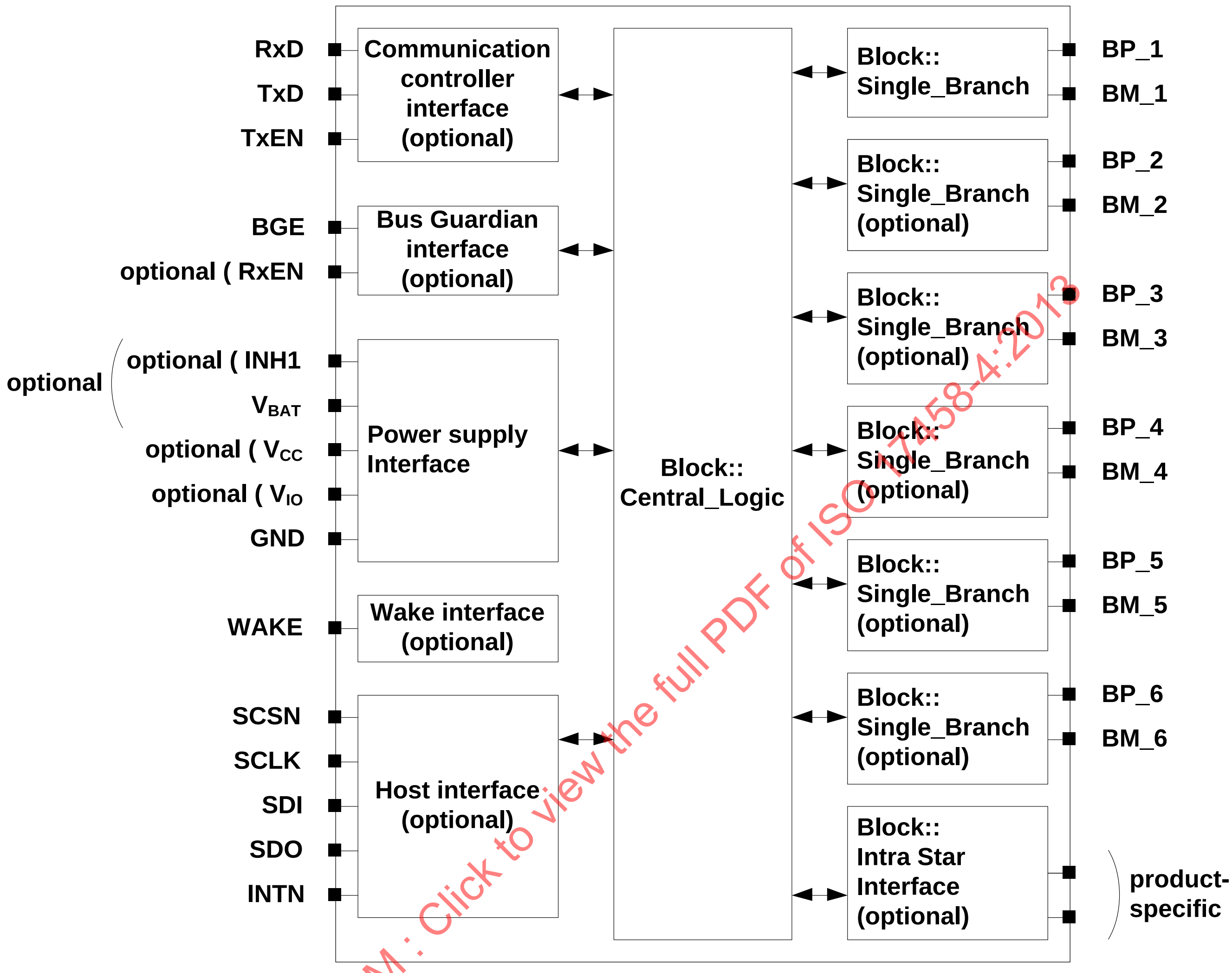
The number of branches may vary from two to an implementation specific maximum. See also Clause 9 for more information about active network layouts.

13.2 Hardware overview

13.2.1 Overview

The basic functionality and the operation modes of active star devices are given in this Clause, but also some restrictions for active stars (=active star device(s) plus peripherals like voltage regulators, etc) are given.

Figure 51 depicts the exemplary active star device with six branches.



Key

RxD	Receive Data	V_{IO}	Supply voltage digital I/O
TxD	Transmit Data	GND	Ground
BGE	Bus Gardian Enable	WAKE	Wakeup input
INH1	Inhibit 1 output	SCSN	Chip select input
V_{BAT}	Supply voltage (battery)	SCLK	SPO clock input
V_{CC}	Supply voltage (+5V)	SDI	SPI data input
SDO	SPI data output	INTN	Interrupt output
BP_x	Bus plus branch x	BM_x	Bus minus branch x

Figure 51 — Exemplary active star device with six branches

The block "Single_Branch" shall comprise a transmitter, a receiver and a bus-failure detector. Optionally, a wakeup detector for detection of wakeup events can be implemented to each of these blocks. A so-called "Central_Logic" block in the active star device coordinates the functions as described in the following subclauses. An active star device needs a power supply interface, which is described in 13.11. The optional voltage reference V_{IO} shall follow the 13.12.

This specification does not prescribe a certain realization. Figure 51 shows an exemplary hardware implementation, other forms are not prohibited. An active star can be realized with a fixed number of branches supported by a single device (so-called monolithic active star), but active stars may also be "non-monolithic" and built up by using separate active star devices each supporting one or more branches. In this case, the functionality of the block "Central_Logic" has to be distributed over the devices that are used, while the interface between the devices denoted as "Intra Star Interface" block in Figure 51, is product specific and therefore not part of this specification.

13.2.2 Communication paths

The active star can have four types of "communication paths":

— Single_Branches ("Branch")

— TxEN/TxD of the communication controller interface

— RxD of the communication controller interface

— Intra Star Interface

Each communication path signals its status to the Central_Logic.

Table 66 defines the communication path signals.

Table 66 — Communication path signals

Communication Path	Description
Activity	The receiver detects activity at the communication path (i.e. the communication channel is detecting activity and the activity detection of this communication path has expired).
NoActivity	The receiver detects idle at the communication path (i.e. there is *Idle* at the communication channel and the idle detection timeout has expired).
ReceiveActive	The communication path has entered a state at that the incoming data stream is forwarded to the other communication paths.
NotReceiveActive	The communication path has entered an idle state or a state at that the communication path is actively transmitting data.

A communication path shall signal either *Activity* or *NoActivity* and either *ReceiveActive* or *NotReceiveActive* to the Central_Logic.

The behaviour for the communication path "branch" is described in 13.6.

The behaviour of the communication path "TxEN/TxD" is described in 13.8.

The communication path "RxD" is not able to signal *Activity* or *ReceiveActive* to the Central_Logic.

The behaviour of the communication path "Intra Star Interface" is product specific.

13.3 Signal timing

13.3.1 Objective

This Clause describes the analog signal timing of the differential bus voltage *uBus* at TP11 of a branch that transmits a communication element in relation to the differential bus voltage *uBus* at TP14 of a branch that receives this communication element.

13.3.2 Signal timing – frames

A frame that passes an active star faces TSS length change and asymmetry, as well as prolongation of the last bit. Figure 52 defines a test pattern and an expected system response on an output load of 40 Ω || 100 pF.

Table 67 defines the active star frame timing characteristics.

Table 67 — Active star frame timing characteristics

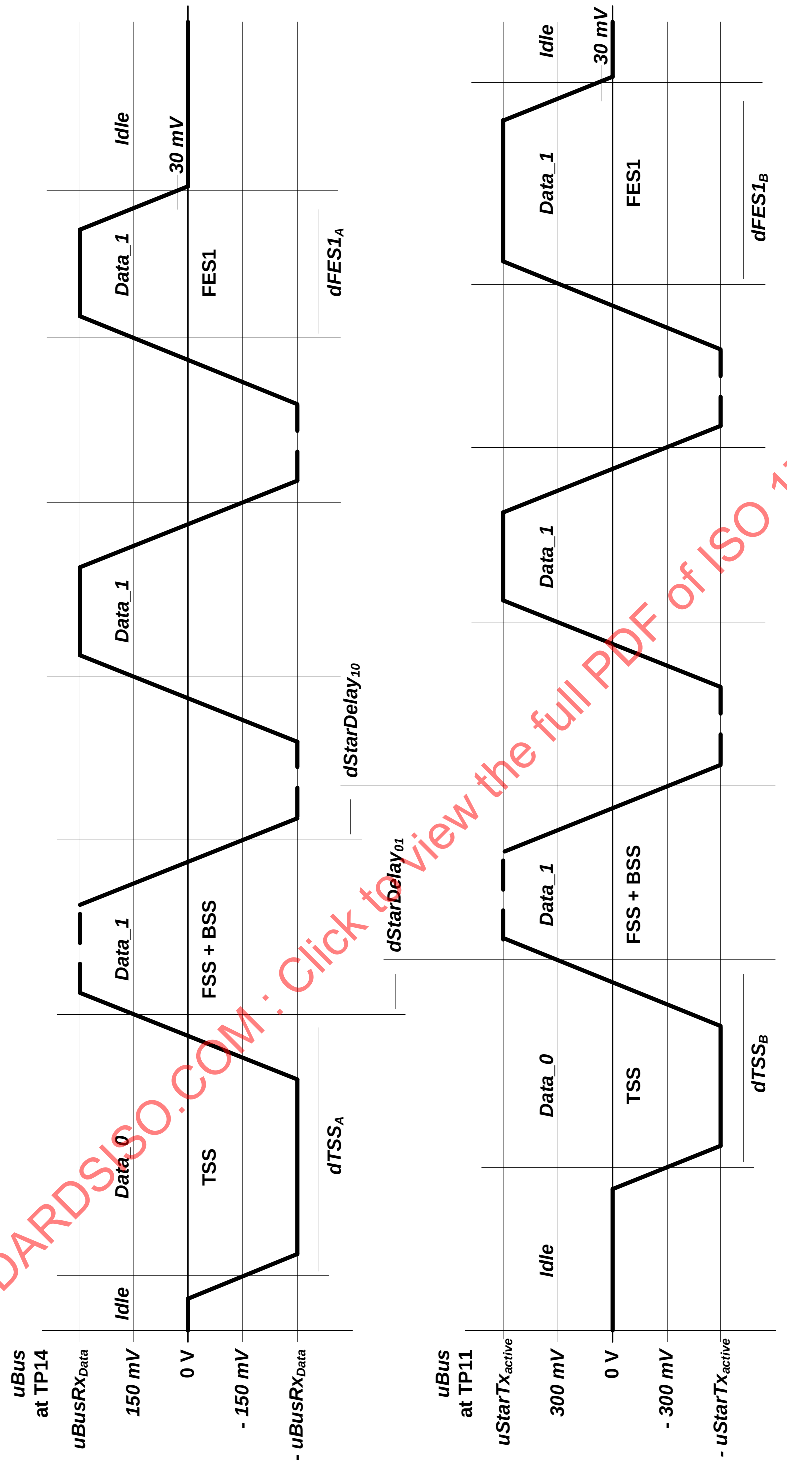
Name	Description	Min	Max	Unit
dStarDelay10	Propagation delay negative edge	—	150	ns
dStarDelay01	Propagation delay positive edge	—	150	ns
dStarAsym	Asymmetric propagation delay, monolithic active star [a]	0	8	ns
dStarAsym2	Asymmetric propagation delay, non-monolithic active star [a]	0	10	ns
dStarTSSLengthChange	Frame TSS length change caused by active star [b]	-450	0	ns
dStarFES1LengthChange	Prolongation of last bit of a frame [c]	0	450	ns

a *dStarAsym* = | $dStarDelay_{10}$ - $dStarDelay_{01}$ |, for *uBus* > 400 mV and 4 400 ns > *dBit* at TP14 > 80 ns.

b $dStarTSSLengthChange = dTSS_B - dTSS_A$

c $dStarFES1LengthChange = dFES1_B – dFES1_A$

Figure 52 shows the situation without ringing. In case ringing occurs see Annex A.



Key

TSS Transmission star sequence

BSS Byte start sequence

FSS Frame start sequence

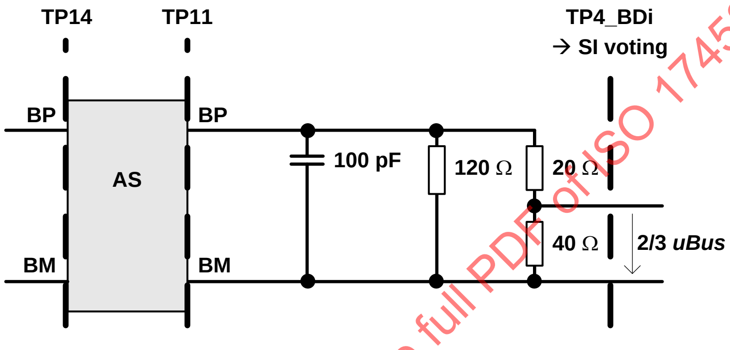
FES Frame end sequence

TP Test plane

Figure 52 — Signal timing of FlexRay frames

13.3.3 Signal timing – system view

Figure 53 depicts the system timing.



Key

AS Active start

BD Bus driver

BM Bus minus

TP Test plane

Figure 53 — System timing

Table 68 defines the system timing.

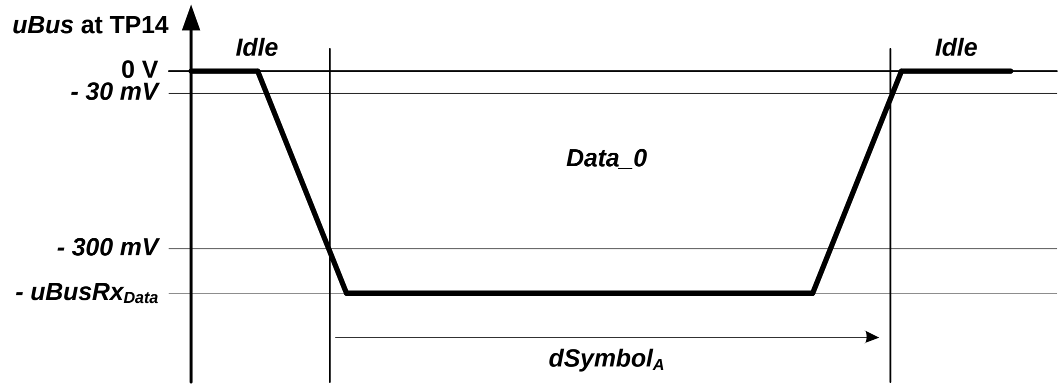
Table 68 — System timing

Description	Condition	Required
TP14 → TP4_BDi asymmetric delay	2/3 *uBus* voted by the SI-procedure [a] (point-to-point)	pass
[a] The SI-procedure is described in Annex A.		

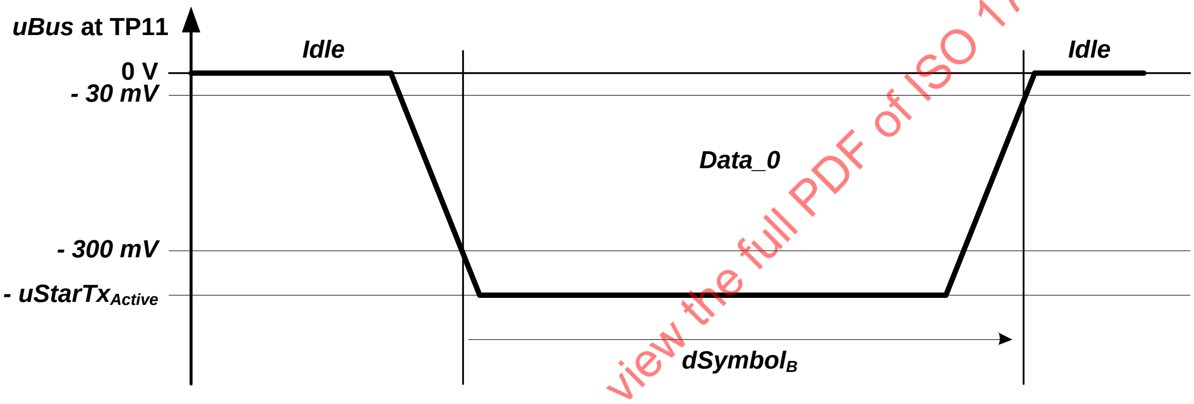
13.3.4 Signal timing – symbols

A symbol that passes an active star faces the effect of "symbol length change", e.g. the symbol length is lengthened or shortened like depicted in Figure 54 due to length change and asymmetric delay. The prolongation of the symbol at the end of a symbol (active→idle transition excluding propagation delay of active star) is depicted in Figure 55. For situation when ringing occurs see Annex A.

Figure 54 depicts the length change and asymmetric delay.



a) uBus at TP14



b) uBus at TP11

Key

TP Test plane

Figure 54 — Length change and asymmetric delay

Table 69 defines the active star symbol timing characteristics.

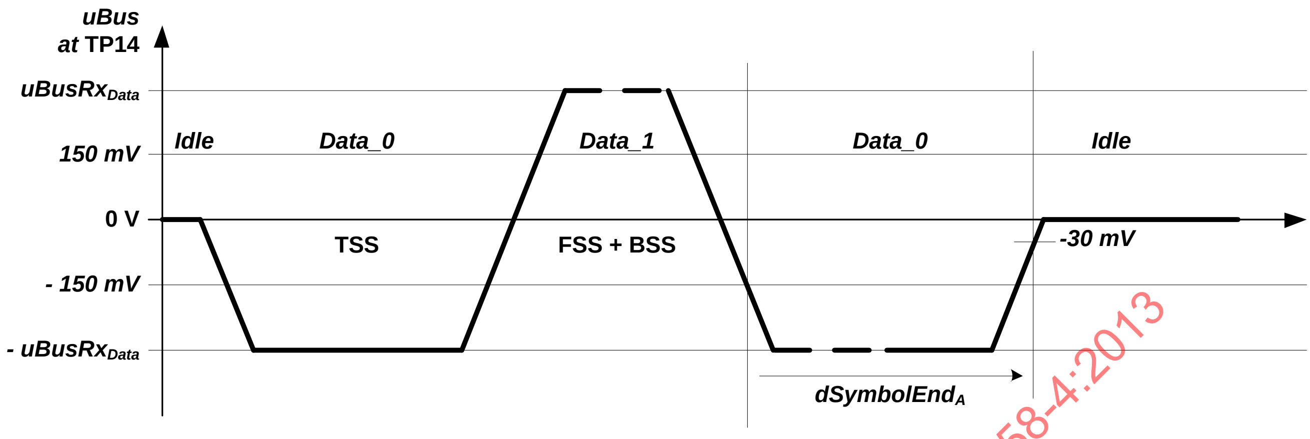
Table 69 — Active star symbol timing characteristics

Name	Description	Min	Max	Unit
dStarSymbolLengthChange	Symbol length change (only static portion) [a]	-300	450	ns
dStarSymbolEndLengthChange	Prolongation of symbol at symbol end [b]	0	450	ns

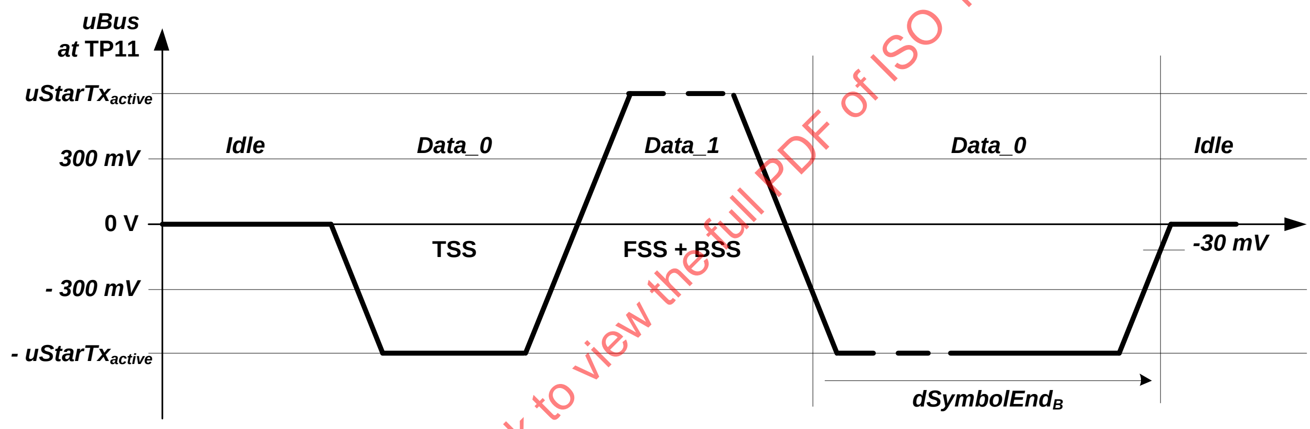
[a] *dStarSymbolLengthChange* = $dSymbol_B - dSymbol_A$

[b] *dStarSymbolEndLengthChange* = $dSymbolEnd_B - dSymbolEnd_A$

Figure 55 depicts the length change at symbol end.



a) uBus at TP14



b) uBus at TP11

Key

TSS Transmission star sequence

BSS Byte start sequence

FSS Frame start sequence

TP Test plane

Figure 55 — Length change at symbol end

13.3.5 Signal timing – collisions

When activity is detected on more than one communication path within the time interval of *dStarSetUpDelay*, it will happen that more than one communication path signals *ReceiveActive*. The other communication paths shall not give any preference to one of the incoming data stream and shall output *Data_0* [2)] when all of the communication paths signalling *ReceiveActive* receive *Data_0* [3)] or at least one receives *Data_0* [4)] and the

2) Respectively logic low at RxD

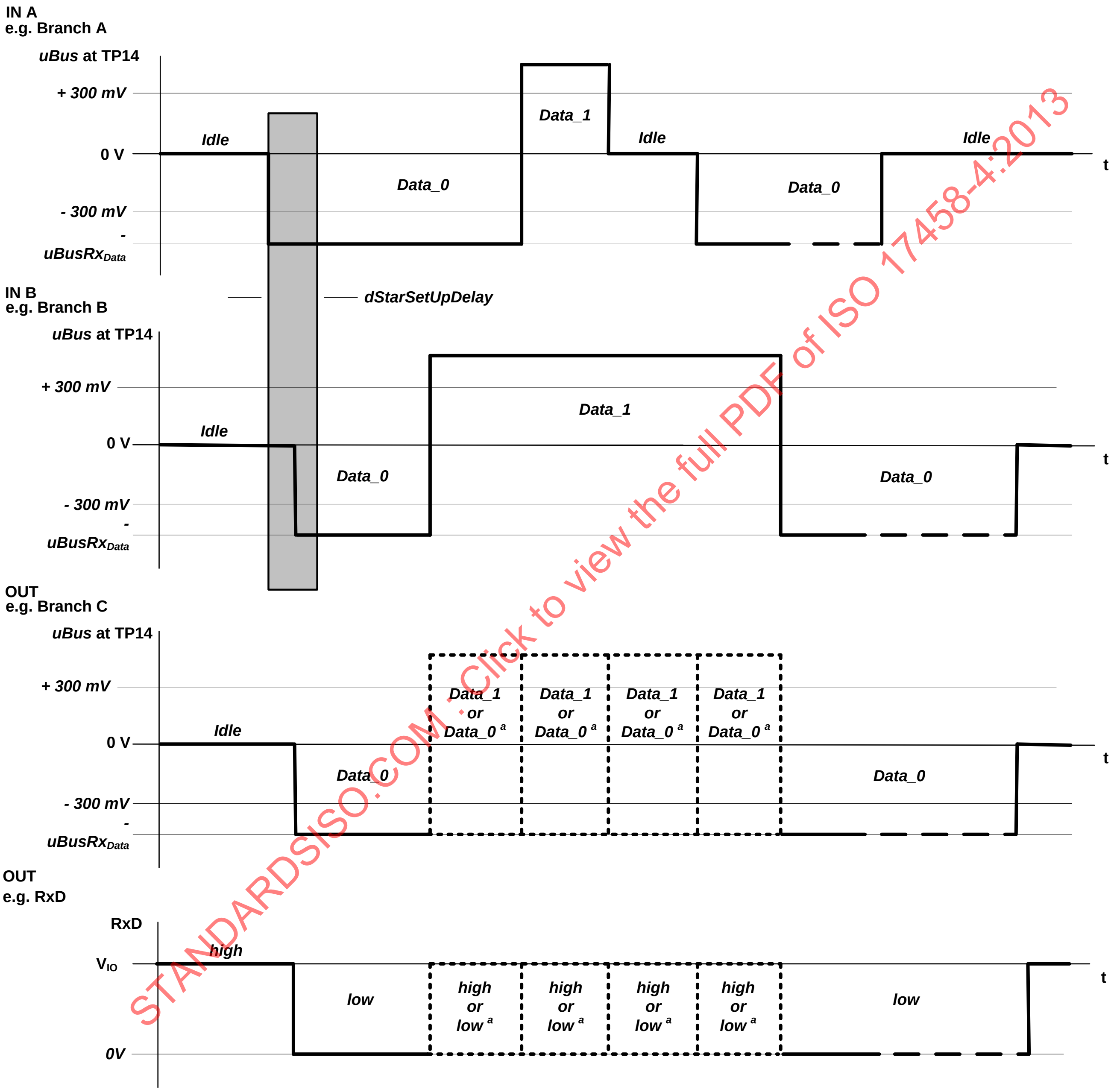
3) Respectively logic low at TxD

4) Respectively logic low at TxD

other *Idle* [5]. The output signals in case of other incoming signals are product specific (e.g. similar to the data collision on the bus, as described in 6.6).

The collision ends when all receiving communication paths are signalling *NotReceiveActive*.

Figure 56 depicts an exemplary situation where two branches A and B are detecting activity within *dStarSetUpDelay*.



a Product specific

5) Respectively logic high at TxEN

Key

TP Test plane

Figure 56 — Exemplary collision scenario on two branches within *dStarSetUpDelay*

In case the incoming data stream on communication path B starts after *dStarSetUpDelay* has expired, the incoming data stream is ignored. On all communication paths (except communication path A) the signal, which is received on communication path A, is transmitted. In case communication path B is a branch, the activity on this branch will be a superposition of the incoming (and ignored) activity and the data stream that is actively transmitted, see 6.6.

Table 70 defines the active star set-up delay.

Table 70 — Active star set-up delay

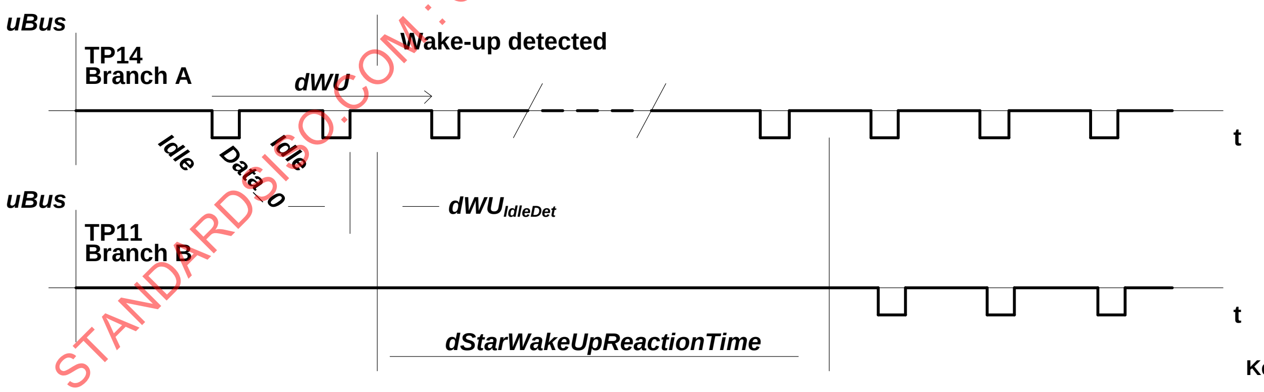
Name	Description	Min	Max	Unit
dStarSetUpDelay	Active star set-up delay	—	500	ns

13.3.6 Signal timing – wakeup patterns

The active star device shall be able to detect wakeup patterns as described in 6.8. Also frames that have the payload content according to 12.11 shall be considered as valid wakeup events.

The following behaviour is required (in case the wakeup detector is switched on):

Figure 57 depicts the wakeup behaviour.



Key

TP Test plane

NOTE 1 Mind that this figure is valid for monolithic and non-monolithic implementations.

NOTE 2 The input test signal on branch A shall constantly repeat 6 µs Data_0 phases followed by 18 µs Idle phases.

Figure 57 — Wakeup behaviour

An active star enters *AS_Normal* from *AS_Standby* or *AS_Sleep dStarWakeupReactionTime* after detecting a remote wakeup as shown in

Figure 57. When *AS_Normal* is entered, the active star shall be able to forward at least 2 (for networks with one active star) respectively at least 7 (for networks with two active stars) wakeup patterns as defined in 6.8. For further details see Annex A.

Table 71 — Active star wakeup reaction time

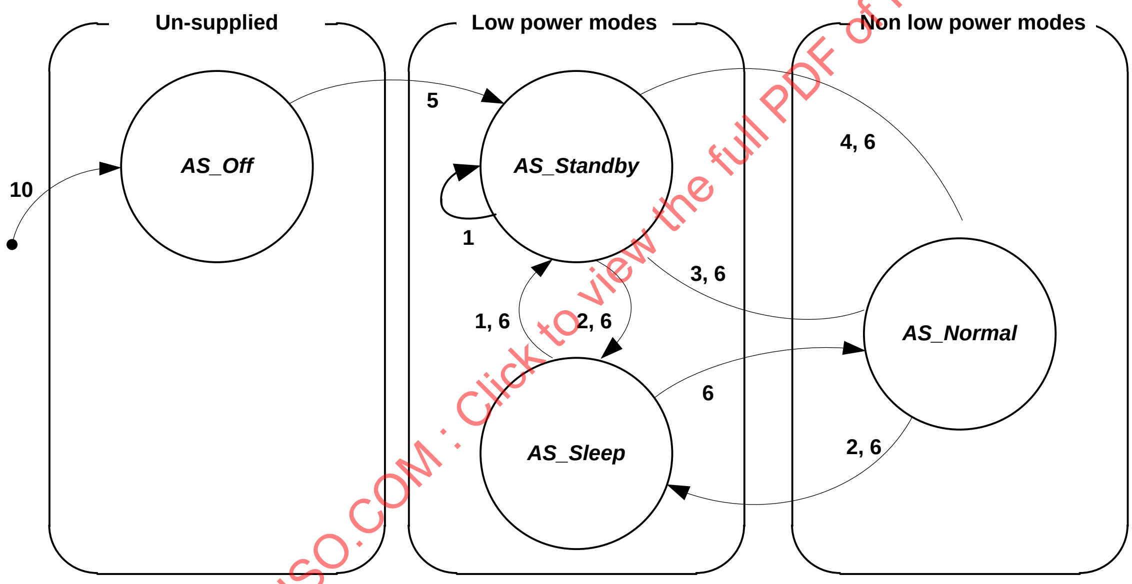
Name	Description	Min	Max	Unit
dStarWakeupReactionTime	Time to enter *AS_Normal* after wakeup [a]	—	70	µs

[a] Prerequisite: necessary supply voltages are available.

13.4 Active star device operation modes

13.4.1 Introduction

Figure 58 depicts the mandatory set of operation modes. Further product specific sub-modes and transitions may be implemented.



Key

1 .. 10 See Table 72.

Figure 58 — Active star operating states

Table 72 defines the operation mode transition table.

Table 72 — Operation mode transition table

Transition	Condition	Remark
1	Local wakeup or remote wakeup on one or more branches	AS sets APM flag
2	*dStarGoToSleep* expired [a] and APM flag set	—
3	Undervoltage on $uV_{StarSupply}$	AS sets APM flag
4	No undervoltage on $uV_{StarSupply}$ and APM flag is set	—
5	Power on, supply voltage of the digital part [b] above power-on threshold [c]	AS sets APM flag
6	Host command [d]	—
10	Power off, supply voltage of the digital part [b] drops below power on threshold; this transition can start from any other state. [c]	—

NOTE The "APM flag" is described in 13.5, *uVStarSupply* is described in 13.11.

[a] The timeout is started at zero, when *AS_Normal* or *AS_Standby* is entered; it is reset and halted while one or more communication paths are signalling *Activity*.

[b] Supply voltage of digital part can be derived from $uV_{StarSupply}$ and/or uV_{BAT} and/or uV_{CC}.

[c] The AS shall react on power-on/off within 100 µs.

[d] In case the APM flag is reset AND a AS-Host interface is present AND V_{DIG} is not in undervoltage AND the mode that shall be entered can be entered according to Table 89.

This event driven state machine shall ensure that a mode change has been performed latest 100 µs after the event occurred.

Table 73 defines the active star go-to-sleep timeout.

Table 73 — Active star go-to-sleep timeout

Name	Description	Min	Max	Unit
dStarGoToSleep	Go-to-Sleep timeout	640	6 400	ms

The minimum of this parameter was chosen to fulfil the following equation:

$$dStarGoToSleep \geq 40 \times cdCycleMax.$$

13.4.2 AS_Sleep

— The *AS_Sleep* mode is a so-called low power mode.

— The power consumption is significantly reduced compared to *AS_Normal*.

— The branches are forced to *Branch_LowPower*; see 13.6.

— *Sleep* is signalled on the INH1 output, in case this signal is implemented.

13.4.3 AS_Normal

— All branches are forced to leave *Branch_LowPower* mode, see 13.6.

— *Not_Sleep* is signalled on the INH1 output, in case this signal is implemented

13.4.4 AS_Standby

— The *AS_Standby* mode is a so-called low power mode.

— The power consumption is significantly reduced compared to *AS_Normal*.

— The branches are forced to *Branch_LowPower*; see 13.6.

— *Not_Sleep* is signalled on the INH1 output, in case this signal is implemented

13.4.5 AS_Off

— In case the supply voltage of the digital part falls below the product specific power on threshold the AS enters *AS_Off* mode.

— The branches are forced to *Branch_Off*; see 13.7.

— *Sleep* is signalled on the INH1 output, in case this signal is implemented.

13.5 Autonomous power moding flag (APM flag)

The APM decides whether the AS performs an autonomous power moding (APM flag set), or a host controlled power moding (APM flag reset).

Set conditions:

— Power on of the AS

— Detecting a local or remote wakeup

— Undervoltage on $V_{StarSupply}$

— An undervoltage on V_{IO}, if implemented

— A dedicated Host command, if an AS-host interface is implemented

Reset Condition:

A dedicated Host command, if an AS-host interface is implemented

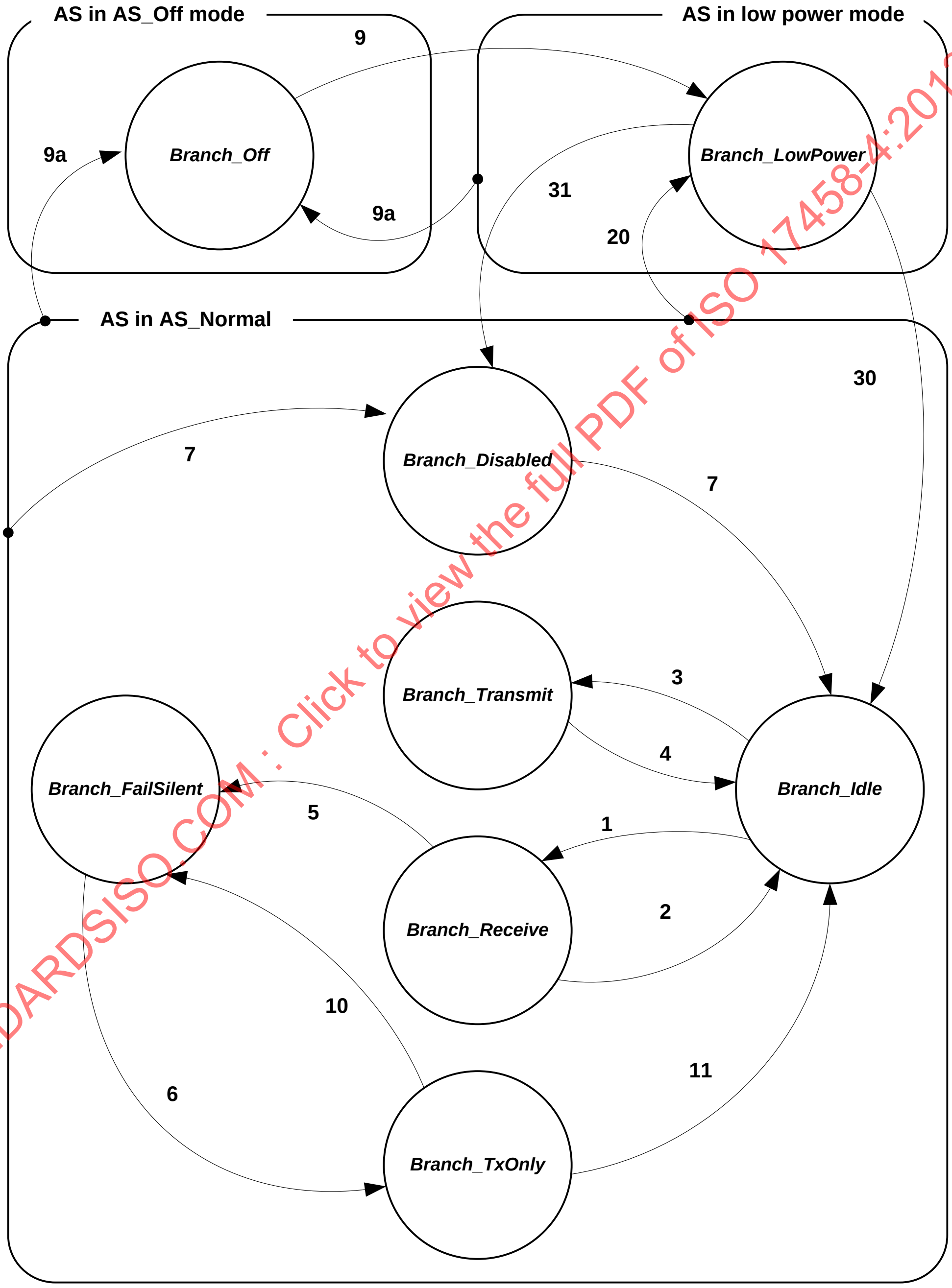
The AS never resets the APM.

13.6 Branch operating states

13.6.1 Introduction

Figure 59 depicts the mandatory set of branch operating states and the causes for transitions. Further product specific operation states and transitions are not prohibited.

Each branch of an active star device has its own states.



Key

1 .. 32 See Table 74.

Figure 59 — Operating states of a branch

Table 74 defines the operating state transition table.

Table 74 — Operating state transition table

Transition	Condition
1	Bus activity detected on this branch
2	*Idle* on this branch detected
3	At least one other communication path signals *ReceiveActive.*
4	No communication path signals *ReceiveActive* AND this branch is *Idle*
5	*dBranchRxActiveMax* expired
6	No communication path signals *ReceiveActive* AND this branch is *Idle* AND [APM flag is set OR host command [a] [b]]
7	Host command [a]
9	AS leaves *AS_Off*
9a	AS enters *AS_Off*
10	Bus error detected on this branch
11	No communication path signals *ReceiveActive* and this branch detects *Idle* (transmission ended without bus error)
20	Active star enters *AS_Sleep* OR *AS_Standby*
30	Active star device enters *AS_Normal*
31 [c]	Active star enters *AS_Normal* (branch previously disabled)

[a] If AS-host interface is implemented

[b] 'Host command' means to enable this transition. Immediate transition upon host command only when idle on all branches if AS host interface is implemented.

[c] Optional

13.6.2 Branch_Off

— The branch enters *Branch_Off* in case the AS enters *AS_Off*.

— Receive from and transmit to the bus is not possible in this state, the branch signals *Idle* on the bus.

13.6.3 Branch_LowPower

— Receive from and transmit to the bus is not possible in this state, the branch signals *Idle* on the bus.

— The wakeup detector is activated (default after power on), but may be switched on or off via host command, in case an AS – host interface is implemented.

— In case the branch detects a wakeup, it forces its AS device to *AS_Normal*.

— All branches are forced to *Branch_LowPower*, in case the AS leaves *AS_Normal*.

— The branch signals *NoActivity* and *NotReceiveActive* to the Central_Logic.

13.6.4 Branch_Idle

- Activity detection is active, the branch signals *Idle* on the bus.
- The branch signals *NotReceiveActive* and *NoActivity* to the Central_Logic.
- When the active star device enters *AS_Normal* the branch enters *Branch_Idle* (preconditioning the branch was previously not disabled)
- When activity is detected on this branch, this branch changes to *Branch_Receive*.
- The branch changes to *Branch_Transmit*, when at least one other communication path signals *ReceiveActive*.

13.6.5 Branch_Transmit

- The branch signals *NotReceiveActive* to the Central_Logic
- The binary data stream received by the communication path signalling *ReceiveActive* is transmitted (in case of no collision)
- In case of collision (see 13.3.5) the branch transmits *Data_0* when at least one of the communication paths signalling *ReceiveActive* receives a *Data_0* (collision).
- The branch signals *Activity* to the Central_Logic as long as activity is detected, otherwise *NoActivity*.
- When no communication path signals *ReceiveActive* and this branch detects *Idle* then *Branch_Idle* is entered.

13.6.6 Branch_Receive

- The branch signals *ReceiveActive* to the Central_Logic
- The branch signals *Activity* to the Central_Logic as long as activity is detected, otherwise *NoActivity*.
- When *Idle* is detected on the branch *Branch_Idle* is entered.
- After being in *Branch_Receive* for longer than *dBranchRxActiveMax* the branch is excluded from communication and enters *Branch_FailSilent*. (i.e. prevention of babbling idiots in absence of BGs.)

Table 75 defines the active star error detection timeouts.

Table 75 — Active star error detection timeouts

Name	Description	Min	Max	Unit
dBranchRxActiveMax	Noise detection time	650	2 600	µs

The maximum length of a communication element that can be sent is limited to the minimum value of *dBranchRxActiveMax*. For calculation of length of an encoded frame see ISO 17458-2.

13.6.7 Branch_Disabled

- To receive from and to transmit to the bus is not possible in this state, the branch signals *Idle* on the bus.
- The branch signals *NoActivity* and *NotReceiveActive* to the Central_Logic

13.6.8 Branch_FailSilent

— To receive from and transmit to the bus is not possible in this state, the branch signals *Idle* on the bus.

— The branch signals *NoActivity* and *NotReceiveActive* to the Central_Logic

— When no communication path signals *ReceiveActive* and enabled by either host or the APM flag, then *Branch_TxOnly* shall be entered.

13.6.9 Branch_TxOnly

— To receive from branch is not possible in this state.

— The branch signals *NotReceiveActive* and *NoActivity* to the Central_Logic.

— The binary data stream received by the communication path signalling *ReceiveActive* is transmitted (in case of no collision)

— In case of collision (see 13.3.5) the branch transmits *Data_0* when at least one of the communication paths signalling *ReceiveActive* receives a *Data_0* (collision).

— When a bus error is detected the branch changes to *Branch_FailSilent*.

— Bus error detection is a product specific feature; however, bus errors shall be detected at least, when it is not possible to send data on the branch.

— When no communication path signals *ReceiveActive* and this branch detects *Idle* then *Branch_Idle* is entered.

13.7 Branch transmitter and receiver circuit

13.7.1 Receiver characteristics

For receiver characteristics refer to 12.9.5.

The main difference is the minimum analog bit time, which is 80 ns, see Table 82.

13.7.2 Receiver behaviour (in non-low power modes)

For receiver behaviour in non-low power modes refer to 12.9.4 (*dStarIdleDetection* and *dStarActivityDetection* replaces *dBDIdleDetection* and *dBDActivityDetection*).

13.7.3 Receiver behaviour (in low power modes)

For receiver behaviour in low power modes refer to 12.9.8.

13.7.4 Receiver behaviour (in AS_Off mode)

For receiver behaviour in *AS_Off* mode refer to 12.9.9.

13.7.5 Active Star – bus interface simulation model parameters

For the purpose of simulation, the AS's product datasheet shall give the equivalent output impedance according to 12.9.11 ($R_{StarTransmitter}$ replaces $R_{BDTransmitter}$).

13.7.6 Transmitter characteristics

For active star devices without communication controller interface the transmitter shall fulfil the parameter *dBusTx10*, *dBusTx01*, *dBusTxai* and *dBusTxia* of 13.8.2 and 13.8.3.

13.8 Active star - communication controller interface (optional)

13.8.1 Overview

This interface itself shall functionally follow the description of the bus driver - communication controller interface as described in 12.4.

In idle (TxEN high) the communication controller interface signals *NotReceiveActive* and *NoActivity* to the Central_Logic. With TxEN on low *ReceiveActive* and *Activity* is signalled.

For TxEN a timeout *dStarTxActiveMax* (analogous to *dBDTxActiveMax*) needs to be implemented.

Table 76 defines the maximum length of transmitter activation.

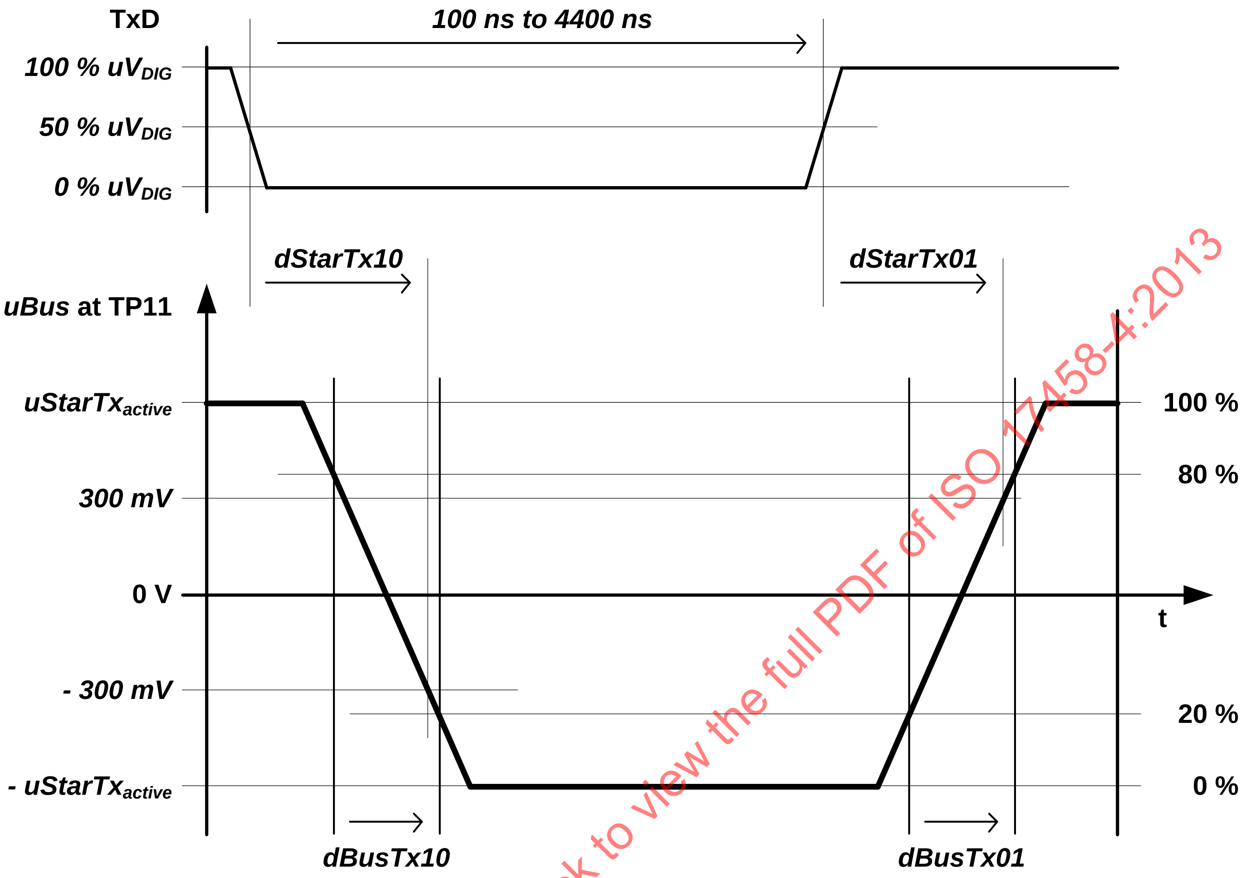
Table 76 — Maximum length of transmitter activation

Name	Description	Min	Max	Unit
dStarTxActiveMax	Maximum length of transmitter activation	650	2 600	µs

The maximum length of a communication element that can be sent is limited to the minimum value of *dStarTxActiveMax*. For calculation of length of an encoded frame see ISO 17458-2.

13.8.2 Transmitter timing characteristics

Figure 60 depicts the transmitter characteristics.



Key

V_{DIG}	Digital voltage
TP	Test plane
TxD	Transmit data
TP	Test plane

Figure 60 — Transmitter characteristics

Figure 60 is valid while TxEN is a logical low and BGE a logical high (if a BGE signal is available).

Table 77 summarizes the transmitter output characteristics.

Table 77 — Transmitter characteristics

Name	Description	Min	Max	Unit
$uStarTx_{active}$	Absolute value of *uBus*, while sending [a]	600	2 000	mV
$uStarTx_{idle}$	Absolute value of *uBus*, while Idle [a]	0	30	mV
dStarTx10	Transmitter delay, negative edge [b] [c]	—	225	ns
dStarTx01	Transmitter delay, positive edge [b] [c]	—	225	ns
dStarTxAsym	Transmitter delay mismatch [c] [d] | *dStarTx10* - *dStarTx01* |	—	10	ns
dBusTx10	Fall time differential bus voltage [b] (80 % → 20 %)	6	18,75	ns
dBusTx01	Rise time differential bus voltage [b] (20 % → 80 %)	6	18,75	ns
dBusTxDif	Difference between differential rise and fall time | *dBusTx10* - *dBusTx01* |	—	3	ns

NOTE Mind that the values given in this table are valid for monolithic and non-monolithic implementations.

a Load on BP/BM: [40..55] Ω || 100 pF.

b Load on BP/BM: 40 Ω || 100 pF.

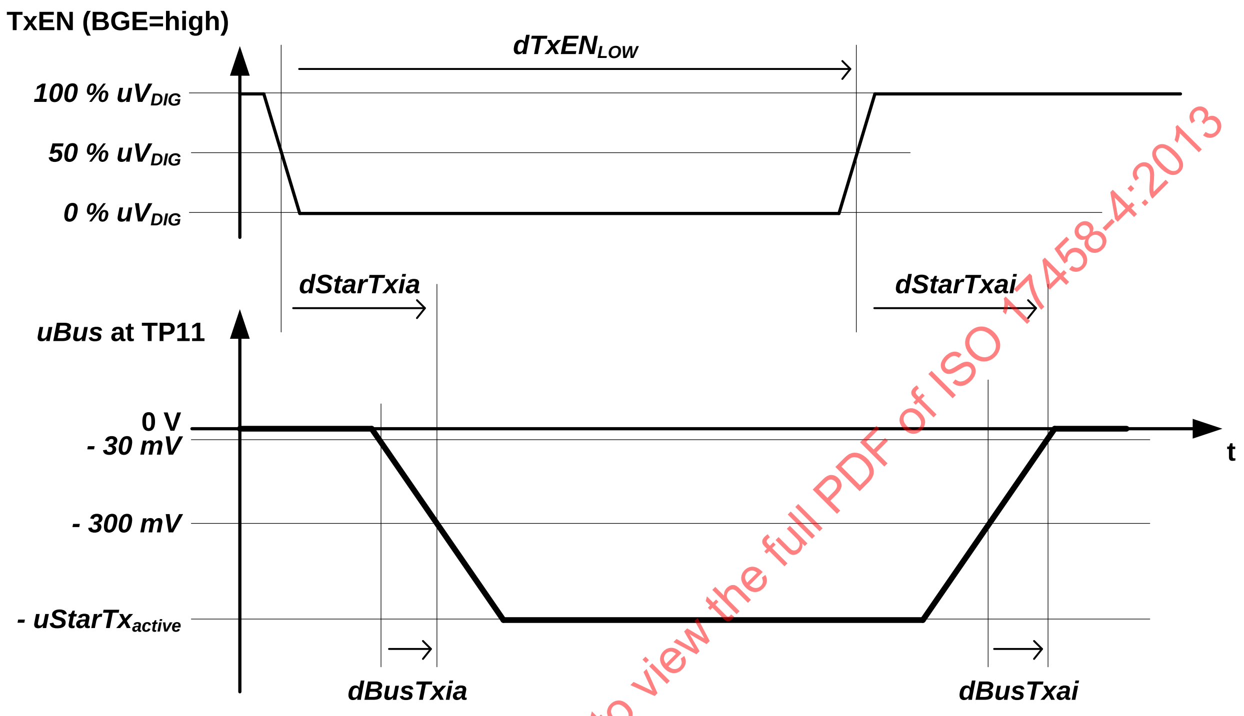
c All TxD signals with a sum of rise and fall time (20 % to 80 % uV_{DIG}) of up to 9 ns. See Figure 60 for further timing constraints.

d *dStarTxAsym* shall be guaranteed for ±300 mV as well as for ±150 mV level of *uBus*.

13.8.3 Transmitter behaviour at transition from idle to active and vice versa

Figure 61 shows the situation at start and end of a transmission with TxD permanent on logical low. The activation of the transmitter via TxEN shall not be possible as long as TxD is on logical high.

Activation of the transmitter via the TxEN signal shall only be possible, when no communication path signals *ReceiveActive*.



Key

BGE Bus guardian enable

TxEN Transmit enable not

TP Test plane

NOTE In case a BGE input is not present, BGE is assumed to be on logical high level.

Figure 61 — Transmitter characteristics at transition from idle to active and vice versa

Table 78 defines the transmitter characteristics.

Table 78 — Transmitter characteristics

Name	Description	Min	Max	Unit
dStarTxia	Transmitter delay idle -> active	—	550	ns
dStarTxai	Transmitter delay active -> idle	—	550	ns
dBusTxia	Transition time idle -> active	—	30	ns
dBusTxai	Transition time active -> idle	—	30	ns
dStarTSSLengthChange_TxD_Bus	TSS length change from TxD pin to signal on all branches [a]	-450	0	ns
dStarFES1LengthChange_TxD_Bus	FES1 length change from TxD pin to signal on all branches [b]	0	450	ns
dStarSymbolLengthChange_TxD_Bus	Symbol length change from TxD pin to signal on all branches [c]	-300	400	ns

NOTE 1 Mind that the values given in this table are valid for monolithic and non-monolithic implementations.

NOTE 2 Load on BP/BM: 40 Ω || 100 pF. Equal to TP1 load conditions, see 11.2.

a *dStarTSSLengthChange_TxD_Bus = dStarTx01 - dStarTxia*

b *dStarFES1LengthChange_TxD_Bus = dStarTxai – dStarTx01*

c *dStarSymbolLengthChange_TxD_Bus = dStarTxai - dStarTxia*

Table 79 defines the transmitter test signal constraint.

Table 79 — Transmitter test signal constraint

Name	Description	Min	Max	Unit
$dTxEN_{LOW}$	Time span of bus activity	550	650	ns

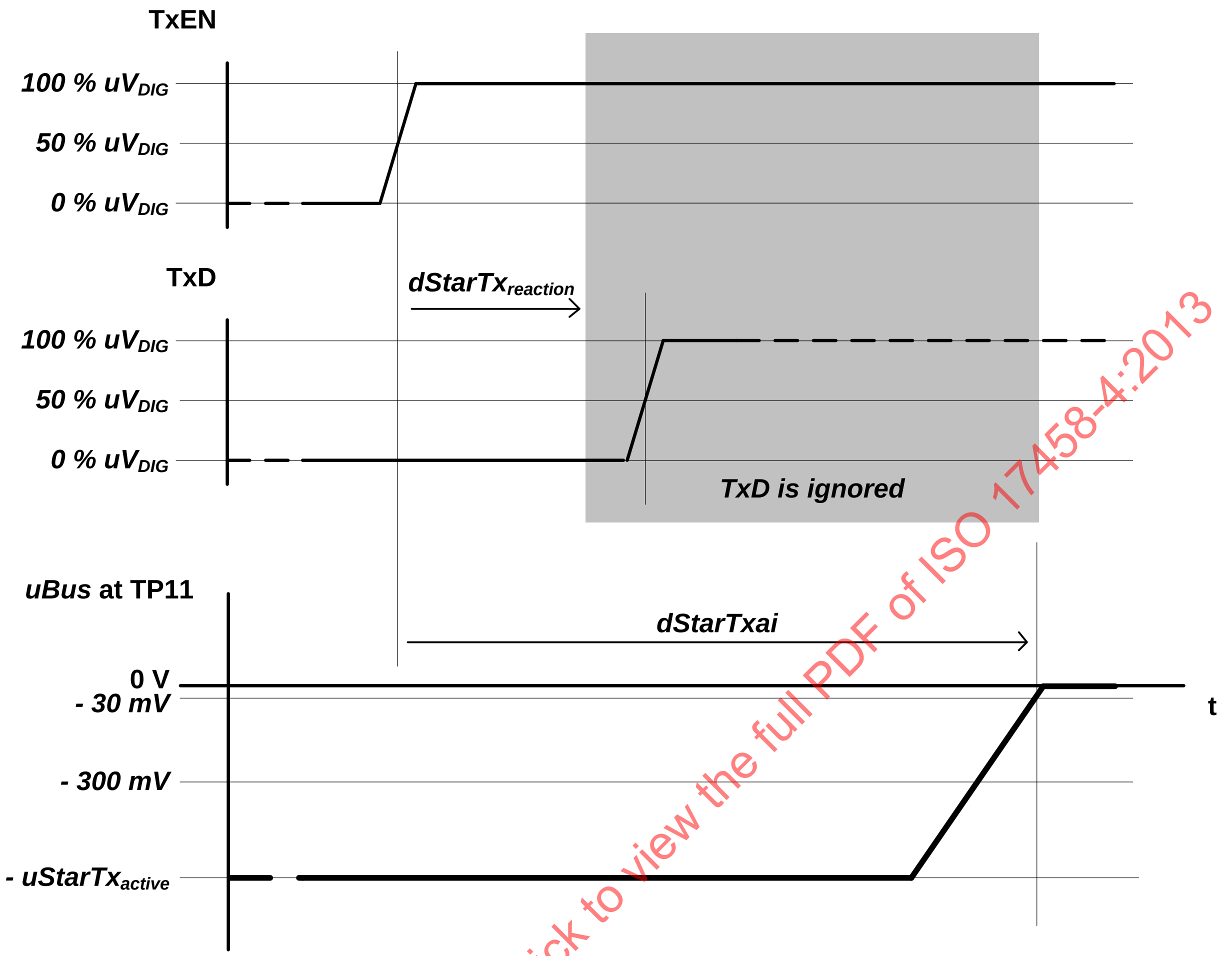
After a time span of $dStarTx_{reaction}$ after TxEN goes HIGH, the active star shall not react on changes at TxD.

Table 80 defines the TxD reaction timing.

Table 80 — TxD reaction timing

Name	Description	Min	Max	Unit
$dStarTx_{reaction}$	TxD reaction time after TxEN HIGH	—	75	ns

Figure 62 depicts the TxD reaction timing.



Key

TxD Transmit data

TxEN Transmit enable not

V_{DIG} Digital voltage

TP Test plane

Figure 62 — TxD reaction timing

13.8.4 Receiver behaviour at transition from idle to active and vice versa

In case a communication path signals *ReceiveActive*, the communication path "RxD" is activated and the binary data stream received by the communication path signalling *ReceiveActive* is transmitted (in case of no collision) at RxD.

In case of collision (see 13.3.5) RxD transmits *Data_0* when at least one of the communication paths signalling *ReceiveActive* receives a *Data_0*.

Table 81 defines the receiver characteristics.

Table 81 — Receiver characteristics

Name	Description	Min	Max	Unit
dStarRxai	Active Star idle reaction time	50	550	ns
dStarRxia	Active Star activity reaction time	100	550	ns
dStarTSSLengthChange_Bus_RxD	TSS length change from branch to RxD pin [a]	-450	0	ns
dStarFES1LengthChange_Bus_RxD	FES1 length change from branch to RxD pin [b]	0	450	ns
dStarSymbolLengthChange_Bus_RxD	Symbol length change from branch to RxD pin [c]	-300	400	ns

NOTE 1 Mind that the values given in this table are valid for the AS-CC interface of monolithic and non-monolithic implementations.

NOTE 2 Timings of length changes and truncation "branch-to-branch" are given in 13.3.

[a] *dStarTSSLengthChange_Bus_RxD = dStarRx01 - dStarRxia*

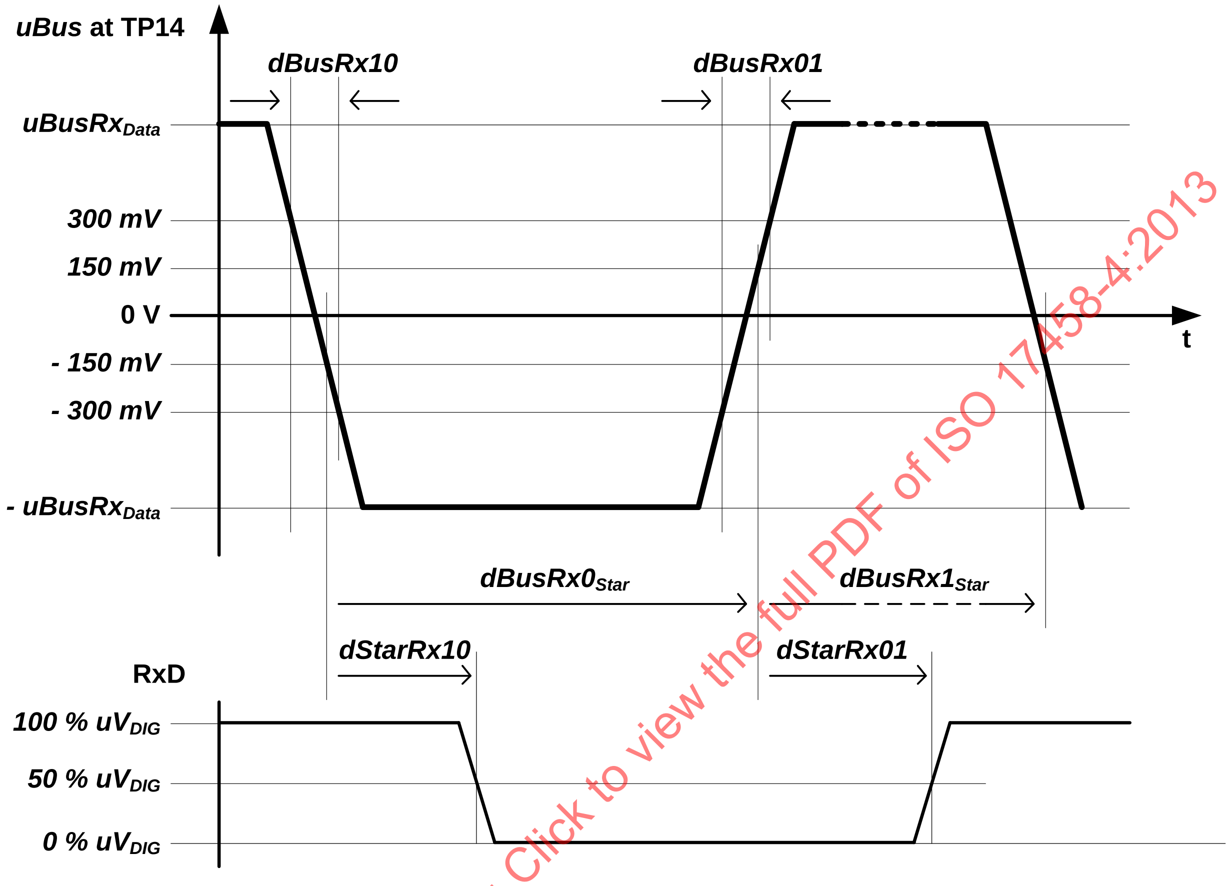
[b] *dStarFES1LengthChange_Bus_RxD = dStarRxai – dStarRx01*

[c] *dStarSymbolLengthChange_Bus_RxD = dStarRxai - dStarRxia*

For illustration see Figure 45 in 12.9.7, where the parameters of the bus driver (*dBDRxia* / *dBDRxai*) need to be replaced by the parameters of the active star (*dStarRxia / dStarRxai*).

13.8.5 Receiver timing characteristics

The receiver delay is defined as the time span for transferring the data stream (analog information) from the signal path (bus) to the binary data stream (digital RxD signal) as depicted in Figure 63. The receiver input signal for measuring the characteristics is also depicted in Figure 63.



Key

RxD Receive data

TP Test plane

Figure 63 — Receiver timing characteristics

Table 82 defines the receiver input signal for data recognition.

Table 82 — Receiver input signal for data recognition

Name	Description	Min	Max	Unit
$uBusRx_{Data}$	*uBus* at TP14	400	3 000	mV
dBusRx10	Transition time *Data_1* ⇒ *Data_0*	—	22,5	ns
dBusRx01	Transition time *Data_0* ⇒ *Data_1*	—	22,5	ns
$dBusRx0_{Star}$	Time span *Data_0* [a]	80	4 320	ns
$dBusRx1_{Star}$	Time span *Data_1* [a]	80	4 320	ns

[a] 200 ns (± 1 ns) ≤ $dBusRx1_{Star}$ + $dBusRx0_{Star}$ ≤ 4 400 ns (± 1 ns).

The behaviour of the receiver when a test signal according to Figure 63 and Table 82 is applied shall be as given in Table 83.

Table 83 defines the receiver data timing requirements.

Table 83 — Receiver data timing requirements

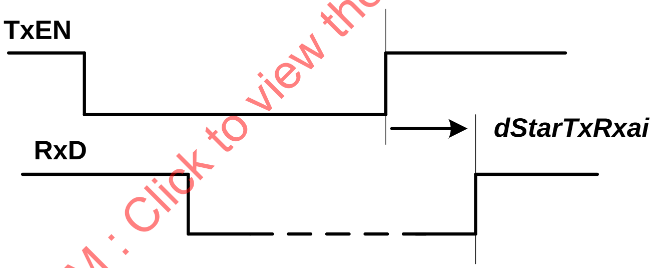
Name	Description	Min	Max	Unit
dStarRx10	Receiver delay, negative edge	—	225	ns
dStarRx01	Receiver delay, positive edge	—	225	ns
dStarRxAsym	Receiver delay mismatch [a] | *dStarRx10* – *dStarRx01* |	—	10	ns

[a] *dStarRxAsym* shall be guaranteed for ±300 mV as well as for ±150 mV level of *uBus*

13.8.6 TxEN – RxD loopback

The time until RxD indicates idle after the end of a transmission needs to be limited in order to ensure that the wakeup protocol mechanism works properly.

Figure 64 depicts the idle-loop delay timing.



Key

RxD Receive data

TxEN Transmit enable not

Figure 64 — Idle-loop delay timing

Table 84 defines the idle-loop delay timing.

Table 84 — Idle-loop delay timing

Name	Description	Min	Max	Unit
dStarTxRxai	Idle-Loop delay [a]	—	325	ns

[a] *dStarTxRxai* is sum of *dStarTxai* Table 77) and *dStarRxai* (Table 80) for TxEN and RxD of a single device under the constraint both values cannot be at their maximum (as these are defined for the non-monolithic implementations).

13.8.7 Electrical behaviour

13.8.7.1 RxD

The RxD signal of an AS shall meet the following definition.

Table 85 defines the RxD signal rise and fall times.

Table 85 — RxD signal rise and fall times

Name	Description	Min	Max	Unit
$dStarRxD_{R15} + dStarRxD_{F15}$	Sum of rise and fall time at 15 pF load [a]	—	13	ns
$\vert dStarRxD_{R15} - dStarRxD_{F15} \vert$	Difference of rise and fall time at 15 pF load	—	5	ns
NOTE The requirements on AS's RxD are intentionally different from the BD's RxD, since more interface asymmetry is allowable.				
[a] 20 % to 80 % uV_{DIG}. A datasheet for the AS shall state maximum rise and fall time on RxD separately.				

RxD shall be on logical HIGH level, when the AS is in low power modes. Thus detection of wakeup shall not be signalled on RxD, which is not necessary since the AS enters *AS_Normal* autonomously after wakeup.

Table 86 defines the resulting RxD signal from AS to CC.

Table 86 — Resulting RxD signal from AS to CC

AS operation mode	Signal on bus wires	RxD [a]
AS_Normal	*Idle*	high
	Data_0	low
	Data_1	high
(All other)	X	high
[a] The output voltages for logical high and low states are defined in Clause 15.		

13.8.7.2 TxD

The TxD input of an AS shall meet the definition of Table 87.

Table 87 — TxD input characteristics

Name	Description	Min	Max	Unit
C_StarTxD	Input capacitance on TxD pin	—	10	pF
uStarLogic_1	Threshold for detecting logical high [a]	—	60	%
uStarLogic_0	Threshold for detecting logical low [a]	40	—	%
[a] Relative to uV_{DIG}, (see 15.3) a hysteresis is not required.				

13.9 Active star – bus guardian interface (optional)

The interface comprises two digital electrical signals: The BGE (Bus Guardian Enable), which is mandatory for this interface, is one input to the AS allowing a BG or a similar supervision unit to disable the transmitter and the RxEN (Receive Enable Not), which is optional, one output of the AS.

The behaviour is equal to the Bus Driver – bus guardian interface described in 12.5.

13.10 Active star – host interface (optional)

This option belongs to the functional class "Active Star – host interface".

The active star device may comprise a host interface in form of an SPI, as described in detail in 15.8, where an interrupt (INTN) signal is also mandatory.

Set conditions: The INTN signal shall be switched to logical low when errors occur and also when they recover. In case of reception of wakeup events the INTN shall also be switched to logical low. Product specific more events can be signalled.

Reset conditions: The INTN shall only be reset with a correct access to the corresponding error or interrupt register.

The AS shall perform the mode change within a time span of $dStarModeChange_{SPI}$ after the rising edge on SCSN, if not prevented by an undervoltage condition.

Table 88 defines the mode transition time.

Table 88 — Mode transition time

Name	Description	Min	Max	Unit
$dStarModeChange_{SPI}$	Mode transition time after host command	—	100	µs
$dStarReactionTime_{SPI}$	Time from detection of an event to falling edge of INTN	—	200	µs

In case the functional class "Active Star internal voltage regulator" is implemented (only V_{BAT}, no V_{CC} supply) and the device is not in *AS_Off* mode and V_{IO} is not in undervoltage, then the SPI shall be accessible in any operation mode.

In case the functional class "Active Star internal voltage regulator" is not implemented and V_{CC} is neither in undervoltage nor unsupplied and V_{IO} (if implemented) is not in undervoltage, then the SPI shall be accessible in any operation mode.

13.11 Active star – power supply interface

13.11.1 Introduction

The interface between the active star and the power supply comprises of at least two pins, which are the ground connection (GND) and one or two primary supply pin(s) (V_{CC} and/or V_{BAT}). Additionally the active star should have an alternative supply delivering $uV_{StarSupply}$, such as a capacitor (charged out of a primary supply) or an internal voltage regulator, to be able to start forwarding wakeup patterns almost immediately. $uV_{StarSupply}$'s required dependency of uV_{BAT} and uV_{CC} is given Table 89. In case the status of uV_{BAT} and/or uV_{CC} changes, $uV_{StarSupply}$'s status shall change according to Table 89 within a product specific delay. The datasheet of the AS shall state the delay or shall give a hint how to calculate this delay.

Furthermore this interface may comprise of an optional inhibit output (INH1), when a V_{BAT} input is implemented.

A power supply input V_{CC} may be implemented, which shall be connected to a low voltage supply with nominal 5 V. The minimum and maximum allowable voltages on V_{CC} are product specific.

A power supply input V_{BAT} may be implemented, which can be directly connected to the vehicle battery (e.g. nominal 42 V) in order to supply the AS, when a V_{CC} input is not available or not implemented. The minimum and maximum allowable voltages on V_{BAT} are product specific.

Table 89 defines the summary of supply voltage conditions.

Table 89 — Summary of supply voltage conditions

uV_{BAT} [a]	uV_{CC}	$uV_{StarSupply}$	AS can enter	WU detection ...
Normal operating range	Not implemented	Normal operating range	All operation modes	Mandatory
Undervoltage or unsupplied	Not implemented	Undervoltage or unsupplied	Low power modes [b] or *AS_Off* [c]	Not mandatory
Not implemented	Normal operating range	Normal operating range	All operation modes	Mandatory
Not implemented	Undervoltage or unsupplied	Undervoltage or unsupplied	Low power modes [b] or *AS_Off* [c]	Not mandatory
Normal operating range	Normal operating range	Normal operating range	All operation modes	Mandatory
Undervoltage or unsupplied	Normal operating range	Normal operating range	All operation modes	Not Mandatory
Normal operating range	Undervoltage or unsupplied	Normal operating range, when all branches in *Idle*. [d]	All operation modes	Mandatory, when $uV_{BAT} \geq 7$ V Not mandatory, when $uV_{BAT} < 7$ V
Undervoltage	Undervoltage	Undervoltage	Low power modes	Not mandatory
Unsupplied or not implemented	Unsupplied or not implemented	Unsupplied	*AS_Off*	Not possible

NOTE Find more information on low voltage conditions in Annex A.

a Mind that uV_{BAT} is the voltage on the AS's pin and uV_{ECU} the voltage applied from the vehicle battery to the ECU connector.

b If $uV_{StarSupply}$ in undervoltage.

c If supply voltage of the digital part is below power on threshold.

d $uV_{StarSupply}$ may enter undervoltage conditions after forwarding wakeup symbols.

Moreover, there are dependencies to the functional classes "AS voltage regulator control" and "AS internal voltage regulator", see 13.15.3 and 13.15.4.

13.11.2 Inhibit output (optional)

This option belongs to the functional classes "Active Star - voltage regulator control" and "Active Star – internal voltage regulator".

Optionally, the active star - power supply interface may have an inhibit output signal (INH1) that is meant to control an external voltage regulator. The active star signals *Sleep* to the power supply, when leaving the INH1 pin floating and signals *Not_Sleep*, when driving the INH1 pin to battery voltage level.

Table 90 defines the inhibit pin characteristics.

Table 90 — Inhibit pin characteristics

Name	Description	Min	Max	Unit
$uINH1_{Not\_Sleep}$	Voltage on inhibit pin, when signaling *Not_Sleep* at 200 µA load, $uV_{BAT} \geq 5{,}5$ V	$uV_{BAT} - 1$ V	—	V
$iINH1_{Leak}$	Absolute leakage current while signaling *Sleep* [a]	—	10	µA

[a] Leakage current can be tested by applying a 100 kΩ to INH and checking for | *uINH1* | < 1 V.

13.11.3 V_{CC} supply voltage monitoring (optional)

The AS shall provide a means to monitor the V_{CC} supply voltage, if a V_{CC} input is implemented. The AS shall detect an error when the V_{CC} supply voltage falls below a product specific threshold, which shall be above 4 V and an interrupt shall be signalled on the AS - host interface if implemented.

Table 91 defines the V_{CC} undervoltage detection.

Table 91 — V_{CC} undervoltage detection

Name	Description	Min	Max	Unit
$dStarUVV_{CC}$	V_{CC} Undervoltage detection time	—	1 000	ms
$dStarRV_{CC}$	V_{CC} Undervoltage recovery time	—	10	ms
$uStarUVV_{CC}$	V_{CC} Undervoltage detection threshold [a]	4	—	V

[a] A hysteresis between detection and recovery threshold can be implemented.

13.11.4 V_{BAT} supply voltage monitoring

In case the AS has a V_{BAT} pin the voltage on this pin shall be monitored. The AS shall detect an error when the V_{BAT} supply voltage falls below a product specific threshold, which shall be above 4 V and an interrupt shall be signalled on the AS - host interface if implemented.

Table 92 defines the V_{BAT} undervoltage detection.

Table 92 — V_{BAT} undervoltage detection

Name	Description	Min	Max	Unit
$dStarUVV_{BAT}$	V_{BAT} Undervoltage detection time	—	1 000	ms
$dStarRV_{BAT}$	V_{BAT} Undervoltage recovery time	—	10	ms
$uStarUVV_{BAT}$	V_{BAT} Undervoltage detection threshold [a]	4	5,5	V

[a] A hysteresis between detection and recovery threshold can be implemented.

13.11.5 Supply voltage monitoring

If the AS does not have sufficient supply to operate conform to this specification this shall be detected within $dStarUVV_{Supply}$. The reaction on an undervoltage condition is defined in 13.4.

Table 93 defines the supply voltage undervoltage detection.

Table 93 — Supply voltage undervoltage detection

Name	Description	Min	Max	Unit
dStarUVV$_{Supply}$	Supply undervoltage detection time	—	1	ms
dStarRV$_{Supply}$	Supply undervoltage recovery time	—	10	ms
uStarUVV$_{Supply}$	Supply undervoltage detection threshold [a]	4	—	V

[a] A hysteresis between detection and recovery threshold can be implemented.

13.12 Active star – level shift interface (optional)

13.12.1 Overview

NOTE This option belongs to the functional class "Active Star - logic level adaptation"

Optionally, a level shift input V_{IO} can be implemented in order to apply a reference voltage uV_{DIG} for all digital inputs and all digital outputs. In case such reference voltage is available, then $uV_{DIG} = uV_{IO}$, otherwise $uV_{DIG} = uV_{CC}$. For more information, see Clause 15.

13.12.2 V_{IO} voltage monitoring

In case there is a V_{IO} voltage input implemented as reference for digital IO, the AS shall provide a means to monitor the V_{IO} voltage. The AS shall not autonomously switch to a low power mode when the V_{IO} voltage falls below a product specific threshold, which needs to be higher than 2 V and an error shall be signalled to the host. Wakeup detection and forwarding of communication elements shall be performed even when V_{IO} is in under-voltage condition. This shall be done according to the latest branch configuration information sent by the host, in case an AS host interface is implemented.

Table 94 defines the V_{IO} undervoltage detection.

Table 94 — V_{IO} undervoltage detection

Name	Description	Min	Max	Unit
dStarUVV$_{IO}$	V_{IO} Undervoltage detection time	—	1 000	ms
dStarRV$_{IO}$	V_{IO} Undervoltage recovery time	—	10	ms
uStarUVV$_{IO}$	V_{IO} Undervoltage detection threshold [a]	2	—	V

[a] A hysteresis between detection and recovery threshold can be implemented.

Undervoltage on V_{IO} sets the APM flag, see 13.4.

In case an AS – CC interface is present the TxEN signal shall be considered as on logical HIGH, while V_{IO} undervoltage persists.

13.13 Active star – bus interface

The active star - bus interface comprises as many blocks named "Single_Branch" as branches are supported by the active star device. Each block "Single_Branch" is an independent branch as described in 12.6 and the following subclauses.

13.14 Active star – wake interface (optional)

NOTE This option belongs to the functional classes "Active Star - voltage regulator control" and "Active Star – internal voltage regulator".

The active star – wake interface comprises a WAKE input. The requirements to this interface are the same as described in 12.10 (*dStarWakePulseFilter* and $dStarWakeupReaction_{local}$ replaces *dBDWakePulseFilter* and $dBDWakeupReaction_{local}$). The WAKE input is battery voltage related input.

13.15 Active star functional classes

13.15.1 Functional class: "Active star - communication controller interface"

Optionally, an active star - communication controller interface can be implemented. Its operation is similar to the operation of the bus driver - communication controller interface block as specified in 12.4. With respect to this interface an active star in *AS_Normal* shall behave like a BD in *BD_Normal*, except for the BD parameters *dBDTxia* and *dBDTxai*, which are overruled by the parameters *dStarTxia* and *dStarTxai*, see 13.8.3.

13.15.2 Functional class: "Active star - bus guardian interface"

This functional class can only be implemented in case an active star - communication controller interface is implemented. It comprises the implementation of an active star - bus guardian interface according to 13.9.

13.15.3 Functional class "Active star - voltage regulator control"

This functional class requires the following options to be implemented:

— "V_{BAT}" power supply input, see 13.11

— "V_{CC}" power supply input; see 13.11

— "INH1" output signal, see 13.11.1

Optionally, an Active Star – wake interface according to 13.14 may be implemented in this functional class.

13.15.4 Functional class "Active star – internal voltage regulator"

This functional class requires the following options to be implemented:

— "V_{BAT}" power supply input; see 13.11.

Optionally, an "INH1" output signal according to 13.11.1 may be implemented in this functional class.

Optionally, an Active Star – wake interface according to 13.14 may be implemented in this functional class.

This functional class requires that no "V_{CC}" supply input is present.

13.15.5 Functional class "Active star – logic level adaptation"

This class requires the implementation of a logic level-shift interface as described in 13.11 and requires that the thresholds of all digital inputs are controlled by this voltage as well as all digital outputs are related to this level. See also 15.2 and 15.3.

13.15.6 Functional class "Active star – host interface"

This class requires the implementation of an interface according to 13.10.

13.15.7 Functional class "Active star increased voltage amplitude transmitter"

This class does not require additional functions to be implemented. However, the minimum of $uStarTx_{Active}$ shall be 900 mV and thus different from the minimum value state in Table 77. The mask test as defined in 11.2.5 needs to be fulfilled.

13.16 Active star behaviour under fault conditions

13.16.1 Environmental faults

Table 95 defines the active star behaviour under fault conditions.

Table 95 — Active star behaviour under fault conditions

Fault description	Behaviour at BP and BM	Behaviour at AS's digital interfaces [a]
AS is without any kind of supply voltage (AS in *AS_Off*)	high impedance, see Table 50	See 15.2.
Undervoltage on $uV_{StarSupply}$	AS shall not force a differential voltage on BP/BM. [b]	—
Undervoltage on uV_{CC}	—	AS shall signal error to the host [c]
Undervoltage on V_{BAT} , but $uV_{StarSupply}$ not in undervoltage	The AS shall continue to forward communication elements from one branch to other branches	AS shall signal error to the host [c]
AS looses connection to channel (BP and BM interrupted)	AS shall detect the channel to be idle, while its TxEN (if implemented) is on logical high and all other branches are not in *Branch_Receive*	RxD behaviour according to 12.4, if CC-interface (see 13.8) is implemented.
BP line shorted to ground	AS shall internally limit the output current. Limits given in Table 57 are valid	AS shall signal error to the host in case communication is not possible. For bus error detection see 12.12.5.
BP line shorted to V_{BAT} or V_{CC}		
BM line shorted to ground		
BM line shorted to V_{BAT} or V_{CC}		
BP line shorted to BM line		
INTN (if implemented) signaling line becomes interrupted	—	No detection by AS. If INTN does not react on changes as expected, the host can assume that the line is clamped. For INTN behaviour see 13.10.
INTN (if implemented) signaling line is shorted to ground	—	
INTN (if implemented) signaling line is shorted to V_{IO} or V_{CC}	—	
TxD (if implemented) line becomes interrupted	AS outputs *Data_0*, when enabled via TxEN (and BGE, if applicable)	—
TxEN (if implemented) line becomes interrupted	AS shall sense the input as high, see 13.16.2.	—
TxEN (if implemented) signal is permanently asserted [d]	After a timeout expires the AS shall behave as if TxEN would be high	AS shall signal an error to the host [c] .

Fault description	Behaviour at BP and BM	Behaviour at AS's digital interfaces [a]
AS detects an over-temperature condition [d]	AS shall not force a differential voltage on BP/BM. [b]	AS shall signal an error to the host [c] .
One of two channel termination units becomes disconnected from the channel	Note: Depending on use case specifics the communication will drop out or might continue with a huge amount of errors.	—
Bus load too high (Resistance R_{DCLoad} too low, see 8.7)	Note: Depending on use case specifics the communication will drop out or might continue with degraded performance.	—
Undervoltage on V_{IO}	—	See 15.2.
Loss of ground	AS shall internally limit the output current, see Table 50.	Product specific behaviour.

[a] In case an AS-Host interface is implemented.

[b] Biasing depends on the operation mode, see Table 49.

[c] INTN is low active, however, reading information from the SPI requires V_{DIG} and at least one supply voltage (V_{BAT} or V_{CC}) within its operating range.

[d] Detection required only while in *AS_Normal*.

13.16.2 Behaviour of unconnected digital input signals

In case one or more of the digital inputs are unconnected (or floating) the AS shall sense the inputs as defined in Table 96.

Table 96 — Logical input when unconnected

Signal	Logical input
TxD [a]	Low
TxEN [a]	High
BGE [a]	Low

[a] If present, see 13.2.

This behaviour leads to a fail silent behaviour with respect to the AS - CC interface and AS – BG interface of the AS, when TxEN or BGE is floating.

In case an AS – host Interface is present, unconnected SPI inputs have to behave according to 15.8.2.

13.16.3 Behaviour with dynamic low battery voltage

Only applicable for active stars that implement the functional class "Bus driver voltage regulator control"

For behaviour in case of dynamic low battery voltage refer to 12.12.3.

13.16.4 Behaviour with dynamic low supply voltage

For behaviour in case of dynamic low supply (V_{BAT} and V_{CC}) voltage refer to 12.12.4.

At the end of the supply voltage notch, the AS shall be in *AS_Normal* or shall be able to be forced to *AS_Normal* by a wakeup.

13.16.5 Over-temperature protection

The AS shall provide a means to monitor the junction temperature on the silicon die. If a certain product specific threshold is exceeded, the AS shall disable the transmitter in order to prevent further heating of the chip. When the over-temperature condition is no longer valid the transmitter shall be enabled at the next activity at TxEN, a single branch or the intra star interface. Entering a low power mode on over-temperature is not acceptable. The receive function shall be maintained as long as possible. The AS shall provide over-temperature information on the bus driver - host interface.

NOTE The over temperature protection is only meant as protection mechanism for the AS.

13.17 Active star signal summary

Table 97 defines the active star signal summary.

Table 97 — Active star signal summary

Signal	I/O	Description	Mandatory	Controlable	Observable
Active Star - CC Interface (optional)					
TxEN	Input	Transmit data enable not	No	If implemented	Not applicable
TxD	Input	Transmit data input	No	If implemented	Not applicable
RxD	Output	Receive data output	No	Not applicable	If implemented
Active Star - Host Interface (optional)					
SCSN	Input	Chip Select input	No	If implemented	Not applicable
SCK	Input	SPI clock input	No	If implemented	Not applicable
SDI	Input	SPI data input	No	If implemented	Not applicable
SDO	Output	SPI data output	No	Not applicable	If implemented
INT	Output	Interrupt	No	Not applicable	If implemented
Active Star - Bus Guardian Interface (optional)					
BGE	Input	BG enable input	No	If implemented	Not applicable
RxEN	Output	Receive data enable not output (optional)	No	Not applicable	If implemented
Active Star - Bus interface (single or multiple)					
BP	Input / Output	Bus line Plus	Yes	Yes	Yes
BM	Input / Output	Bus line Minus	Yes	Yes	Yes
Active Star - Power Supply interface (optional)					
INH1	Output	Control signal to power supply	No	Not applicable	Not applicable
GND	—	Primary supply voltage ground	Yes	Yes	Not applicable
V_{CC}	—	Primary supply voltage input	Yes [a]	If implemented	Not applicable
V_{BAT}	—	Secondary supply voltage input	Yes [b]	If implemented	Not applicable
V_{IO}	—	IO-Level sensing input	No	If implemented	Not applicable

a mandatory, if V_{BAT} is not implemented

b mandatory, if V_{CC} is not implemented

14 Interface definitions

14.1 Overview

In order to ensure interoperability between bus physical layer devices, communication controllers and hosts, this Clause lists the requirements on the interfaces of such devices.

14.2 Communication controller – bus driver interface

14.2.1 Introduction

To ensure that no additional asymmetry is added to the data streams by the BD-CC interface, the CC has to provide the electrical characteristics defined in the following subclauses. A CC shall provide this behaviour over the entire temperature range, which is stated in its datasheet. Qualification according to AEC-Q100 [10] is required.

14.2.2 TxEN

The TxEN signal of a CC shall meet the following definition.

Table 98 defines the TxEN signal rise and fall times.

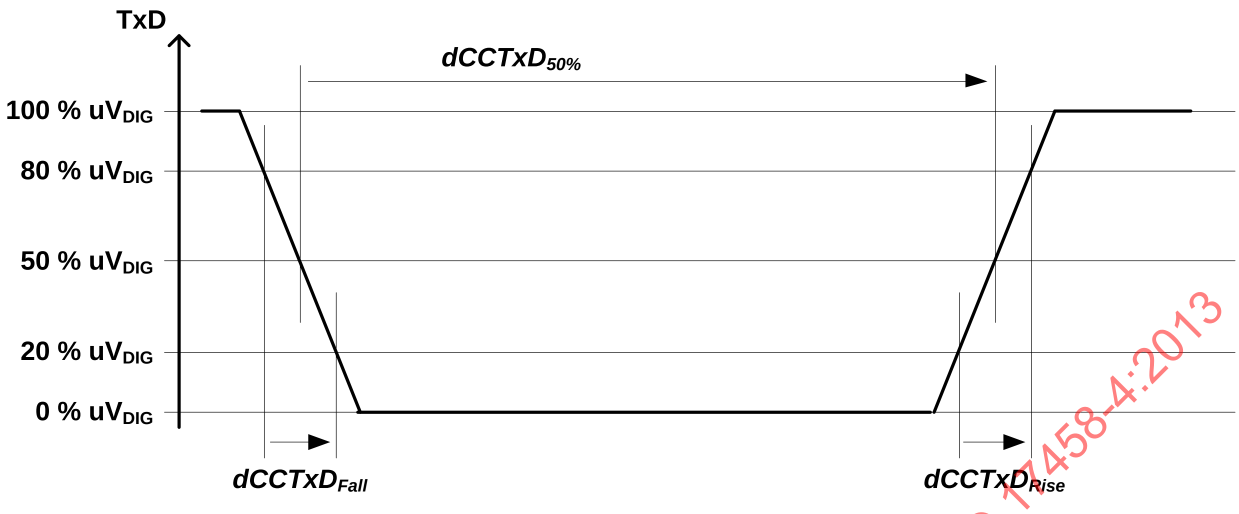
Table 98 — TxEN signal rise and fall times

Name	Description	Min	Max	Unit
$dCCTxEN_{RISE25}$	Rise time of TxEN signal at CC [a]	—	9	ns
$dCCTxEN_{Fall25}$	Fall time of TxEN signal at CC [a]	—	9	ns
dCCTxEN01	Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxEN	—	25	ns
dCCTxEN10	Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxEN	—	25	ns
[a] 20 % - 80 % uV_{DIG} at 25 pF load.				

14.2.3 TxD

The TxD signal of a CC shall meet the following definition.

Figure 65 depicts the TxD signal of the CC.



Key

TxD Transmit data

Figure 65 — TxD signal of the CC

dCCTxAsym = *dCCTxD50 %* - N × *gdBit* ; N ≤ 10 and *gdBit* = [100 ns; 200 ns; 400 ns]

Table 99 defines the requirements on TxD signal of the CC.

Table 99 — Requirements on TxD signal of the CC

Name	Description	Min	Max	Unit
dCCTxAsym	Asymmetry of sending CC at 25 pF load [a]	-2,45	2,45	ns
$dCCTxD_{Rise25}$ + $dCCTxD_{Fall25}$	Sum of rise and fall time at 25 pF load [b]	—	9	ns
dCCTxD01	Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxD	—	25	ns
dCCTxD10	Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxD	—	25	ns

a Valid for all data rates excluding clock tolerance, see also Table 18, rows 1 and 2.

b 20 % to 80 % uV_{DIG}. A datasheet for the CC shall state maximum rise and fall time on TxD separately.

It shall be verified by simulation of the CC that the sum of rise and fall time at TP1_BD does not exceed the above specified maximum in case the load is a standard lossless transmission line (with an impedance of 50 Ω and a propagation delay of 1 ns) plus a capacitor of 10 pF to ground instead of being only 25 pF.

Table 100 defines the TxD signal timing at sending BD.

Table 100 — TxD signal timing at sending BD

Description	Condition	Min	Max	Unit
TxD signal sum of rise and fall time at TP1_BD	between 20 % and 80 % uV_{DIG} at 10 pF load at the end of a 50 Ω, 1 ns microstripline	—	9	ns
NOTE The compliance to this maximum needs to be verified by simulation during the design process of the CC. The datasheet shall state a note that this is performed according to this part of ISO 17458 and the entire temperature range of the device has been taken into account. The result of the simulation has to be provided to customer on demand.				

14.2.4 RxD

The RxD input of a CC shall meet the definition of Table 101.

Table 101 — RxD input characteristics

Name	Description	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin	—	10	pF
uCCLogic_1	Threshold for detecting logical high [a]	35	70	%
uCCLogic_0	Threshold for detecting logical low [a]	30	65	%
dCCRxD01	Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, rising edge of RxD	—	10	ns
dCCRxD10	Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, falling edge of RxD	—	10	ns
[a] Relative to uV_{DIG} with *uCCLogic_1* ≥ *uCCLogic_0*, a hysteresis between the two thresholds is not required (e.g. 35 % ≤ *uCCLogic_0* ≤ 65 % and 35 % ≤ *uCCLogic_1* ≤ 65 %).				

14.2.5 Receiver asymmetry

The sampling logic in the receiving CC shall guarantee to receive every possible valid frame correctly, i.e. without errors (incl. syntax error), that has a sum of rise and fall times (20 % to 80 % of uV_{DIG}) in the RxD signal of up to 13 ns (16,5 ns) [corresponding to 15 pF (25 pF) load on RxD],a mismatch between rise and fall time of less than 5 ns (see 12.4) and a bit asymmetry (measured at 50 % of uV_{DIG}) of less than $dCCRxAsymAccept_{15}$ ($dCCRxAsymAccept_{25}$).

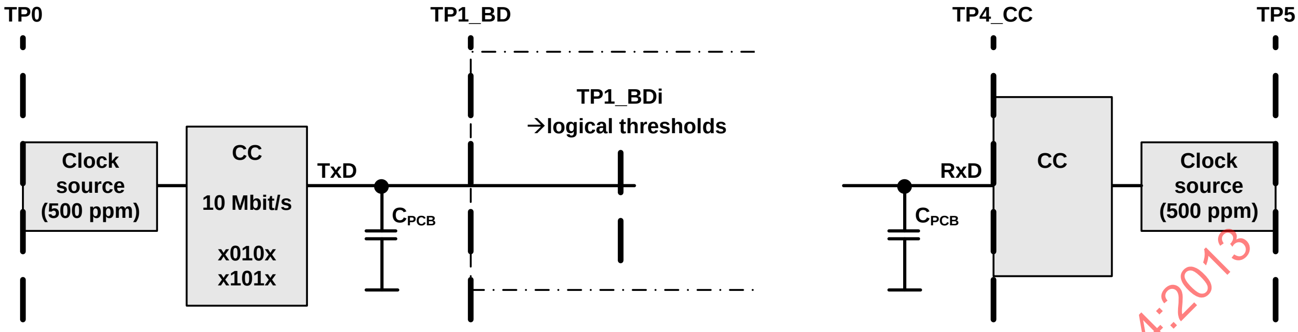
Table 102 defines the requirement on sampling logic of the CC.

Table 102 — Requirement on sampling logic of the CC

Name	Description	Min	Max	Unit
$dCCRxAsymAccept_{15}$	Acceptance of asymmetry at receiving CC with 15 pF load [a]	-31,5	+44,0	ns
$dCCRxAsymAccept_{25}$	Acceptance of asymmetry at receiving CC with 25 pF load [a]	-30,5	+43,0	ns
[a] For all data rates including clock deviation of 500 ppm. See also table 6-5 (last two rows, worst case values) with N=10 that defines a margin of 6 ns (7 ns) to the theoretical decoder limits of -37,5 ns and +50,0 ns (see Annex A). Mind that a positive asymmetry means that rising edges are delayed relative to the falling BSS edges.				

14.2.6 Communication controller system timing

From system timing perspective the definitions made in 10.5 lead to the effects depicted in Figure 66.



Key

BD Bus driver

CC Communication controller

C_{PCB} Represents the load on the pin that consists of the parasitic capacitance of the printed circuit board and the input pin capacitance of the CC.

RxD Receive data

TxD Transmit data

TP Test plane

Sum of rise and fall time on RxD ≤ 13 ns and difference of rise and fall time ≤ 5 ns (20 % to 80 % uV_{DIG})

Figure 66 — System timing at sending and receiving CC

Table 103 defines the system timing at sending and receiving CC.

Table 103 — System timing at sending and receiving CC

Description	Condition	Min	Max	Unit
asymmetry of sending CC TP0 → TP1_BDi	measured at 40 % uV_{DIG} at 25 pF load	—	4	ns
	measured at 60 % uV_{DIG} at 25 pF load	—	4	ns
Acceptance of asymmetry at receiving CC atTP4_CC 15 pF load at RxD	Sum of RxD rise and fall time ≤ 13 ns with a mismatch between rise and fall time of max. 5 ns (20 % - 80 % u_{VDIG})	-31,5	31,5	ns
Acceptance of asymmetry at receiving CC atTP4_CC 25 pF load at RxD	Sum of RxD rise and fall time ≤ 16,5 ns with a mismatch between rise and fall time of max. 5 ns (20 % - 80 % u_{VDIG})	-30,5	30,5	ns

14.3 Host

The host shall provide an interface according to 15.2 and 15.3.

In case SPI is used this shall also be according to 15.8.

15 General features for FlexRay physical layer parts

15.1 Objective

This Clause specifies general features that apply to all electrical physical layer devices.

15.2 Voltage limits for digital output signals

All digital outputs of bus drivers and active stars shall have the electrical characteristic according to Table 104.

For the BD's RxD output additional requirements are given in 12.4.

For the AS's RxD output additional requirements are given in 12.8.

Table 104 defines the digital signal output limits.

Table 104 — Digital signal output limits

Name	Description	Condition	Min	Max	Unit
$uV_{DIG\text{-}OUT\text{-}HIGH}$	Output voltage on a digital output, when in logical high state [a]	No undervoltage on V_{DIG} AND either V_{CC} or V_{BAT} supplied [b]	80	100	%
$uV_{DIG\text{-}OUT\text{-}LOW}$	Output voltage on a digital output, when in logical low state [a]	No undervoltage on V_{DIG} AND either V_{CC} or V_{BAT} supplied [b]	—	20	%
$uV_{DIG\text{-}OUT\text{-}UV}$	Output voltage on a digital output at 100 kΩ load to GND, when V_{DIG} in undervoltage	Either V_{CC} or V_{BAT} supplied [b]	—	500	mV
$uV_{DIG\text{-}OUT\text{-}OFF}$	Output voltage on a digital output at 100 kΩ load, when unsupplied [b]	—	Product pin specific behaviour		

[a] Relative to uV_{DIG}. Load conditions are product specific and documented in the product datasheet.

[b] Product specific supply thresholds below undervoltage thresholds, e.g. in *BD_Off* or *AS_Off* mode.

15.3 Input voltage thresholds for digital signals

All digital inputs, except for TxD, shall have the electrical characteristic according to Table 105, in case the reference voltage of digital IO is not in undervoltage. TxD input thresholds are specified separately for the BD (see 12.4) and AS (see 13.8.7.2). (The RxD input of the CC is specified in Clause 14).

Table 105 defines the digital signal input thresholds.

Table 105 — Digital signal input thresholds

Name	Description	Min	Max	Unit
$uV_{DIG\text{-}IN\text{-}HIGH}$	Threshold for detecting logical high [a]	—	70	%
$uV_{DIG\text{-}IN\text{-}LOW}$	Threshold for detecting logical low [a]	30	—	%

[a] Relative to uV_{DIG}

In case the reference voltage uV_{DIG} for digital IO falls below a product specific undervoltage threshold, all inputs shall be considered as if they were unconnected, see 12.12.2.

15.4 ESD protection on chip level (HBM)

All pins of FlexRay physical layer parts shall be protected against damage by electrostatic discharge (ESD) according to the Human-Body-Model JEDEC JESD22-A114 [11], as referenced by AEC-Q100 [10].

This Human-Body-Model foresees the contact discharge of a 100 pF capacitor to the pin under test with an additional series resistance of 1 500 Ω.

Those pins of FlexRay parts that are intended to be connected to terminals outside the ECU shall withstand a discharge of $uESD_{Ext}$ relative to device's ground pin. All others shall withstand a discharge of $uESD_{Int}$.

Table 106 defines the ESD protection (HBM).

Table 106 — ESD protection (HBM)

Name	Description	Min	Max	Unit
$uESD_{Ext}$	ESD protection on pins that lead to ECU external terminals [a]	6	—	kV
$uESD_{Int}$	ESD on all other pins	2	—	kV
[a] Typically: BM, BP, WAKE and V_{BAT}.				

15.5 ESD protection on chip level (IEC61000-4-2)

The IEC 61000-4-2 foresees the contact discharge of a 150 pF capacitor to the pin under test with an additional series resistance of 330 Ω.

Table 107 defines the ESD protection (see IEC 61000-4-2).

Table 107 — ESD protection (IEC 61000-4-2)

Name	Description	Min	Max	Unit
$uESD_{IEC}$	ESD protection on BP and BM	6	—	kV

15.6 ESD protection on ECU level

ESD protection at the ECU level is the responsibility of the equipment manufacturer and not part of this specification. Find application hints in Annex A for enhanced ESD protection.

15.7 Operating temperature

The FlexRay devices (BD, AS, CC) have to fulfil the requirements of this specification in at least one of the following operating temperature classes. Class 1 is the typical operating temperature class. Device qualification according to AEC-Q100 [10] is required.

Table 108 defines the operating temperature range.

Table 108 — Operating temperature range

Name	Description	Min [a]	Max [a]	Unit
T_{AMB_Class0}	Ambient temperature for class 0	-40	+150	°C
T_{AMB_Class1}	Ambient temperature for class 1	-40	+125	°C
T_{AMB_Class2}	Ambient temperature for class 2	-40	+105	°C
T_{AMB_Class3}	Ambient temperature for class 3	-40	+85	°C
The temperature in the immediate ambience of the physical layer device is meant. Qualification according to AEC-Q100 [10] is required.				
[a] The given Min. and Max. values are given the minimal range to be covered for the respective temperature class. The device might cover a larger temperature range (e.g. -45 to 140 °C).				

15.8 Serial peripheral interface (SPI)

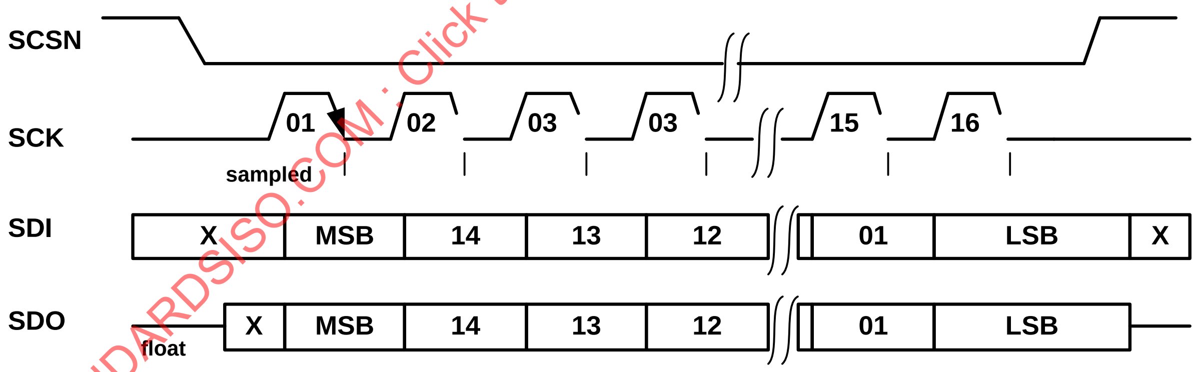
15.8.1 SPI definition

Any bit sampling is performed with the falling clock edge and the data is shifted with the rising clock edge.

The transfer speed shall at least cover the range from 10 kbit/s to 1 Mbit/s.

It is recommended to support transfer-rates up to 10 Mbit/s.

Figure 67 depicts the SPI register access.



Key

LSB	Least significant bit
MSB	Most significant bit
SCSN	SPI chip select not input
SCK	SPI clock input
SDI	SPI data input
SDO	SPI data output

Figure 67 — SPI register access

Within one SCSN cycle (SCSN on logical low), 16 clock periods (SCK) are expected for a correct access. Any deviation in the number of clock periods is recognized as an error and the write access is ignored.

15.8.2 Behaviour of unconnected SPI input pins

In case one or more of the digital inputs are unconnected (or floating) the SPI shall sense the inputs as follows:

Table 109 defines the logical input when unconnected.

Table 109 — Logical input when unconnected

Signal	Logical input
SCSN	High
SCK	Low
SDI	Low

Annex A
(informative)

Application notes

A.1 Objective

The objective of this document is to collect valuable information that shall help to implement FlexRay systems. The content of this document is informative and not normative.

A.2 Application notes

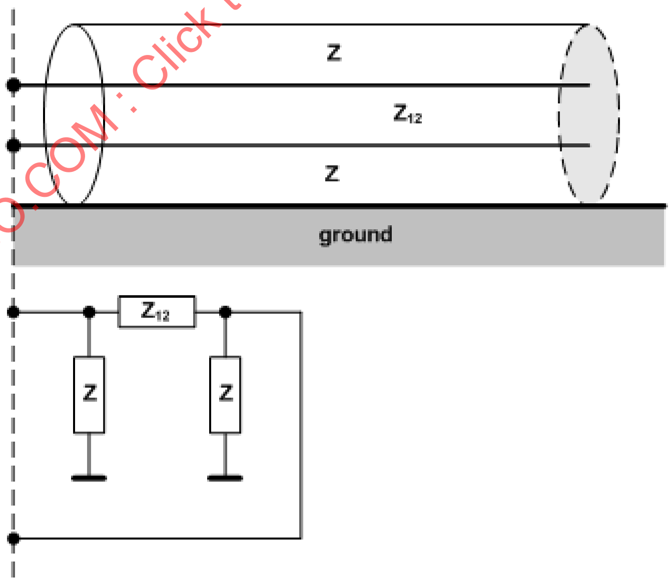
A.2.1 Application hint: Cable impedance

With a differential mode impedance in the range of [80 .. 110] Ω an optimum matching with the defined DC bus load can be achieved. Mismatches between DC bus load and cable impedance may be intentionally applied, but need to be checked application specific.

The figure below shows the equivalent input circuit of a symmetric two-wire transmission line applicable to shielded and unshielded twisted pair lines.

The differential input impedance calculates to $Z_0 = (2 \times Z) \parallel Z_{12}$

Figure A.1 depicts the cable impedance.



Key

Z Impedance wire to ground

Z_{12} Impedance wire to wire

Figure A.1 — Cable impedance

A.2.2 Application hint: Connectors

This application hint note does not prescribe certain connectors for FlexRay systems.

However, some recommendations are given in Table A.1.

Table A.1 — Connector parameters

Name	Description	Type	Unit
lContactDistance$_{BP\text{-}BM}$	Contact distance [a]	≤ 4,5	mm
lContactMetal	Distance between outer metal parts and center of contact	≥ 2	mm
lECUCoupling	Length of connector to control unit [b]	≤ 75	mm

a adjacent chambers shall be used

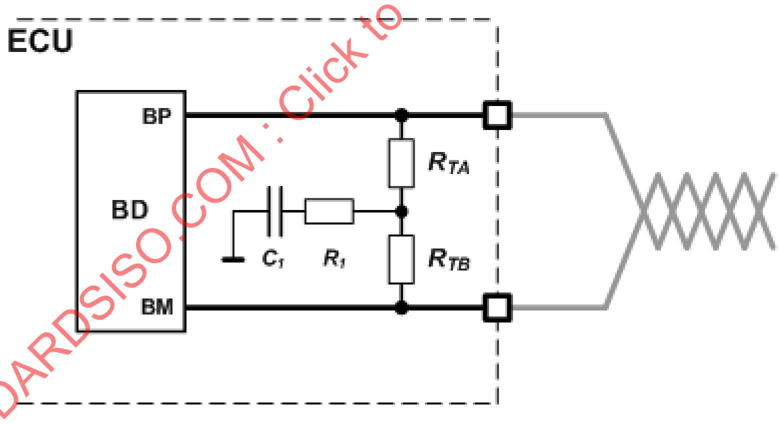
b to be measured from end of the twisted area in cable to PCB housing

See also the subclause about connectors in this part of ISO 17458.

A.2.3 Application hint: Split termination

In order to achieve a better EMC performance, it is recommended to make use of a so-called split termination in all ECUs, where the Termination resistance R_T is split into two equal parts R_{TA} and R_{TB}.

Figure A.2 depicts the ECU with split termination.



Key

BD Bus Driver

BP Bus plus

BM Bus minus

C_1 Termination capacitor

R_1 Termination resistor

R_{TA} Termination resistor

R_{TB} Termination resistor

Figure A.2 — ECU with split termination

The serial RC combination (R_1;C_1) at the center tap of the split termination provides a termination to GND for common mode signals. R_1 is preferably omitted. Typical values are given in Table A.2.

Table A.2 — Termination parameters

Name	Description	Type	Unit
R_1	Resistor	< 10	Ω
C_1	Capacitor	4 700	pF
$2 x \|R_{TA} - R_{TB}\| / (R_{TA} + R_{TB})$	Matching of termination resistors	≤ 2	%

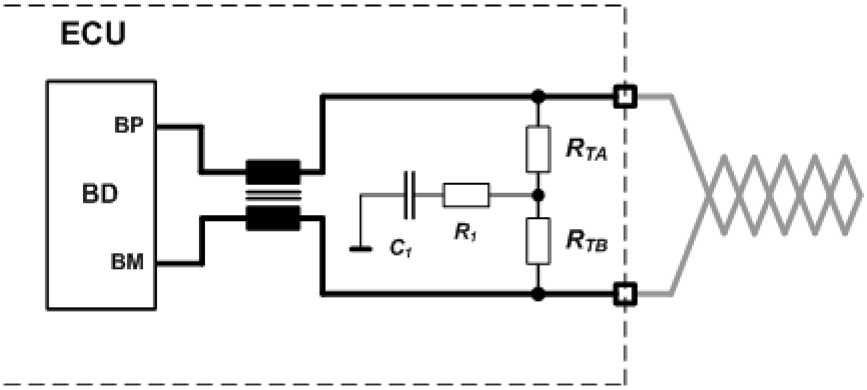
For R_{TA} and R_{TB} the use of 1 % tolerated resistors leads to a matching of 2 %; see Table A.2.

The better the matching of the split termination resistors R_{TA} and R_{TB}, the lower the electromagnetic emission.

A.2.4 Application hint: Common mode chokes

To improve the emission and immunity performance, a common mode choke may be used. The function of the common mode choke is to force the current in both signal wires to be of the same strength, but opposite direction. Therefore, the choke represents high impedance for common mode signals. The parasitic stray inductance should be as low as possible in order to keep oscillations on the bus low. The common mode choke shall be placed between transceiver and split termination. The following figure shows how to integrate the common mode choke in presence of a split termination.

Figure A.3 depicts the ECU with split termination and common mode choke.



Key

BD	Bus Driver
BP	Bus plus
BM	Bus minus
CMC	Common mode choke
ECU	Electronic control unit
C_1	Termination capacitor
R_1	Termination resistor
R_{TA}	Termination resistor
R_{TB}	Termination resistor

Figure A.3 — ECU with split termination and common mode choke

Table A.3 lists the recommended characteristics of common mode chokes in FlexRay networks.

Table A.3 — Common mode choke characteristics

Name	Description	Type	Unit
R_{CMC}	Resistance per line	≤ 1,5	Ω
L_{CMC}	Main inductance	100	µH
L	Stray inductance	< 1	µH

Mind that in case the stray inductance exceeds a certain application specific limit, a node sees activity on the bus temporarily immediately after stopping its own transmission. I.e. when last transmitted bit was *Data_1*, then a *Data_0* can be read and vice versa. For further information see Annex A.2.15.

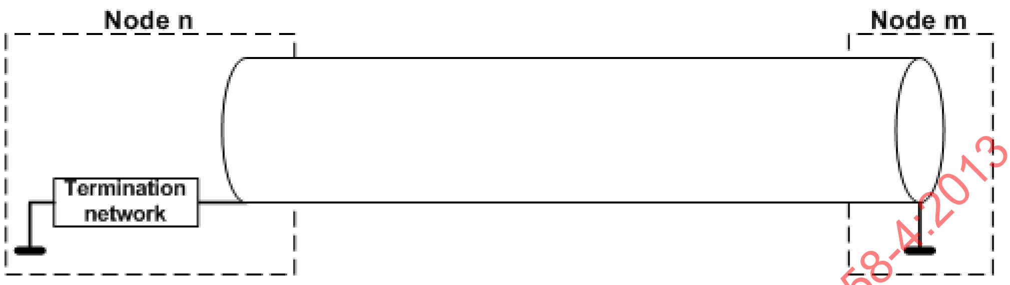
The maximum mechanical overall dimensions should not exceed the limits listed in Table A.4.

Table A.4 — Maximum mechanical dimensions

Name	Description	Min	Max	Unit
H	Height	-	5,2	mm
W	Width	-	6,0	mm
L	Length	-	10,0	mm

A.2.5 Application hint: Exemplary cable shield connection

Figure A.4 shows an exemplary cable shield connection. It is also assumed that the connectors are shielded, thus the shielding is not interrupted between two ECU housings.



Key

Node n	Node connected to a shielded cable
Node m	Node connected to a shielded cable

Figure A.4 — Exemplary cable shield connection

The short-circuited shield could cause resonances. Additional circuits to damp these resonances are up to the application.

A.2.6 Application hint: Network topology layout

Recommendations that are listed here should be followed when topologies are planned in order to increase the chance to find a reasonable termination concept, so that signal voting according to Annex A.2.20 can result in a "pass" at each node as receiver in combination with all possible sending nodes.

— Avoid "stubs on stubs". A splice shouldn't be connected to more than two other splices.

— Keep the cumulative cable length as short as possible. Avoid $\sum lStub_i + \sum lSpliceDistance_{i,j} > 24$ m.

— Connect ECUs that are optional to a separate branch of an active star in order to avoid un-terminated cable ends.

— Apply a split termination to each ECU by taking the DC-load range into account.

A.2.7 Application hint: Termination concepts

A.2.7.1 Termination concept for point to point connections

Both cable ends are terminated with a resistor (R_{TA} + R_{TB}) that has a resistance equal to the nominal cable impedance. Limitations of cable impedance and DC busload are given in this part of ISO 17458.

A.2.7.2 Termination concept for passive star topologies

At those two nodes that have the maximum electrical distance over the passive star, the cable ends are terminated with a resistance equal or slightly higher to the nominal cable impedance. At all other nodes a high ohmic split termination (e.g. 2x 1 300 Ω + 4,7 nF) should terminate the cable. Limitations of cable impedance and DC busload are given in this part of ISO 17458.

A.2.7.3 Termination concept for passive linear bus topologies

At those two nodes that have the maximum electrical distance on the bus, the cable ends are terminated with a resistance equal or slightly higher to the nominal cable impedance. At all other nodes a high ohmic split termination (e.g. 2x 1 300 Ω + 4,7 nF) should terminate the cable. Limitations of cable impedance and DC busload are given in this part of ISO 17458.

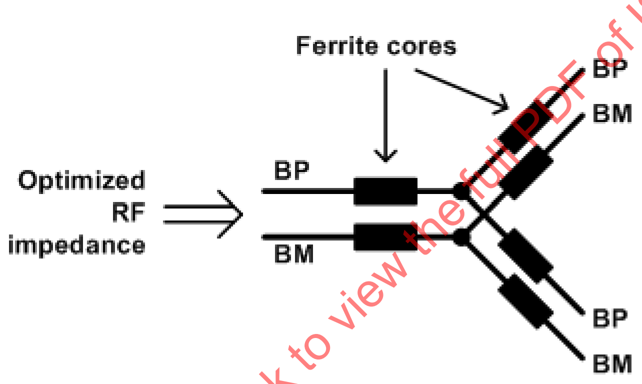
A.2.7.4 Termination in hybrid topologies

To each subclause, the termination concept is chosen as outlined in the subclauses above.

A.2.8 Application hint: Passive star - impedance adjustment

Passive star topologies tend to reflections at their low resistive center. To avoid this, ferrite cores can be used for increasing the impedance for high frequencies. Their selection is specific to the application.

Figure A.5 depicts ferrite cores on each wire at a passive star.



Key

BD Bus Driver

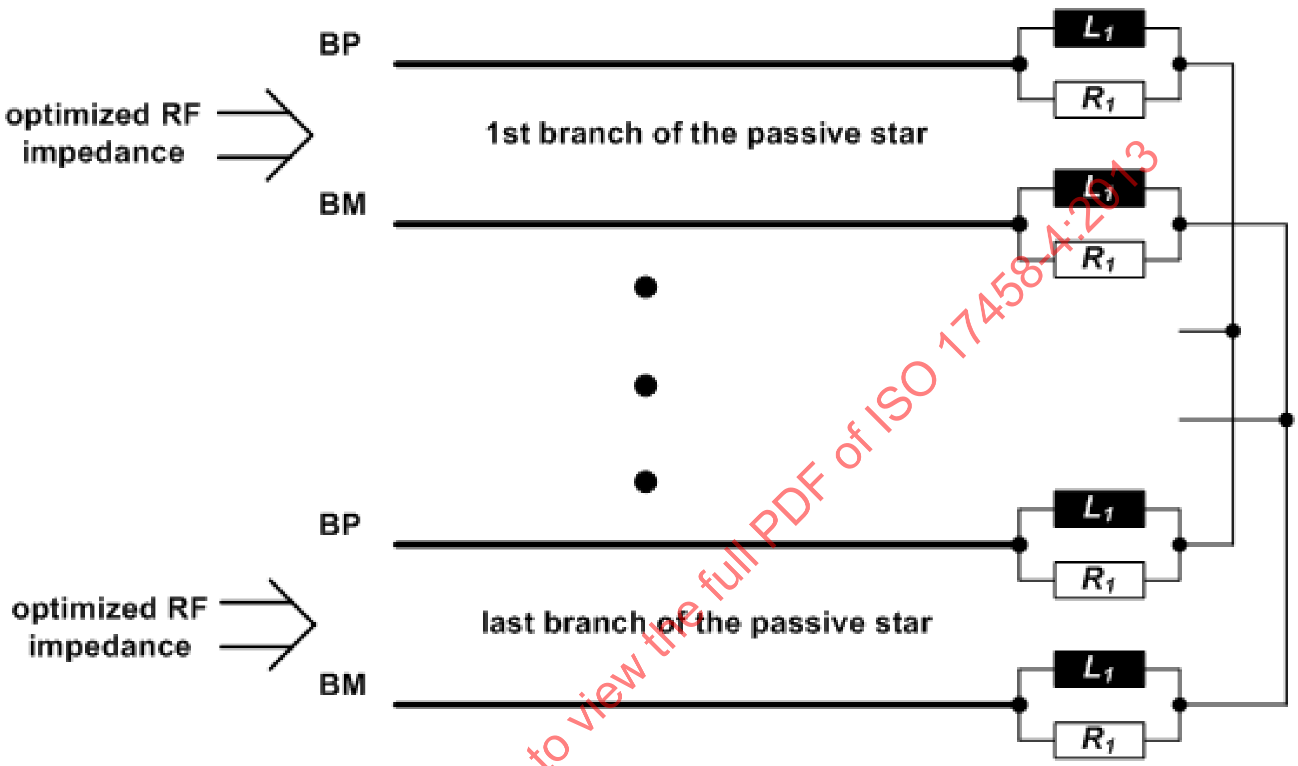
BP Bus plus

RF Radio frequency

Figure A.5 — Ferrite cores on each wire at a passive star

This impedance adjustment might be also achieved by discrete components as depicted in Figure A.6 or, in case a cable shield is used in the system as depicted in Figure A.7.

Figure A.6 depicts discrete elements for impedance adjustment at a passive star (no cable shield).



Key

BP Bus plus

BM Bus minus

L_1 Termination inductor

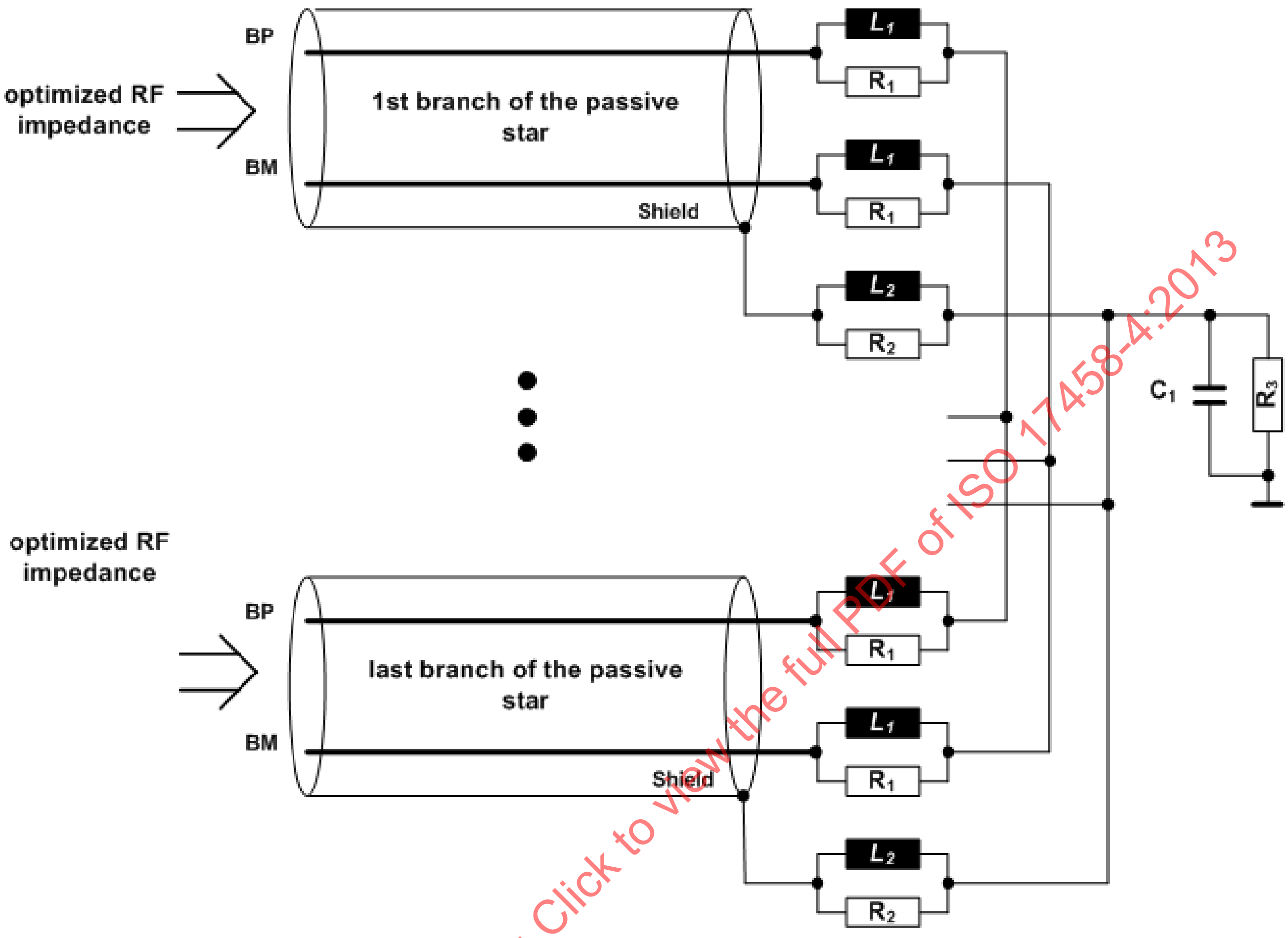
R_1 Termination resistor

RF Radio frequency

Figure A.6 — Discrete elements for impedance adjustment at a passive star (no cable shield)

or, in case a cable shield is used in the system:

Figure A.7 depicts the discrete elements for impedance adjustment at a passive star (with cable shield).



Key

BP	Bus plus
BM	Bus minus
L_1	Termination inductor
R_1	Termination resistor
L_2	Termination inductor
R_2	Termination resistor
C_1	Termination capacitor
R_3	Termination resistor
RF	Radio frequency

Figure A.7 — Discrete elements for impedance adjustment at a passive star (with cable shield)

Table A.5 defines the typical component values for impedance adjustment.

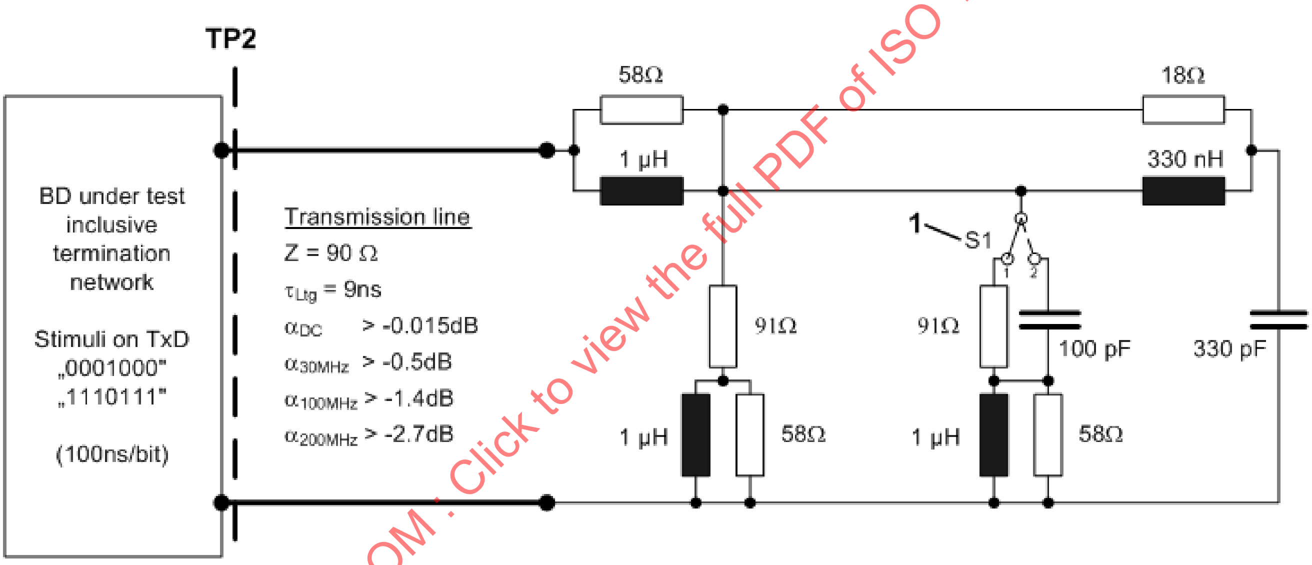
Table A.5 — Typical component values for impedance adjustment

Name	Description	Typ	Unit

R_1	Series resistance at signal wire	22	Ω
L_1	Series inductance at signal wire	220	nH
R_2	Resistance at cable shield	100	Ω
L_2	Inductance at cable shield	220	nH
R_3	Resistance at shield to system ground	1	MΩ
C_1	Capacitance to system ground	100	pF

A.2.9 Application hint: AC busload test

Figure A.8 shows a load dummy that can be connected to TP2 for AC busload investigations. The SI voting at TP2 (see Annex A.2.20) needs to result in PASS.



Key

1 Switch S1 is in default position ´1´, when the BD under test has a termination resistor; otherwise S1 is in position ´2´

BP Bus plus

T_{Ltg} Propagation delay of the line

α Attenuation

TxD Transmit data

TP Test plane

Figure A.8 — AC busload dummy

A.2.10 Application hint: Increased ESD protection

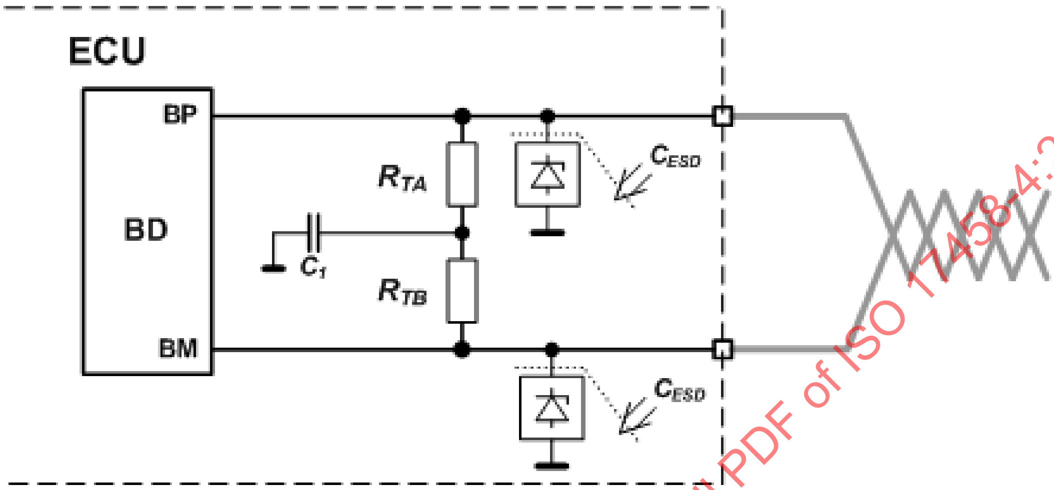
ESD protection elements typically represent a certain capacitive load on the bus lines BP and BM.

EMC investigations have shown that in case such capacitances on BP and BM do not match, the emission is increased and the RF immunity is decreased.

Therefore it is strongly recommended to strictly limit the mismatch in the entire capacitive load caused by ESD protection diodes, PCB layout, connectors and further termination circuits.

A mismatch of more than 2 % seems not to be acceptable.

Figure A.9 depicts the ESD protection diodes in an ECU.



Key

ECU Electronic control unit

BD Bus Driver

BP Bus plus

BM Bus minus

C_1 Termination capacitor

R_{TA} Termination resistor

R_{TB} Termination resistor

C_{ESD} Capacitance of the ESD protection element

Figure A.9 — ESD protection diodes in an ECU

Table A.6 defines the capacitance of ESD protection elements.

Table A.6 — Capacitance of ESD protection elements

Name	Description	Min	Max	Unit
C_{ESD}	Capacitance of ESD protection element	-	20	pF

A.2.11 Application hint: Operation at low voltage on V_{BAT}

In case communication is required during crank then sufficient bypass capacitance is expected to be existent at BD's supply voltage pins. This applies specially to conditions as specified in ISO 7637-1 – Test pulse 4 maximum severity level. Mind that the BD may enter a low power mode, when uV_{ECU} becomes less than 6,5 V, since a further voltage drop between uV_{ECU} and uV_{BAT} at the transceiver pin has to be considered due to protection diodes.

A.2.12 Application hint: Protocol relevant parameters / propagation delay

The maximum propagation delay of a transmitting BD is given by $dBDTx10 \leq 75$ ns, for a receiving BD by $dBDRx10 \leq 75$ ns and for an active star $dStarDelay_{10} \leq 150$ ns. Furthermore a limitation for the specific line (cable) delay is given in 8.2 of this part of ISO 17458 $T'_0 \leq 10$ ns/m.

Under the arbitrary chosen assumption that all cable segments have lengths up to 24 m, the following values have been calculated in Table A.7.

Table A.7 — Exemplary propagation delay

Name	Description	Min	Max	Unit
$dPLPropagationDelay0AS_{M,N}$ [a]	Propagation delay on a path without active stars from node module M to node module N	-	390	ns
$dPLPropagationDelay1AS_{M,N}$ [a]	Propagation delay on a path with one active star from node module M to node module N	-	780	ns
$dPLPropagationDelay2AS_{M,N}$ [a]	Propagation delay on a path with two active stars from node module M to node module N	-	1 170	ns
[a] *The path from TP1_BD to TP4_CC is covered, the CC-portions are not included.*				

The actual propagation delay influences the performance of the FlexRay system. An estimate of this influence can be made by using the equations given in ISO 17458-2.

The following rules of thumb can be derived:

— Minimize max { $dPropagationDelay_{M,N}$ } in order to achieve an optimum efficiency of the dynamic part and short interslot gaps.

— Minimize the difference [max { $dPropagationDelay_{M,N}$ } - min { $dPropagationDelay_{M,N}$ }] in order to achieve an optimum precision of clock synchronisation.

A.2.13 Application hint: Protocol relevant parameters / TSS and symbol length change

For calculating several protocol parameters the knowledge about the frame TSS length change and symbol length change is necessary. Relevant values are given in Table A.8 and Table A.9.

A negative value means that the symbol is shortened, a positive value means the symbol is elongated.

Table A.8 — Frame TSS length change

Name	Description	Min	Max	Unit
$dFrameTSSLengthChange0AS_{M,N}$ [a]	Frame TSS length change on a path without active stars from node module M to node module N	-400	50	ns
$dFrameTSSLengthChange1AS_{M,N}$ [a]	Frame TSS length change on a path with one active star from node module M to node module N	-850	50	ns
$dFrameTSSLengthChange2AS_{M,N}$ [a]	Frame TSS length change on a path with two active stars from node module M to node module N	-1 300	50	ns
[a] *The path from TP1_BD to TP4_CC is covered, the CC-portions are not included.*				

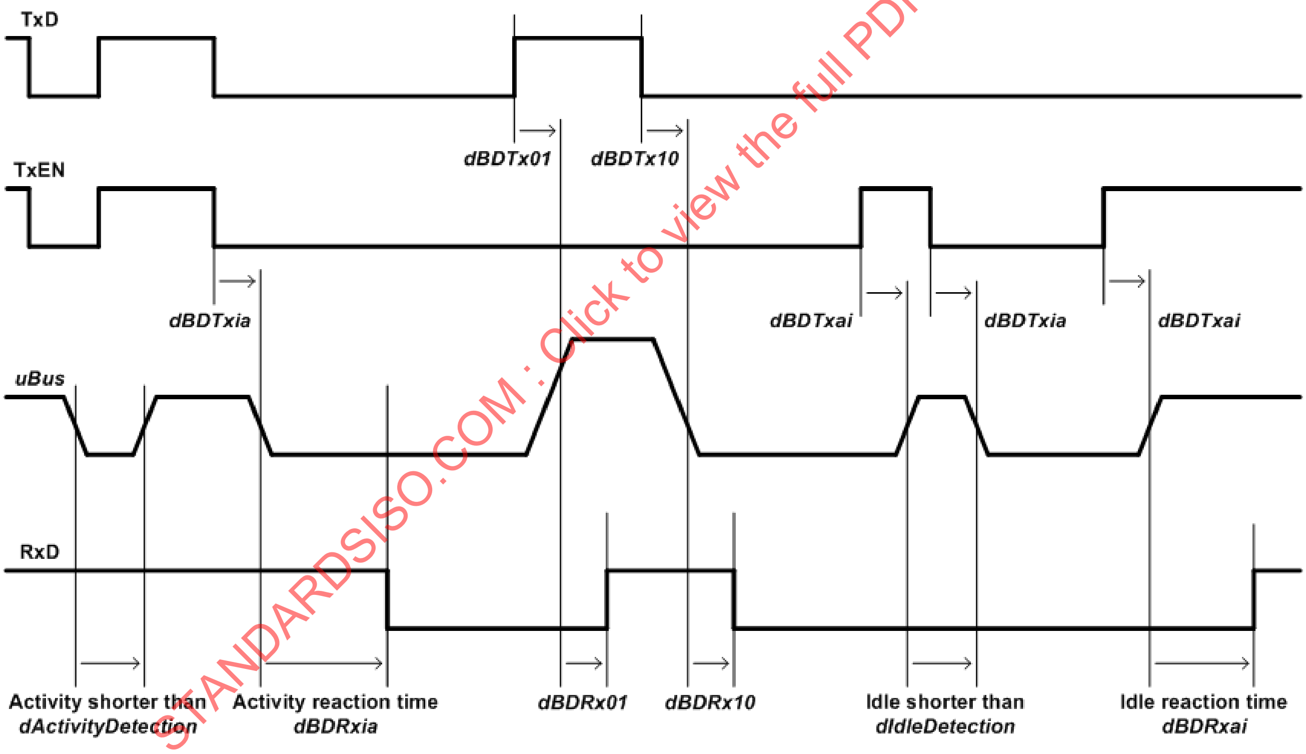
Table A.9 — Symbol length change

Name	Description	Min	Max	Unit
dSymbolLengthChange0AS$_{M,N}$ [a]	Change of length of a symbol on a path without active stars from node module M to node module N	-325	225	ns
dSymbolLengthChange1AS$_{M,N}$ [a]	Change of length of a symbol on a path with one active star from node module M to node module N	-625	675	ns
dSymbolLengthChange2AS$_{M,N}$ [a]	Change of length of a symbol on a path with two active stars from node module M to node module N	-925	1 125	ns

[a] *The path from TP1_BD to TP4_CC is covered, the CC-portions are not included.*

Mind that the minimum and maximum values in both tables do not take jitter caused by EMC effects into account. More information about EMC jitter is given in Annex A.2.14.

Figure A.10 depicts the receiver timings.



Key

TxD	Transmit data
TxEN	Transmit Enable
uBus	Differential bus voltage
RxD	Receive data

Figure A.10 — Receiver timings

Here it becomes clear that the Frame TSS length change at the receiver is caused mainly by the activity reaction time.

$$dFrameTSSLengthChange_{Receiver} = dBDRx01 - dBDRxia.$$

With *dBDRxia* = [100 .. 325] and *dBDRx01* = [0 .. 75] follows $dFrameTSSLengthChange_{Receiver}$ = [-325 .. -25].

At the transmitter the length of the TSS may also face a lengthening or shortening:

$$dFrameTSSLengthChange_{Transmitter} = dBDTx01 - dBDTxia.$$

With *dBDTxia* = [0 .. 75] and *dBDTx01* = [0 .. 75] follows $dFrameTSSLenghtChange_{Transmitter}$ = [-75 .. 75].

The two portions mentioned above lead to the resulting value for a signal path without active stars: $dFrameTSSLengthChange0AS_{M,N}$ = [-400 .. 50].

Considering the parameter *dStarTSSLengthChange*: = [-450 .. 0] it follows that:

- Resulting value for a signal path with one active star: $dFrameTSSLengthChange1AS_{M,N}$ = [-850 .. 50].
- Resulting value for a signal path with two active stars: $dFrameTSSLengthChange2AS_{M,N}$ = $dFrameTSSLengthChange_{M,N}$ = [-1 300 .. 50].

Symbol length change at the transmitter is determined as $dSymbolLengthChange_{Transmitter}$ = | dBDTxia - *dBDTxai* = *dBDTxDM* | ≤ 50ns.

Symbol length change at the receiver is determined as $dSymbolLengthChange_{Receiver} = dBDRxai - dBDRxia$.

With *dBDRxia* = [100 .. 325] and *dBDRxai* = [50 .. 275] follows $dSymbolLengthChange_{Receiver}$ = [-275 .. 175].

The two portions mentioned above lead to the resulting value for a signal path without active stars: $dSymbolLengthChange0AS_{M,N}$ = [-325 .. 225].

Considering the parameter *dStarSymbolLengthChange*: = [-300 .. 450] it follows that:

- Resulting value for a signal path with one star: $dSymbolLengthChange1AS_{M,N}$ = [-625 .. 675].
- Resulting value for a signal path with two active stars: $dSymbolLengthChange2AS_{M,N}$ = $dSymbolLengthChange_{M,N}$ = [-925 .. 1 125].

A.2.14 Application hint: Protocol relevant parameters / EMC jitter

A.2.14.1 Introduction

Injection of RF fields results in a certain jitter portions seen in the RxD signal at receiving nodes. These different portions have been investigated and the results are documented in the following subsection.

A.2.14.2 EMC jitter on data edges

Jitter on edges in the RxD signal, which are different from first transition from HIGH to LOW (start of frame) and the last transition from LOW to HIGH (the end of a frame), shall be considered in the course of system evaluation. This is discussed in detail in the following chapter in this document.

A.2.14.3 EMC jitter on TSS length

Jitter on the TSS length might lengthen or shorten the TSS additionally to the length change as described in Annex A.2.13. The empirical upper bound of this effect is given in Table A.10.

A negative value means that the TSS is shortened, a positive value means the symbol is elongated.

Table A.10 — EMC jitter on Frame TSS length change

Name	Description	Min	Max	Unit
$dFrameTSSEMIInfluence0AS_{M,N}$	Change of length of a TSS due to EMC effects in systems without active stars	-25	25	ns
$dFrameTSSEMIInfluence1AS_{M,N}$	Change of length of a TSS due to EMC effects in systems one active star per channel	-50	50	ns
$dFrameTSSEMIInfluence2AS_{M,N}$	Change of length of a TSS due to EMC effects in systems two active stars per channel	-75	75	ns

A.2.14.4 EMC jitter on symbol length change

The summation of jitter on the idle to active and active to idle edges of symbols might lead to deviations of the symbol length change as described in Annex A.2.13. The empirical upper bound of this effect is given in Table A.11.

A negative value means that the symbol is shortened, a positive value means the symbol is elongated.

Table A.11 — EMC jitter on Symbol length change

Name	Description	Min	Max	Unit
$dSymbolEMIInfluence0AS_{M,N}$	Change of length of a symbol due to EMC effects in systems without active stars	-100	200	ns
$dSymbolEMIInfluence1AS_{M,N}$	Change of length of a symbol due to EMC effects in systems with one active star per channel	-200	400	ns
$dSymbolEMIInfluence2AS_{M,N}$	Change of length of a symbol due to EMC effects in systems with two active stars per channel	-300	600	ns

A.2.15 Application hint: Protocol relevant parameters / echoes

A transmitting node may see a kind of echo after the end of transmission, which means that its RxD pin might signal additional edges after disabling the transmitter. In most cases, where echoes occur, the stray inductance of common mode chokes is too high and the network can be seen as defective.

Beside echoes also ringing (see Annex A.2.16) might affect the transmitting node. Both effects will overlay and the effect of multiple RxD switching can be combined to a time span of RxD uncertainty (*dRxUncertainty*).

Nevertheless such a time span of multiple RxD switching can be accepted by the protocol mechanisms and can be considered in the protocol configuration constraints.

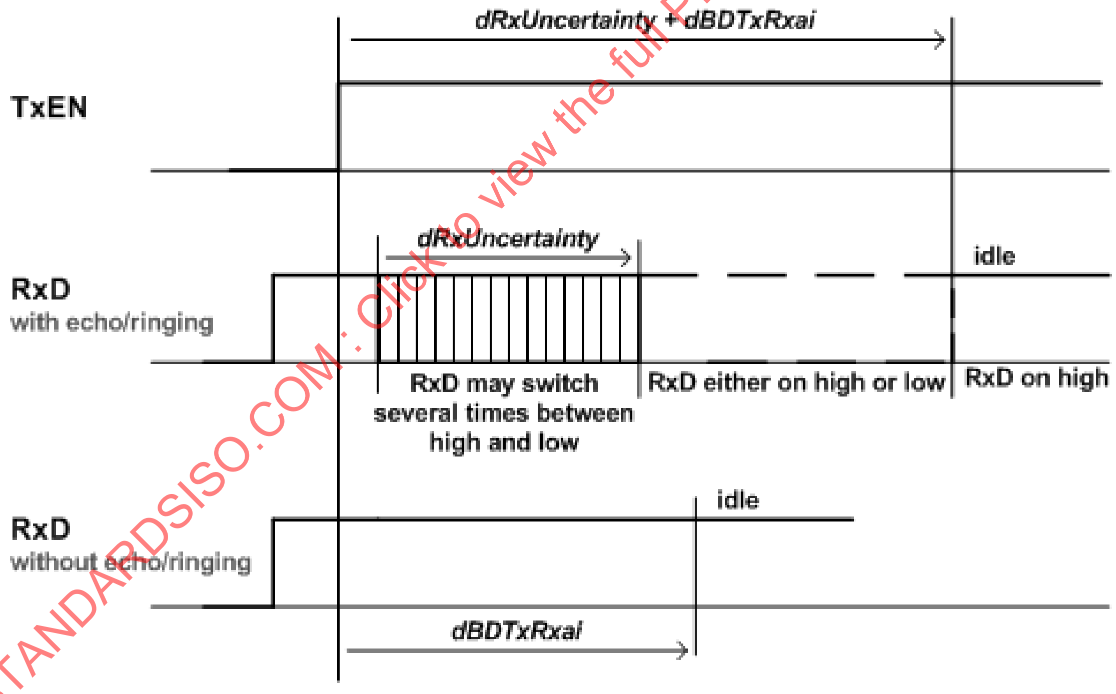
Examples of the effects of *dRxUncertainty* are given in Figure A.**11** and Figure A.**12**. In case a communication controller is connected to an active star – communication controller interface (see 13.8) the parameter *dStarTxRxai* shall be used instead of *dBDTxRxai*.

Table A.12 defines the duration of RxD instability after transmission.

Table A.12 — Duration of RxD instability after transmission

Name	Description	Min	Max	Unit
dRxUncertainty	Time following the end of a transmission where instability may occur on RxD as a result of echoes and/or ringing. During this time the RxD output may change states several times and may not reflect the actual condition of the bus.	0	250	Ns
NOTE In case ferrite cores or other inductive elements are used for impedance matching (e.g. at passive stars), *dRxUncertainty* may be even greater than 250 ns.				

Figure A.11 depicts the RxD uncertainty after frame end.



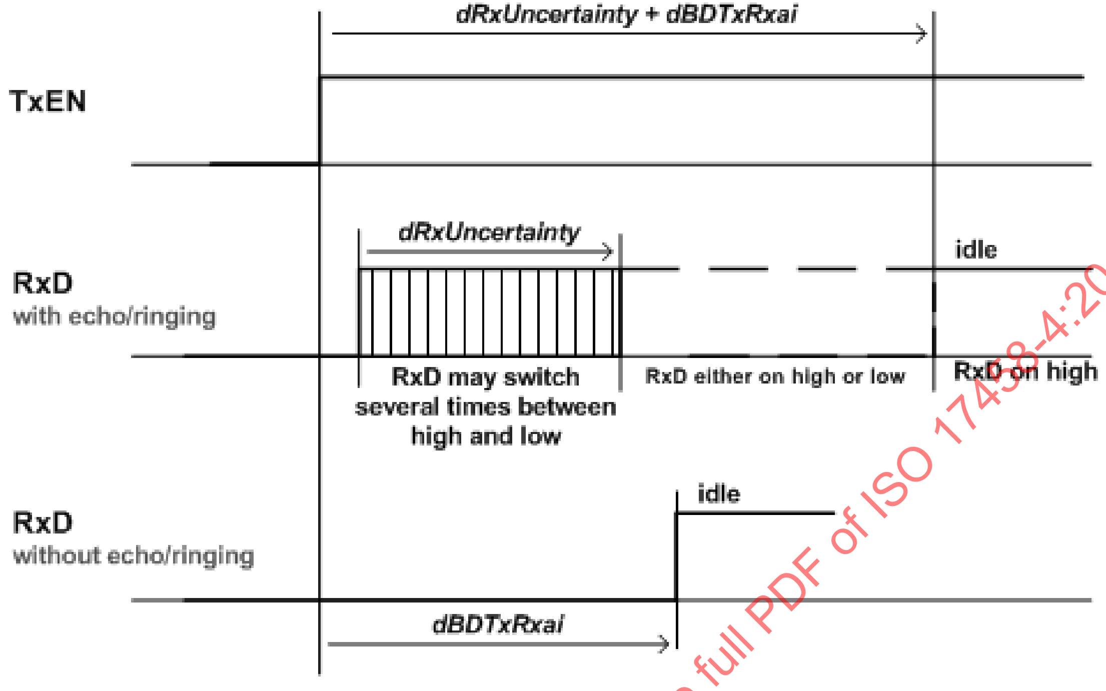
Key

TxEN Transmit Enable

RxD Receive data

Figure A.11 — RxD uncertainty after frame end

Figure A.12 depicts the RxD uncertainty after symbol end.



Key

TxEN Transmit Enable

RxD Receive data

Figure A.12 — RxD uncertainty after symbol end

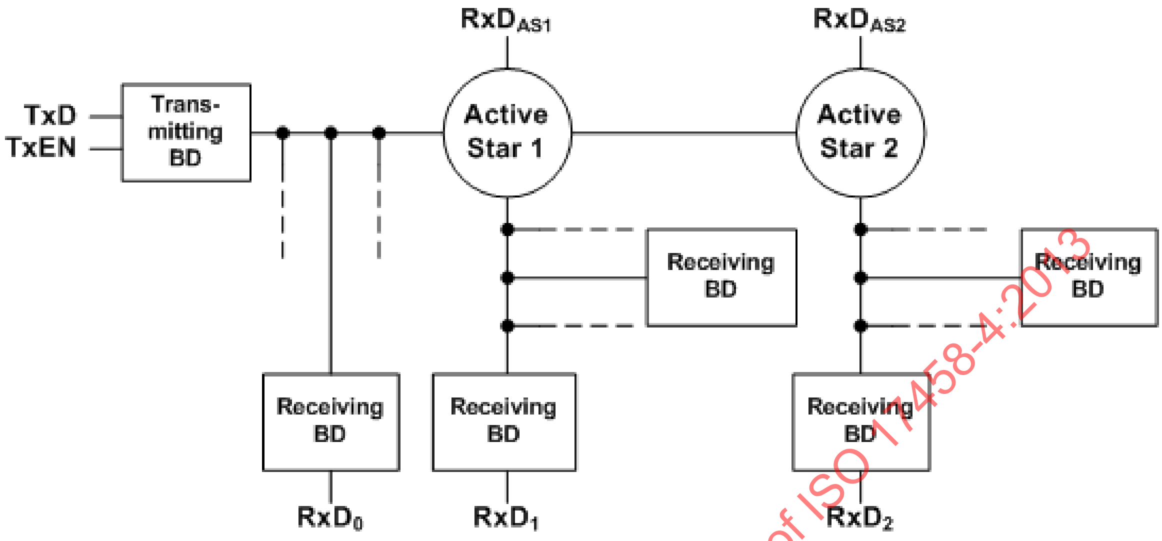
A.2.16 Application hint: Protocol relevant parameters / ringing

A receiving node or active star may see a kind of ringing at the end of a received signal.

In the description below, ringing is described as a period of instability following the end of the FES high bit, i.e., the description assumes that transmission is turned off after the FES high bit, as it would be for a frame transmission in the static segment. Note, however, that ringing with similar characteristics could also occur at the end of all other types of transmission, for example at the end of the DTS for frame transmissions in the dynamic segment or at the end of the active low phase in a WUS transmission.

Such ringing can be accepted by the protocol mechanisms and can be considered in calculating protocol configuration parameters. The ringing takes different effect depending on the location of the receiver in the network.

Figure A.13 depicts the different positions of RxD signals in a FlexRay network.



Key

BD Bus Driver

TxD Transmit data

TxEN Transmit enable

RxD Receive data

Figure A.13 — Different positions of RxD signals in a FlexRay network

Table A.13 defines the ringing period in different network types.

Table A.13 — Ringing period in different network types

Name	Description	Min	Max	Unit
$dRingRxD_0$	Time following the FES1 where instability may occur on RxD without pass through active stars	0	525	ns
$dRingRxD_{AS1}$	Time following the FES1 where instability may occur on RxD at the first receiving active star in a network	0	800	ns
$dRingRxD_1$	Time following the FES1 where instability may occur on RxD when signal passed through one active star	0	1 225	ns
$dRingRxD_{AS2}$	Time following the FES1 where instability may occur on RxD at the second receiving active star in a network	0	1 250	ns
$dRingRxD_2$	Time following the FES1 where instability may occur on RxD when signal passed through two active stars	0	1 675	ns

When ringing occurs the RxD signal may switch multiple times and ends either on logical high or logical low, which cannot be predicted. From the perspective of a receiving node the worst case occurs when the ringing period ends with a logical low RxD signal. In this case the idle detection after transmission of a frame is delayed by the duration of ringing plus the idle reaction time. The idle detection time after transmission of a symbol is delayed by the duration of the ringing.

Figure A.14 shows the receivers behaviour with the maximum timings. The hatched areas indicate the time span in which ringing at the bus may occur and the RxD signal may switch multiple times. The white rectangles indicate time spans in which the RxD signal is stable; either on low or on high. When the receiver is in idle the RxD signal is on logical high.

Table A.13 shows the worst case values (i.e. for ringing that ends on active low) for different topologies and for nodes which are located a various positions within these topologies. These values are calculated under the assumption that the duration of ringing (*dRing*) does not exceed 250 ns. This value is also the basis for the derivation of parameter ranges in ISO 17458-2.

In case ferrite cores or other inductive elements are used for impedance matching (e.g. at passive stars), ringing periods may get even longer than 250 ns.

Table A.14 defines the educated guess of ringing period.

Table A.14 — Educated guess of ringing period

Name	Description	Min	Max	Unit
dRing	Educated guess for the ringing period	0	250	ns

The effect of ringing with respect to the resulting RxD signal is depending whether the transmission ends with an active high bit or with an active low bit. In three cases the transmission ends with an active high bit:

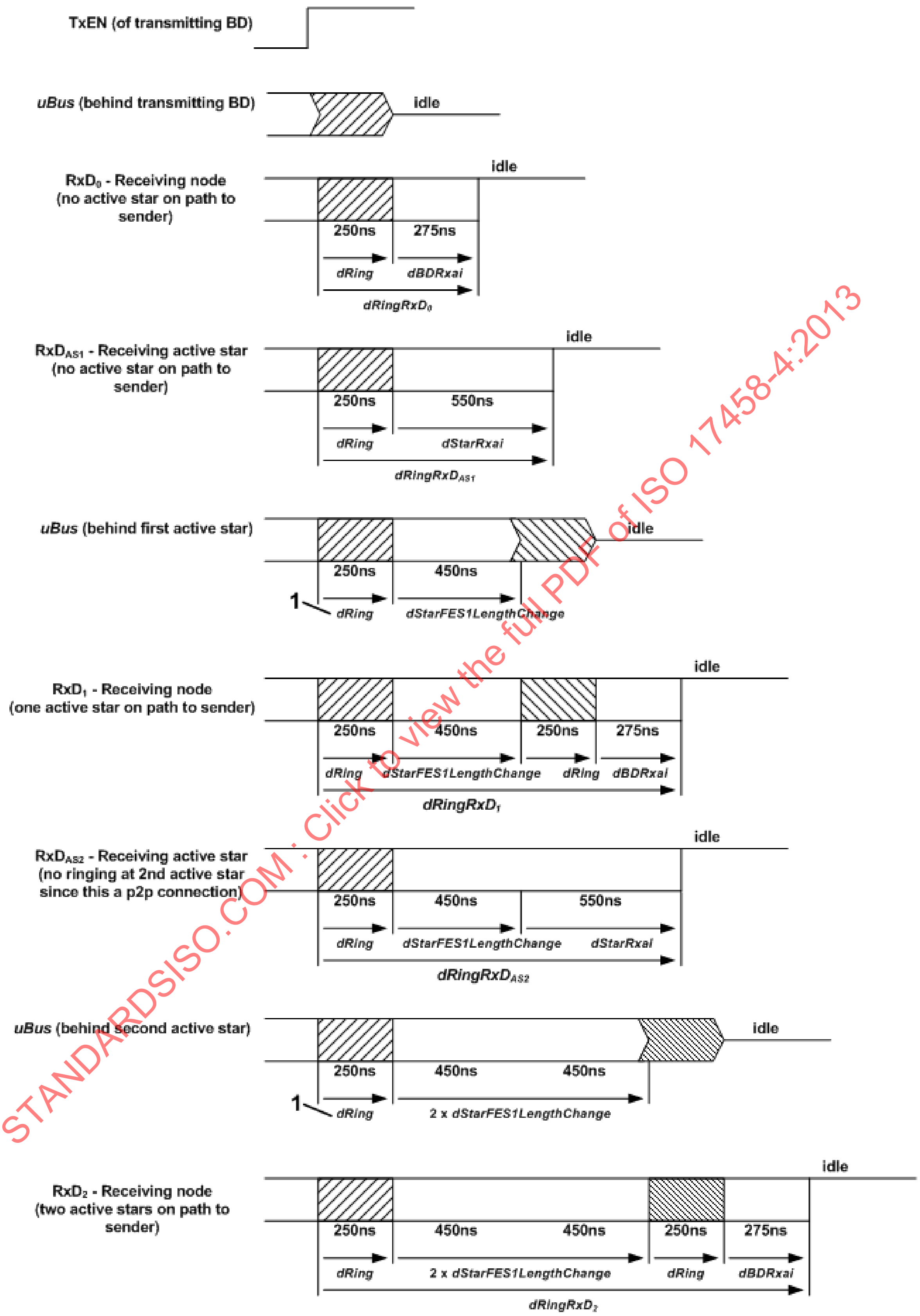
— FES high bit after the transmission of a static frame (see Figure "Frame encoding in the static segment" in ISO 17458-2),

— DTS high bit after the transmission of a dynamic frame (see Figure "Frame encoding in the dynamic segment" in ISO 17458-2),

— Additional high bit after the transmission of a WUDOP (see Figure "Wakeup during operation pattern" in ISO 17458-2);

The transmission of a symbol (WUS, CAS, MTS) ends on an active low bit.

Figure A.15 gives an example for the resulting RxD_2 signal for different scenarios (frame vs. symbol) with and without ringing.



Key

1 Received ringing is actively forwarded by the active star

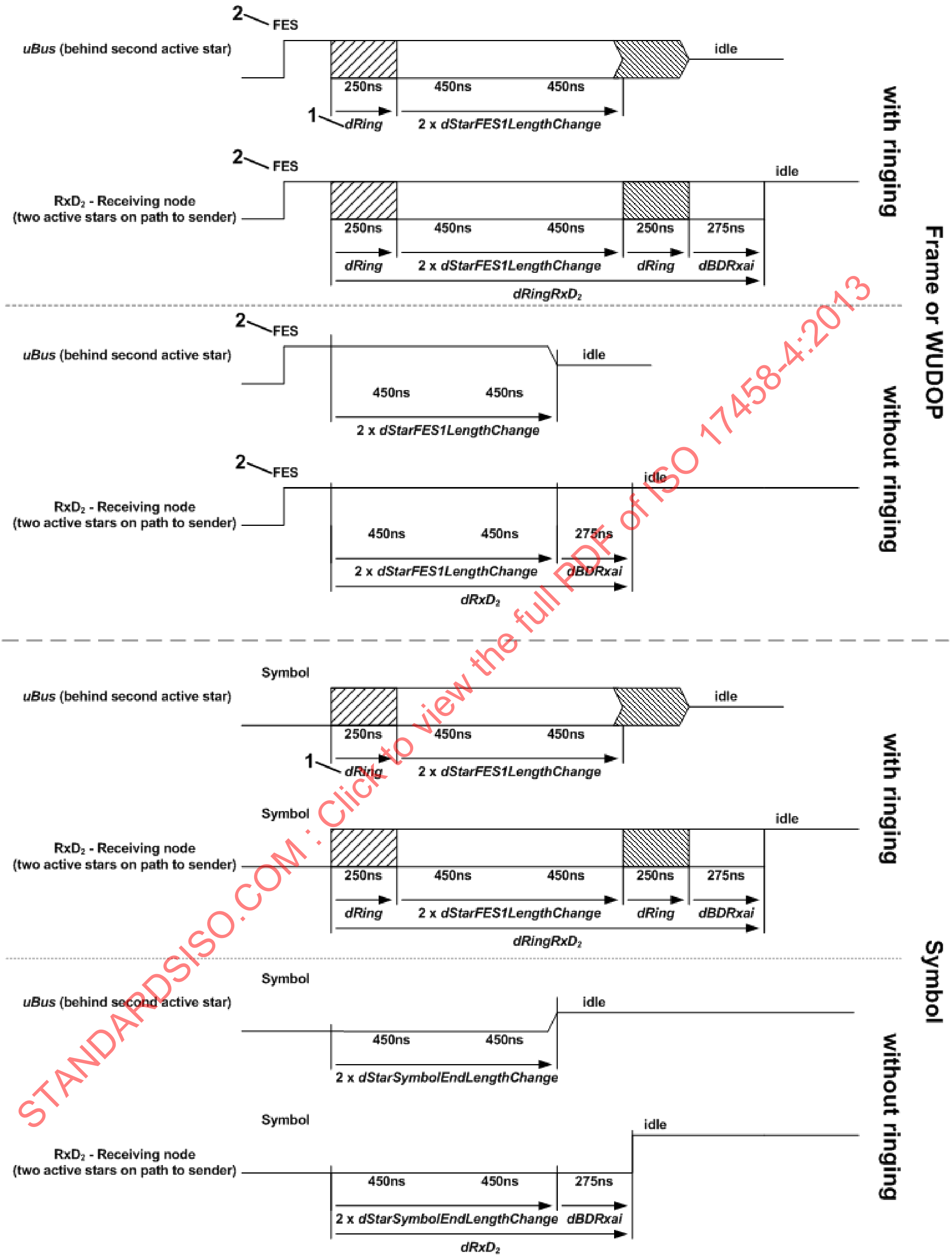
BD Bus Driver

TxEN Transmit enable

uBus Differential bus voltage

RxD Receive data

Figure A.14 — Ringing after transmission end



Key

1	Received ringing is actively forwarded by the active star
2	FES or DTS or additional high bit after WUDOP (see [PS09])
FES	Frame End Sequence

uBus Differential bus voltage

RxD Receive data

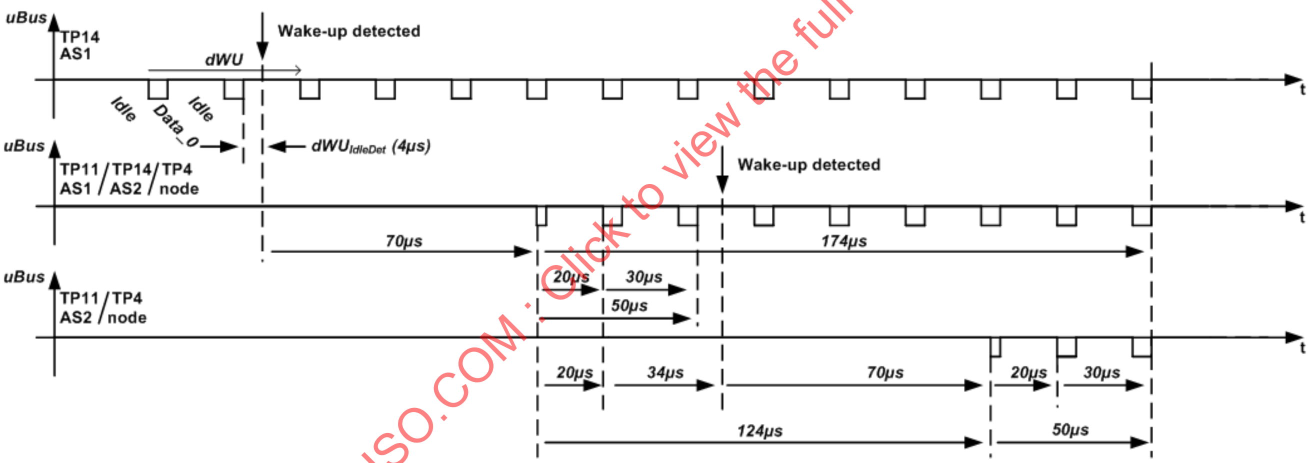
Figure A.15 — Example for transmission end with and without ringing

A.2.17 Application hint: Active star / wakeup reaction

In case of non-monolithic implementations, only the active star device with the branch that receives the wakeup event has to initiate the transition to *AS_Normal* on this remote wakeup. Other active star devices used in the same non-monolithic active star shall initiate the transition to *AS_Normal* latest on the next activity that is signaled on the intra star interface between the different active star devices.

The system designer shall ensure that a stabilized voltage supply is available latest *dStarMainSupply* after the remote wakeup event was detected; i.e. the AS has re-entered *AS_Normal* after *dStarMainSupply* after wakeup, in case the capacitor could not bridge the voltage regulator ramp up.

The AS needs to forward a minimum number of wakeup pattern after its wakeup to ensure a proper wakeup of the network. Figure A.16 depicts the exemplary situation with 2 active stars, with timings ensuring a sufficient wakeup pattern at the branches of the 2nd AS. In case the AS is supplied solely out of a capacitor after wakeup, this capacitor, which is charged out of V_{BAT}, shall be able to sufficiently supply the AS for at least *dStarAuxSupply*.



Key

TP Test plain

uBus Differential bus voltage

Figure A.16 — Wakeup timing

Table A.15 defines the active star wakeup reaction time.

Table A.15 — Active star wakeup reaction time

Name	Description	Min	Max	Unit
dStarAuxSupply$_{1AS}$ [a]	Time during the AS is supplied from an auxiliary supply (e.g. storage capacitor) when a network with 1 active stars is used	50	-	µs
dStarAuxSupply$_{2AS}$ [a]	Time during the AS is supplied from an auxiliary supply (e.g. storage capacitor) when a network with 2 active stars is used	174	-	µs
dStarMainSupply [a]	Time after that the AS gets stabilized voltage supply	-	100	ms
[a] *Parameter on system level*				

NOTE For the calculation of the timings it is expected that during the wakeup reaction time (max. 70 µs) the active star is supplied out of V_{BAT}. If not, this extra time needs to be considered for the dimensioning of a capacitor.

A.2.18 Application hint: Active star / branch recovery

An active star will deactivate branches upon detection of error conditions (see subclause 13.6).

Unless the host steps in to prevent it branch recovery could occur at any time, and this recovery might have temporary implications on the operation of the protocol.

See ISO 17458-2 for mechanisms by which the slot counters can become desynchronized, the implications and limitations on the scope of the damage.

A.2.19 Application hint: Eye-diagram

A.2.19.1 Objective

The eye diagram is an easy to use tool to estimate jitter and signal quality in serial data systems. In FlexRay systems it is a fast and helpful tool to obtain an overview about jitter, noise, reflections, amplitude difference between various nodes, and possibly errant edge timing problems in the system. Nevertheless for the physical layer testing it is insufficient to be used as a signal integrity compliance test alone because reflections and glitches could fail the eye diagram even though the communication controller works faultless. The main reason for this is the low-pass filter characteristic of the FlexRay bus driver as well as the FlexRay glitch filter and signal voting in the communication controller, which could eliminate the negative effect of short glitches and reflections.

The "SI voting" as described in Annex A.2.20 makes another assessment of the signal quality.

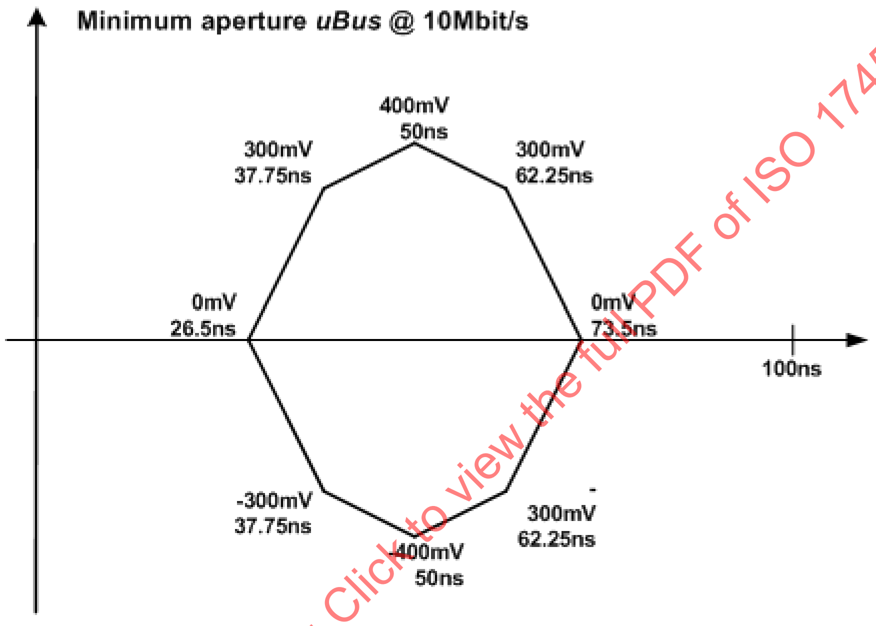
To see all effects of signal variation in the eye diagram, including jitter, the eye shall be created from consecutive bits from one or more FlexRay frames. The more frames are used to create the eye diagram, the more confidence it gives in the signal integrity performance of the FlexRay under test. Therefore the eye-diagram shall be created using an oscilloscope with special software that extracts/recovers the clock from the data signal. The FlexRay receiver's clock recovery hardware has to be emulated. The capturing method for the eye diagram is described in Annex A.2.19.3.

A.2.19.2 Eye-diagrams for different data rates

A.2.19.2.1 Eye-diagram for 10 Mbit/s

The eye diagram timing for 10 Mbit/s is based on the decoder requirement of 62,5 ns (= 5/8 x *gdBit*) plus 11 ns asymmetry on the path from TP4 to TP5. An implemented eye diagram procedure is assumed to be synchronized every 10 Bits (falling BSS edges, see Annex A.2.19.3).

Figure A.17 depicts the FlexRay eye-diagram @ 10 Mbit/s.



Key

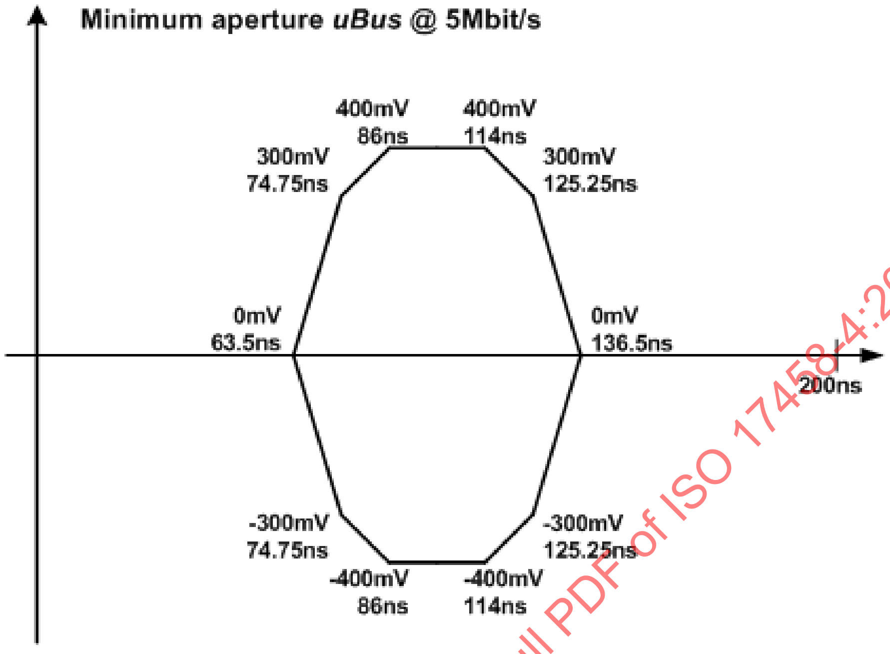
uBus Differential bus voltage

Figure A.17 — FlexRay eye-diagram @ 10 Mbit/s

A.2.19.2.2 Eye-diagram for 5 Mbit/s

The eye diagram timing for 5 Mbit/s is based on the decoder requirement of 125 ns (= 5/8 x *gdBit*) plus 11,5 ns asymmetry on the path from TP4 to TP5. An implemented eye diagram procedure is assumed to be synchronized every 10 Bits (falling BSS edges, see Annex A.2.19.3).

Figure A.18 depicts the FlexRay eye-diagram @ 5Mbit/s.



Key

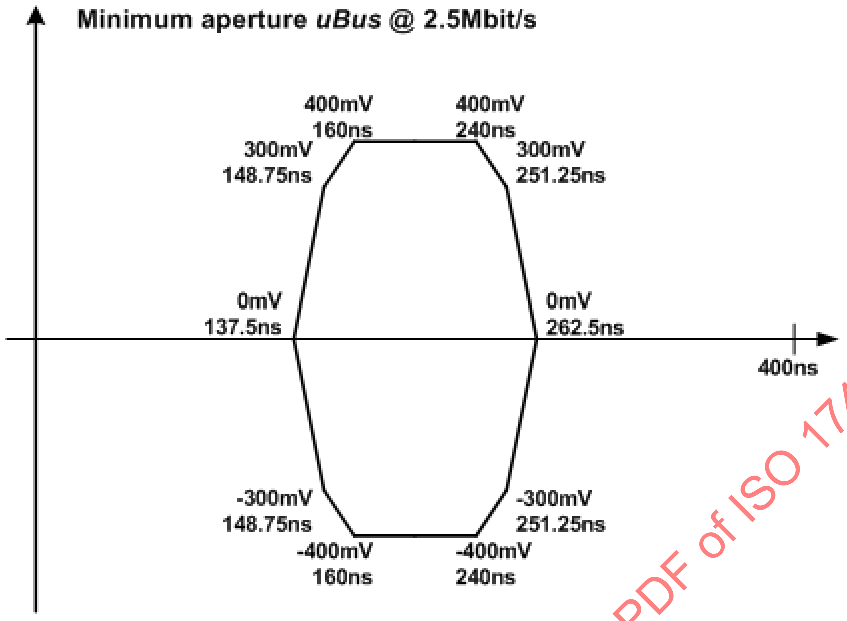
uBus Differential bus voltage

Figure A.18 — FlexRay eye-diagram @ 5 Mbit/s

A.2.19.2.3 Eye-diagram for 2.5 Mbit/s

The eye diagram timing for 2.5 Mbit/s is based on the decoder requirement of 250 ns (= 5/8 x *gdBit*) plus 12,5 ns asymmetry on the path from TP4 to TP5. An implemented eye diagram procedure is assumed to be synchronized every 10 Bits (falling BSS edges, see Annex A.2.19.3).

Figure A.19 depicts the FlexRay eye-diagram @ 2.5 Mbit/s.



Key

uBus Differential bus voltage

Figure A.19 — FlexRay eye-diagram @ 2.5 Mbit/s

A.2.19.3 Capturing method

To recover the receiver's clock the oscilloscope has to find the first BSS event (= falling edge in the BSS) after the TSS and looks for the next BSS events to occur within 10 ± ½ bit fields after the prior BSS event. With each BSS event, the oscilloscope generates ideal clocks synchronized to this BSS event. This process of generating ideal clocks synchronized to each BSS event continues until the oscilloscope detects the frame-end-sequence (FES). If the oscilloscope fails to find a BSS event within 10 ± ½ bits fields after the prior BSS event, the clock recovery shall be aborted until detection of the next TSS event.

After generating the ideal clocks synchronized to each BSS event for the entire acquisition, the scope "slices" the acquired waveform into single bit field segments based on the timing of the recovered clocks. These "slices," are overlaid on top of each another to create the real-time FlexRay eye-diagram.

Figure A.20 depicts the generation of FlexRay eye-diagrams.

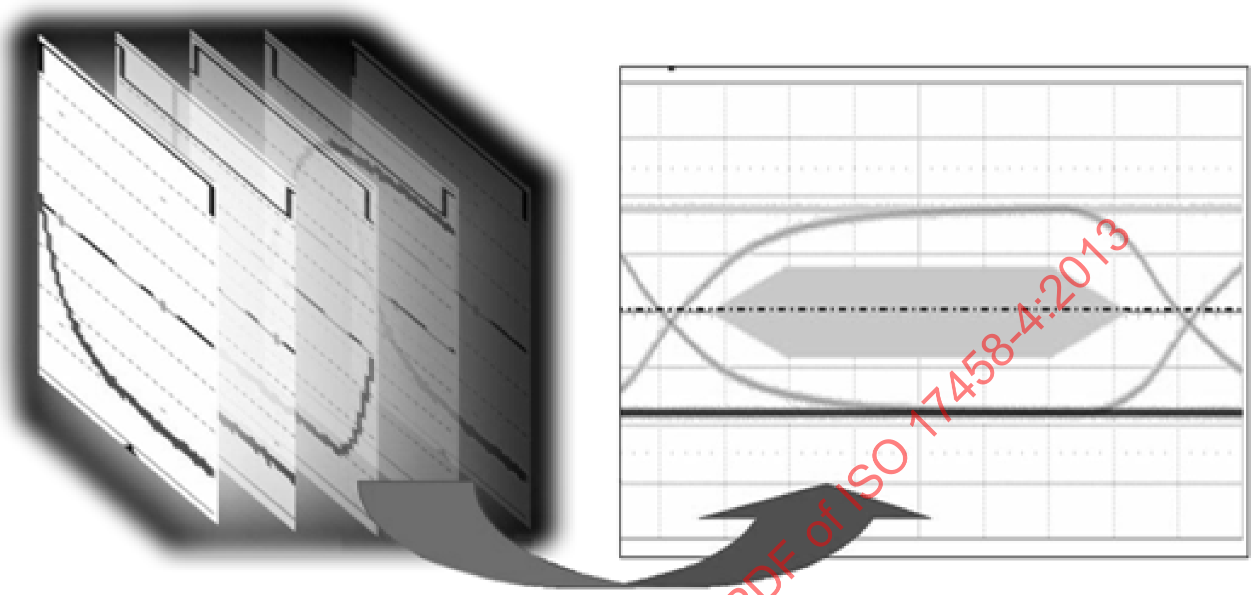


Figure A.20 — Generation of FlexRay eye-diagrams

Advantageously the oscilloscope allows using all captured frames as well as using only selected frames; e.g. those which are sent by one selected node, to generate the eye-diagram.

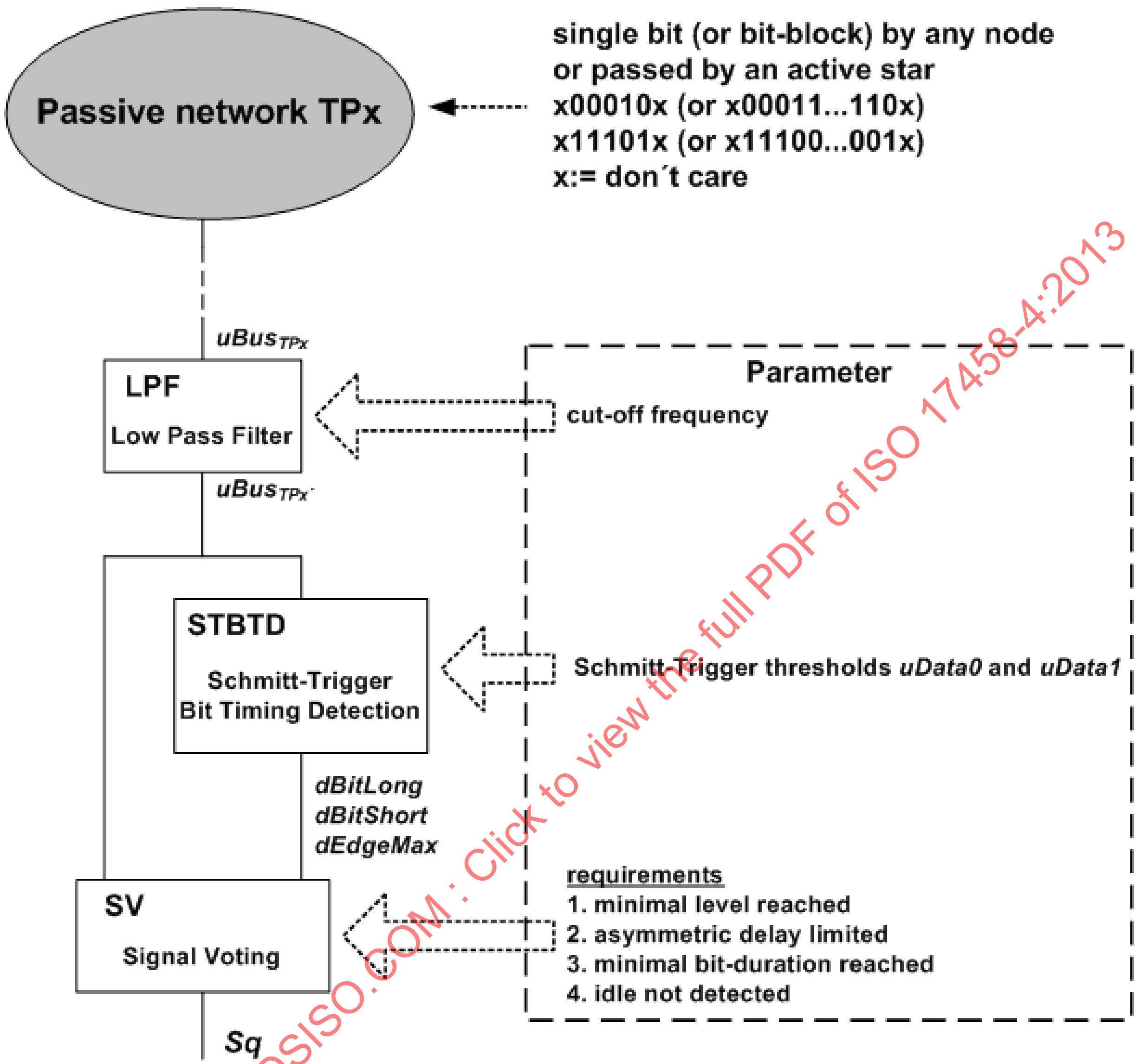
A.2.20 Signal integrity voting

A.2.20.1 Description of voting method

An eye diagram test applied to any passive network is going to fail in case of reflections even if the communication works faultlessly. Reflections appear in e.g. passive stars. The signal integrity voting is a procedure following the example given by the BD properties and its robustness against disturbances.

The procedure detects whether a FlexRay topology is operable or not in principle. Differential bus signal shapes measured at any position are taken into account. The signal integrity voting is a mathematical calculation procedure. Any block of identical bits in a row preceded and followed by an inverted bit (consecutive edges) can be used. To keep the description simple, a single bit is assumed.

Figure A.21 depicts the single bit signal integrity model.



Key

uBus	Differential bus voltage
TP	Test plain
Sq	Signal quality

Figure A.21 — Single bit signal integrity model

In the 1st step the measured differential signal $uBus_{TPx}$ passes a mathematically perfect low-pass filter. The resulting signal $uBus_{TPx'}$ should meet minimal level requirements (level test). In the 2nd step the signal $uBus_{TPx'}$ passes a Schmitt-Trigger with the threshold variations according to Table A.18. The resulting bit-timing has to meet the specified requirement (bit-timing test). The voting result *Sq* summarizes the results of the level test and the bit-timing tests.

A.2.20.2 Low pass filter (LPF)

Table A.16 defines the low pass filter characteristics.

Table A.16 — Low pass filter characteristics

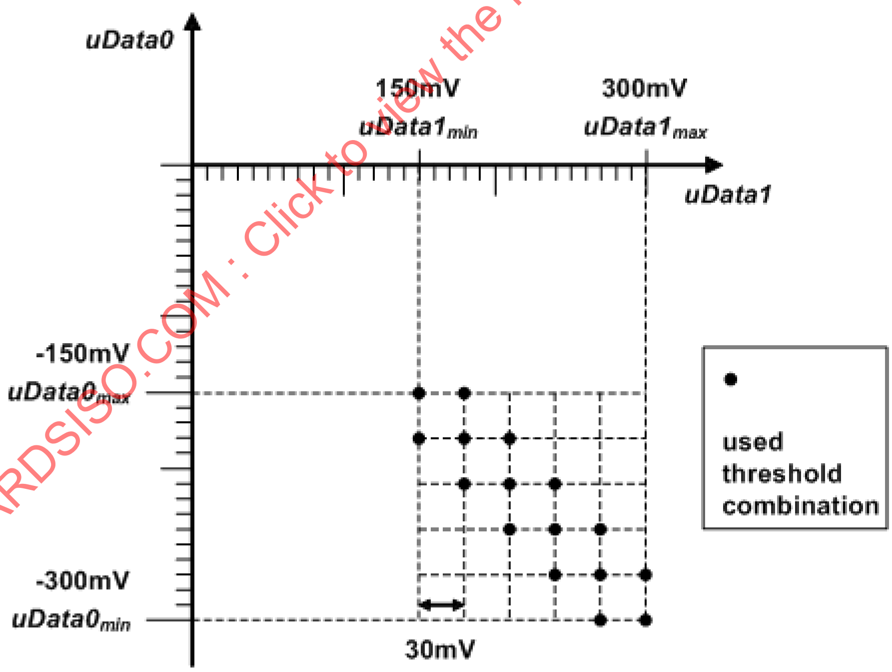
IN	$uBus_{TPx}$	Measured differential voltage at any test plane
OUT	$uBus_{TPx'}$	Filtered differential voltage signal
PARAMETER	$fSIVoting_{cutoff}$	The 3 dB cut off frequency is 14 MHz
BEHAVIOUR	1st order low pass filter, infinite input impedance	

Standard oscilloscopes offer to limit the measuring bandwidth down to 20 MHz. Using this feature allows to get an impression of the signal integrity easily.

A.2.20.3 Schmitt trigger bit timing detection (STBTD)

According to Table 40 the data detection thresholds *uData0* und *uData1* have to match. The tolerance range has to be sampled with a 30 mV resolution.

Figure A.22 depicts the threshold tolerances and their test coverage.



Key

uData0 Differential bus voltage corresponding to Data_0

uData1 Differential bus voltage corresponding to Data_1

Figure A.22 — Threshold tolerances and their test coverage

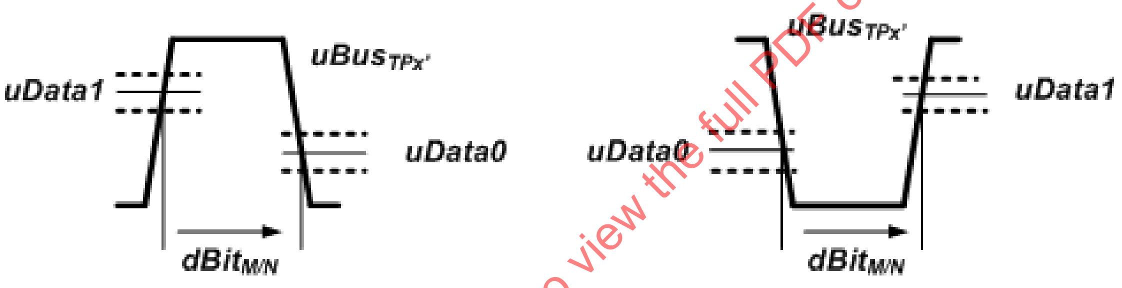
Table A.17 defines the signal voting parameter list.

Table A.17 — Signal voting parameter list

IN	*$uBus_{TPx'}$*	Filtered differential voltage signal
OUT	*dBitLong*	Longest detectable duration of one bit [a]
	dBitShort	Shortest detectable duration of one bit [a]
	dEdgeMax	Duration slowest edge
PARAMETER	*uData1*	*Data_1* threshold (see behaviour)
	uData0	*Data_0* threshold (see behaviour)

[a] *determined by applying all threshold combinations shown in **Figure A.22 — Threshold tolerances and their test coverage** .*

Figure A.23 depicts the Signal voting – bit length measurements.



a) Single target bit x00010x   b) Single target bit x11101x

Key

uBus   Differential bus voltage

uData0   Differential bus voltage corresponding to Data_0

uData1   Differential bus voltage corresponding to Data_1

Figure A.23 — Signal voting – bit length measurements