IEC/PAS 62326-14

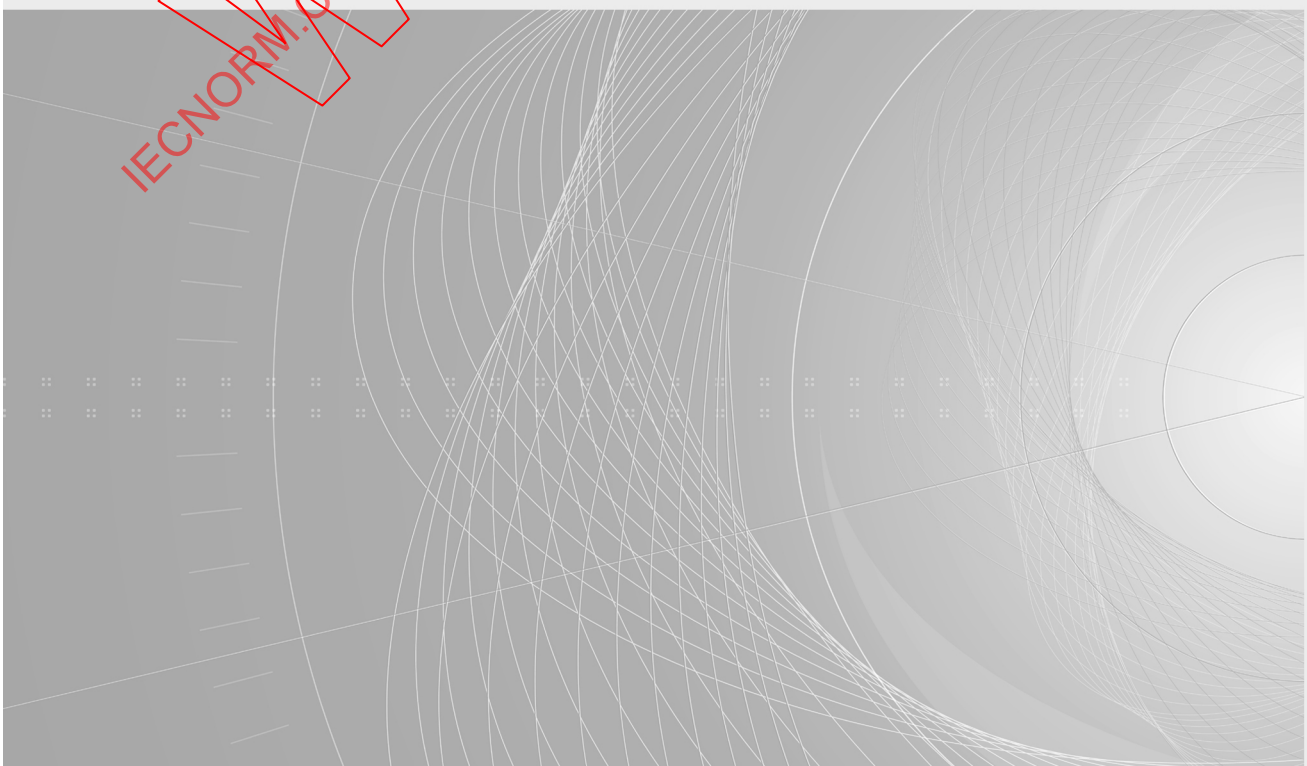
Edition 1.0 2010-09

PUBLICLY AVAILABLE SPECIFICATION

PRE-STANDARD

colour inside

Printed boards –
Part 14: Device embedded substrate – Terminology / reliability / design guide



IEC/PAS 62326-14:2010(E)

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

PRINTED BOARDS – Part 14: Device embedded substrate – Terminology / reliability / design guide

FOREWORD

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It is based on JPCA-EB01 (2009) 2nd edition. It is published as a double-logo PAS and JPCA.

The text of this PAS is based on the following document:

This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document

Draft PAS	Report on voting
91/893/PAS	91/910/RVD

Following publication of this PAS, which is a pre-standard publication, the technical committee or subcommittee concerned may transform it into an International Standard.

This PAS shall remain valid for an initial maximum period of 3 years starting from the publication date. The validity may be extended for a single period up to a maximum of 3 years, at the end of which it shall be published as another type of normative document, or shall be withdrawn.

A list of all the parts in the IEC 62326 series, under the general title *Printed boards*, can be found on the IEC website.

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PRINTED BOARDS – Part 14: Device embedded substrate – Terminology / reliability / design guide

1 Scope

This PAS is applicable to device embedded substrates fabricated by embedding discrete active and passive electronic devices into an inner layer of a substrate with electric connections by vias, conductor plating, conductive paste, and printing. The device embedded substrate may be used as a substrate to mount SMDs to form electronic circuits, as conductor and insulator layers may be formed after embedding electronic devices.

The purpose of this PAS is to obtain common understanding in design, fabrication and use of device embedded substrates in the industry.

This PAS describes the substrate embedding devices including but not limited to module, integrated passive device (IPD), microelectrochemical systems (MEMS), discrete component formed in the fabrication process of the electronic wiring board, and sheet form component. Figure 1 shows examples of device embedding in the fabrication process of the device embedded substrate. Active and passive devices are connected to each other by interlayer vias and/or conductor patterns. Insulating layers are formed using insulating materials with vias for the connection of inside conductor patterns to the conductor patterns formed on the surface(s) of the substrate. Figure 2 shows the substrate with connections using pads, and Figure 3 shows the board using via connections.

The insulating layer includes rigid and flexible insulating resins such as phenol resin, epoxy resin, polyimide resin and modified polyimide resin, which are reinforced with glass cloth, aramid cloth or paper, and resins without reinforcement. Interconnections to the input and output terminals to the embedded device and the surface conductor pattern include conventional interconnection of the terminals of the embedded device to an interconnecting land for SMD, and formation of terminals on the surface of an embedded device by copper plating or vias using conductive paste.

This PAS does not specify the fabrication process of device embedded substrates, via diameter/via land diameter, conductor width/conductor spacing nor conductor line density.

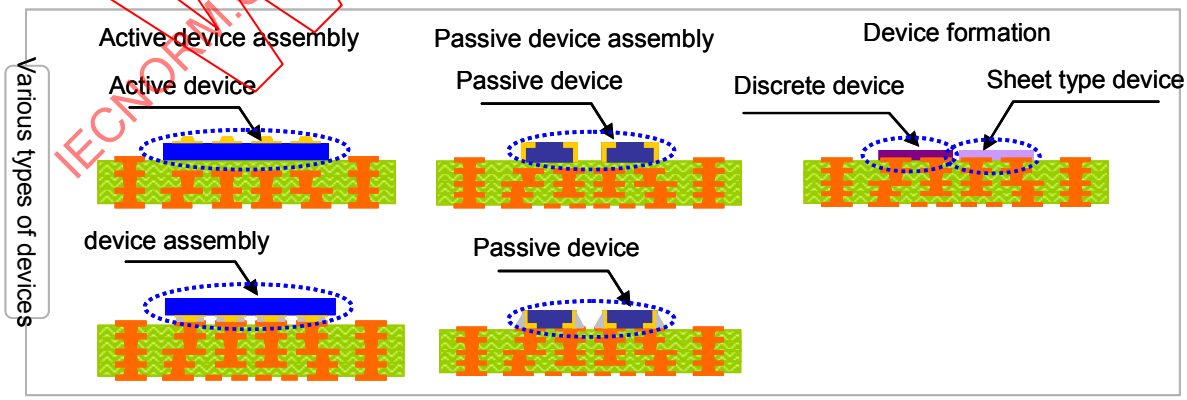


Figure 1 – Examples of device embedded substrate

2 Normative references

Void

3 General definitions

3.1 Technology of the device embedded substrate

There are two types of device embedded substrates: one type consists in embedding an active and/or passive discrete device on a base substrate and covering it with organic resin and the other consists in forming a device on a substrate and then covering it with organic resin. The device embedded substrate also includes composite type substrates which consist of mass produced inorganic ceramic including LTCC (low temperature co-fired ceramics) substrates (hereafter they are called just ceramics) on which passive devices are embedded as shown in Figure 4, and the other type as shown in Figure 5 where the ceramic substrate is used as a base on which active and passive devices are mounted and the entire body is covered by organic resin; details of inorganic ceramics are not specified in this document. Such a ceramic is treated just handled as a base of a device embedded module.

Classification of device embedding is given in Table 1. Active devices include bare die, wafer-level package (WLP), BGA, LGA, and QFN. Passive devices include chip component, complex chip component like an array and integrated passive device (IPD). Module and MEMS are embedded onto the substrate after packaging and moulding into module and MEMS. The component formed during substrate formation is not covered in this document but also included in Table 1. There are two types of formed passive component embedding, one is to form passive components using thick film or thick film technology on the base of a silicon or compound semiconductor and/or on the stacked chip at the wafer level or on package-on-package (PoP), and the other is to use a sheet-type passive device on an organic substrate first and then to embed the other devices.

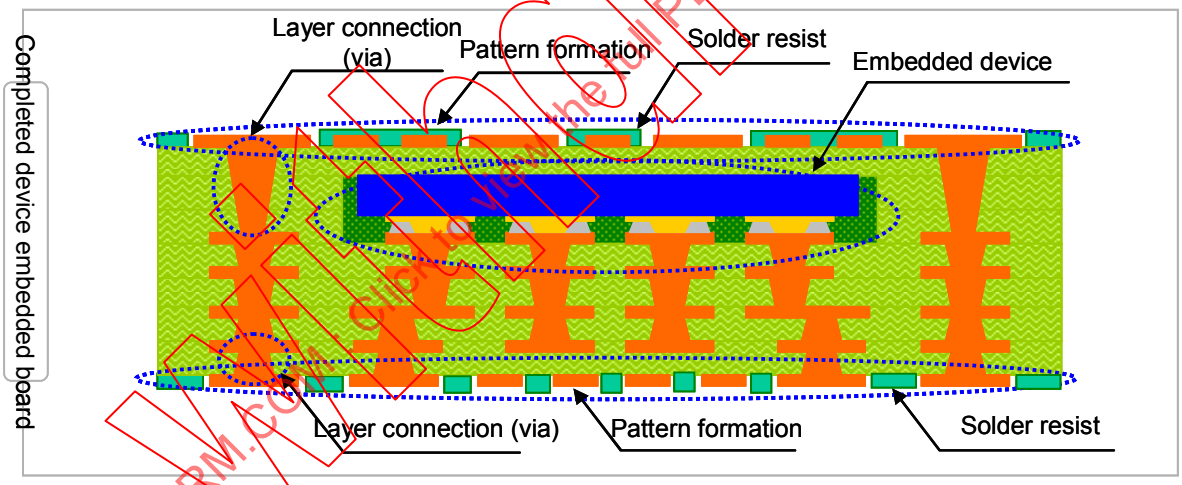


Figure 2 – Completed device embedded substrate (pad connection)

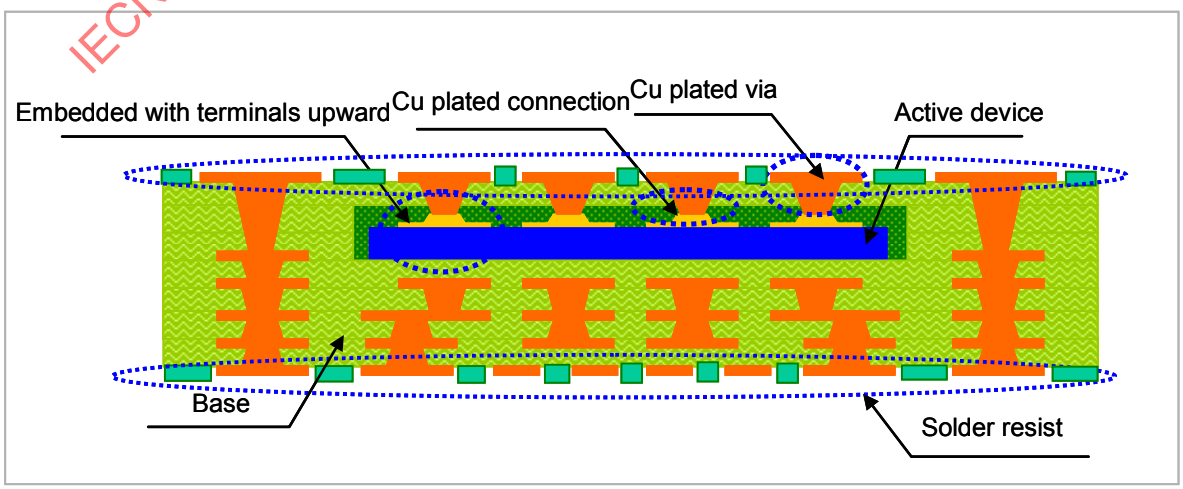


Figure 3 – Completed device embedded substrate (via connection)

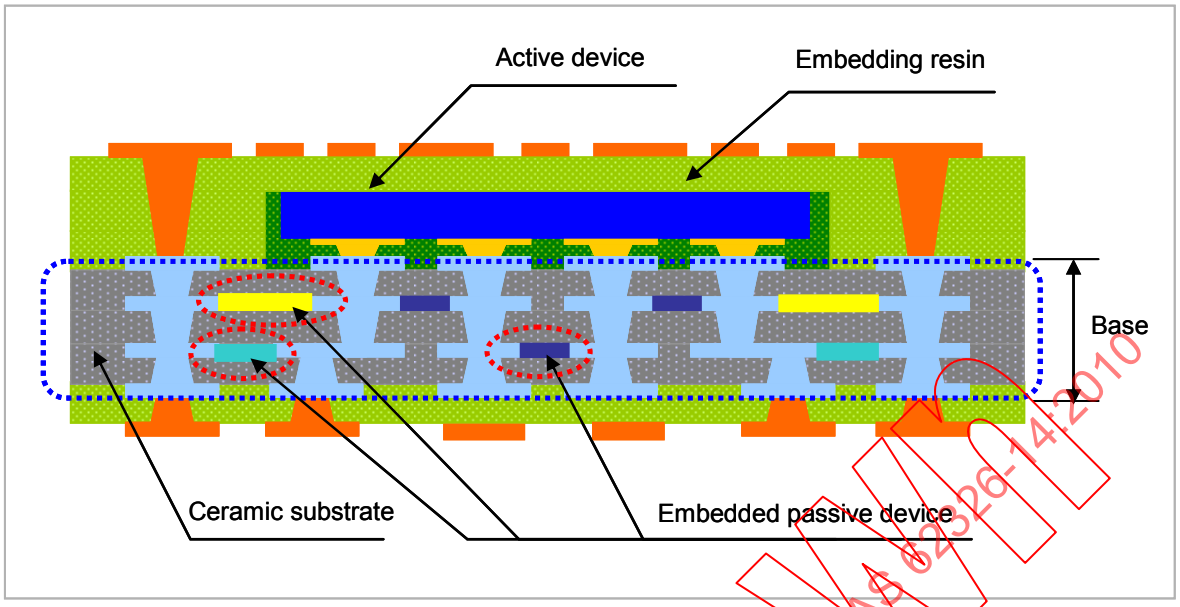


Figure 4 – Structure of a device embedded substrate using a passive device embedded substrate as a base and then a active and/or a passive device is mounted and then covered by resin (Pad connection type)

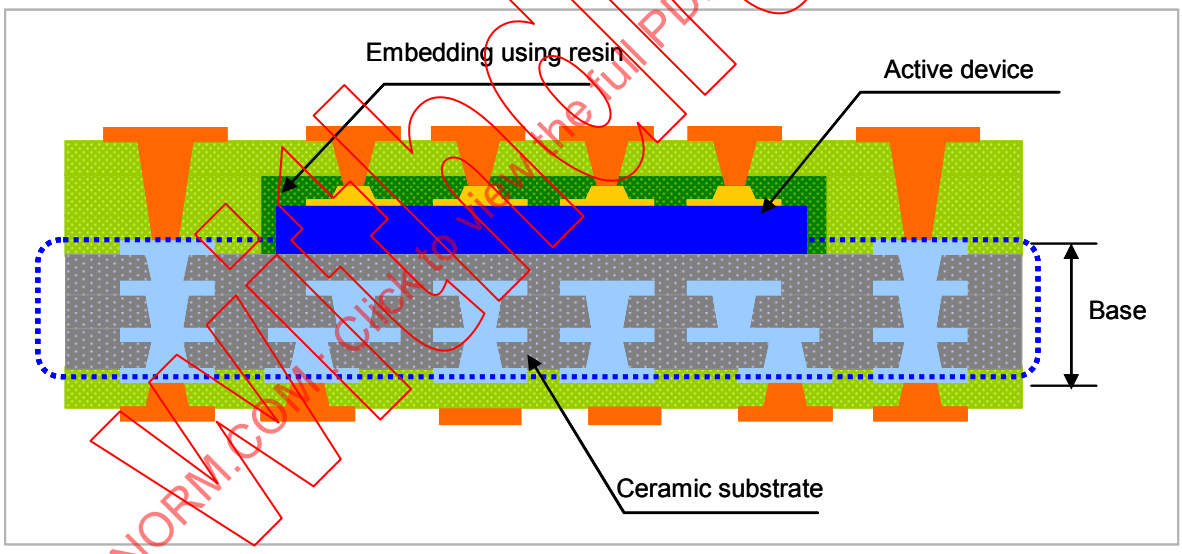


Figure 5 – Structure of a device embedded substrate using a ceramic board as the base (via connection type)

Table 1 – Classification of device embedding

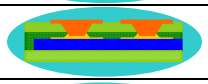
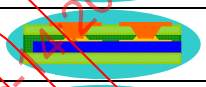
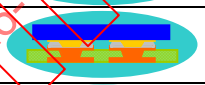
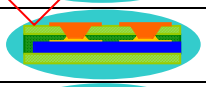
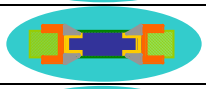
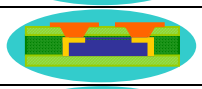
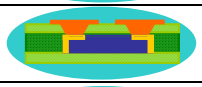
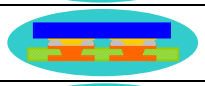
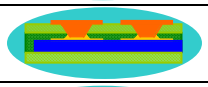
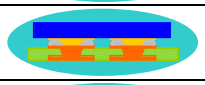
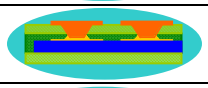
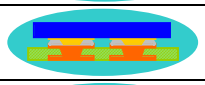
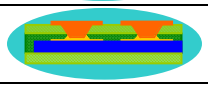
Classification	Item	Embedding	Device terminals	Bonding	Schematics
Active device	Bare die	Die bonding	Peripheral	Wire bonding	
		Flip chip bonding	Peripheral area array	Flip chip bonding	
		Die bonding	Peripheral area array	Via connection (plating, paste)	
	Wafer level package	Mounting	Peripheral area array	Soldering conductive paste	
		Die bonding	Peripheral area array	Via connection (plating, paste)	
	Package	Mounting	BGA, LGA, QFN	Soldering conductive paste	
		Mounting	BGA, LGA, QFN	Via connection (plating, paste)	
Passive device	Chip component	Mounting	Rectangular chip Rod type chip	Through hole	
		Mounting	Rectangular chip Rod type chip	Soldering conductive paste	
		Mounting	Rectangular chip	Via connection (plating, paste)	
	Module chip component	Mounting	Rectangular chip	Soldering conductive paste	
		Mounting	Rectangular chip	Via connection (plating, paste)	
	Integrated passive device	Mounting	IPD	Soldering conductive paste	
		Mounting	IPD	Via connection (plating, paste)	
Module	Packaging and moulding	Mounting	Arbitrary	Soldering conductive paste	
		Mounting	Arbitrary	Via connection (plating, paste)	
MEMS	Packaging and moulding	Mounting	Arbitrary	Soldering conductive paste	
		Mounting	Arbitrary	Via connection (plating, paste)	

Table 1 – Classification of device embedding *(continued)*

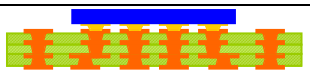
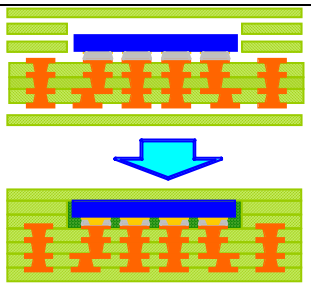
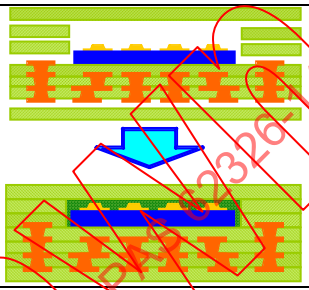
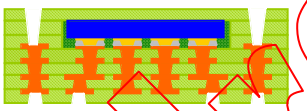
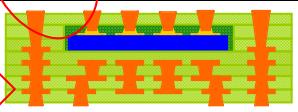
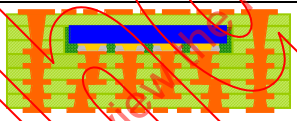
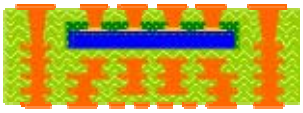
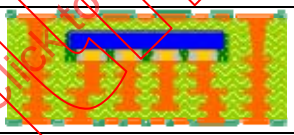
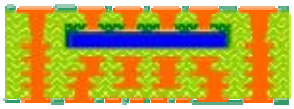
Classification	Item	Embedding	Device terminals	Bonding	Schematics
Active device	Formed	Thin film Sputtering	Silicon	Via connection (plating, paste)	
		Thick film Screen printing	Semiconducting polymer	Via connection (plating, paste)	
Passive device	Formed	Double through hole	Copper plating	Via connection (plating, paste)	
		Etching	Laminate material	Via connection (plating, paste)	
		Etching	Film	Via connection (plating, paste)	
		Screen printing	Polymer	Via connection (plating, paste)	
		Transfer	Ferromagnetic Ceramics	Via connection (plating, paste)	
		Lamination	Seeding	Via connection (plating, paste)	
		Spin coating	Polymer	Via connection (plating, paste)	

3.2 Substrate

Structures and fabrication processes of device embedded substrates are illustrated in Table 2. A base substrate is necessary for the device embedded substrate to embed active and passive devices. Most of the base substrates are multilayer substrates and build-up substrates, but an insulating resin board, insulating sheet, metal sheet or film carrier can certainly also be used. Table 2 shows the method to embed the active or passive device and then connect the device to the surface conductor by vias made of copper plating and conductive paste and checking items during the fabrication process.

This document, however, does not cover active devices formed on a silicon interposer, a compound semiconductor substrate or a printed wiring board and passive device (resistor, capacitor or inductor) but it does cover inductors formed together with a conductor pattern and capacitor in its structure.

Table 2 – Embedded device structure and fabrication process

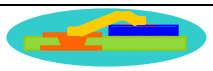
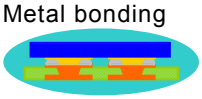
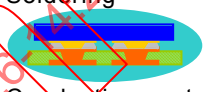
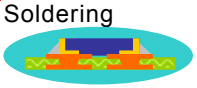
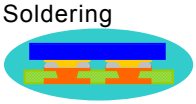
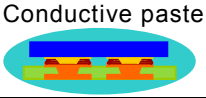
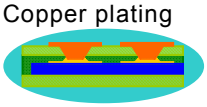
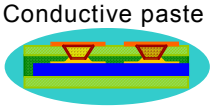
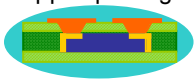
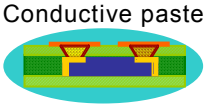
Process	Item	Structure		To check
		Pad bonding	Via connection	
1	Base			Opening, short
2	Mounting			Position accuracy
3	Pad bonding		—	Connection, conduction
4	Embedding			Microvoid Board thickness Flatness
5	Via hole			Hole position Terminal position Resistance to chemicals
6	Via hole	—		Thickness of Cu plating & conductive paste Micro void
7	Pattern formation (multi-layer)			Open, short
8	Surface treatment (solder mask, etc.)			Observation

3.3 Jisso mounting and interconnection

There are two types of terminal connections; one is to connect terminals of an embedded device to connecting pads formed on the base, and the other is to form connecting vias on the device after embedding. The device is connected to the pads on the base using conventional semiconductor and SMD mounting techniques and then the device is embedded. The device is connected to the conductor pattern in the second case after embedding by copper plating or conductive paste.

Both of the device mountings can be classified into die-bonding and mounting methods as shown in Table 3.

Table 3 – Jisso mounting and interconnection of the device embedded substrate

Jisso mounting		Device	Interconnection		Structure
			Process	Interconnection	
Pad bonding	Die bonding	Chip	Wire bonding	Wire melt-connection	
			Flip-chip bonding	Metal bonding Contact connection	Metal bonding  Contact 
	Mounting	Wafer level packaging (WLP)	Reflow Polymer bonding	Soldering Conductive paste	Soldering  Conductive paste 
		Package	Reflow Polymer bonding	Soldering Conductive paste	
		Rectangular chip	Reflow Polymer bonding	Soldering Conductive paste	Soldering  Conductive paste 
		Rod-type chip	Reflow Polymer bonding	Soldering Conductive paste	
		Module	Reflow Polymer bonding	Soldering Conductive paste	Soldering  Conductive paste 
		MEMS	Reflow Polymer bonding	Soldering Conductive paste	
Via bonding	Die bonding	Chip	Via connection	Copper plating Conductive paste	Copper plating  Conductive paste 
		Wafer level package (WLP)	Via connection	Copper plating Conductive paste	
	Mounting	Package	Via connection	Copper plating Conductive paste	
		Rectangular chip	Via connection	Copper plating Conductive paste	Copper plating  Conductive paste 
		Rod-type chip	Via connection	Copper plating Conductive paste	
		Module	Via connection	Copper plating Conductive paste	
		MEMS	Via connection	Copper plating Conductive paste	

NOTE The shape and surface treatment of the terminals of the embedding device should be agreed upon between the user and the supplier of the device.

3.4 Structure and terminology

3.4.1 General

Figure 6 shows each section of the device embedded substrate and its name. See JPCA-TD01-2008, Terms and definitions in electronic circuits, and JIS C 5603, Terms and definitions in printed wiring boards. The number of layers is counted after completion of the device embedding as L1, L2 ~ L6 (in case of 6 layers) from the top layer.

The structure of the device embedded substrate is illustrated by means of the structure of the build-up substrate. See JPCA-BU01–2007, Build-up wiring board (Terms and test methods). Figure 7 shows the typical structure of the base and Figure 8 the cavity structure. Other structures are shown in Figure 9 with the insulating base, in Figure 10 for the base using a conductive carrier or a metal sheet. Figure 11 shows the structure of the device embedded ceramics and Figure 12 shows the standard ceramic board as the wiring board base.

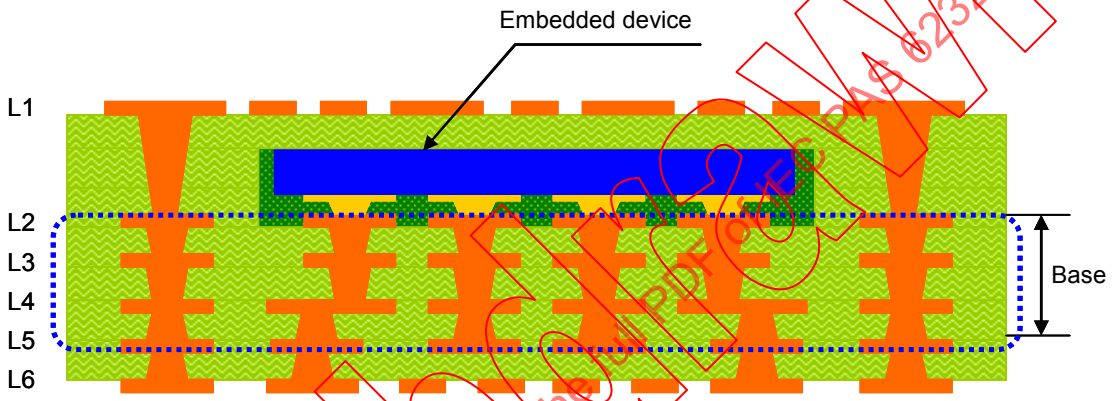


Figure 6 – Entire structure of device embedded substrate

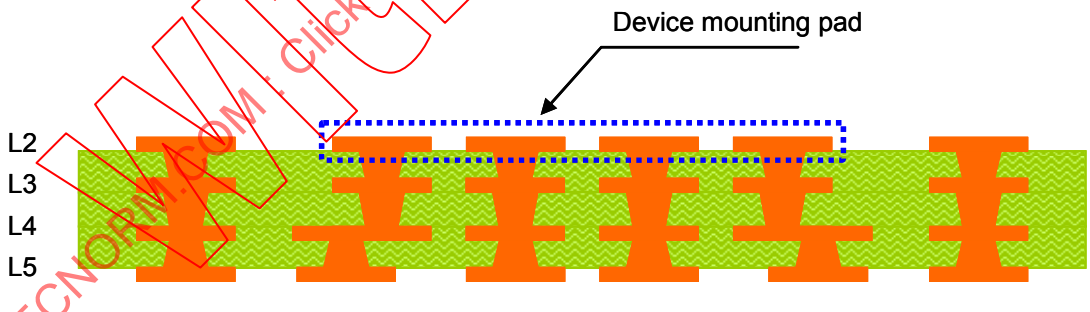


Figure 7 – Base (typical structure)

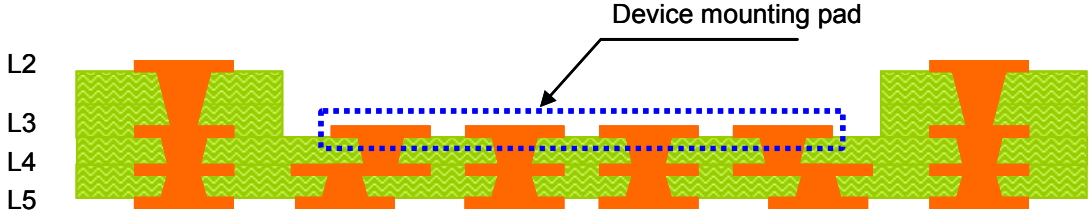
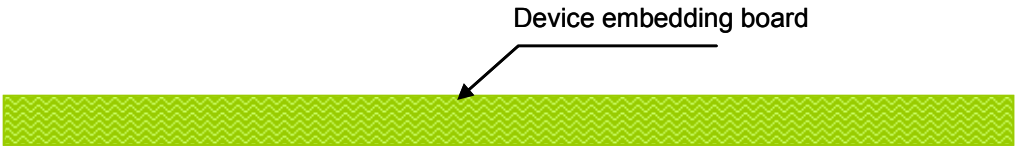


Figure 8 – Base (Cavity structure)



* Used for terminal connection in electronic circuit board

Figure 9 – Base (insulator)

Figure 10 – Base (conductive carrier – metal plate)

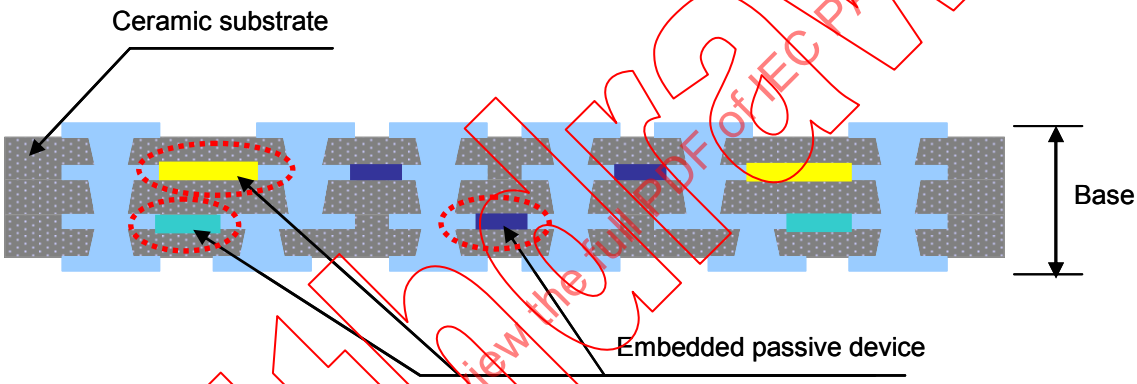


Figure 11 – Passive device embedded ceramic substrate used as a base

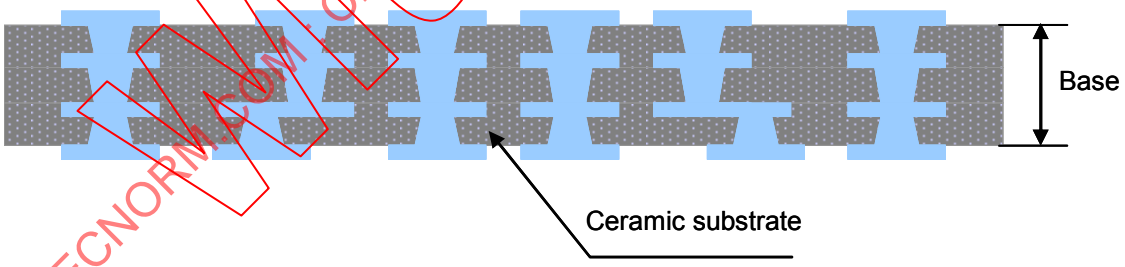


Figure 12 – Ceramic board used as base

Figure 13 to Figure 19 show various cases of device embedding in conventional mounting technique, electric connection after embedding various types of devices, embedding device over more than one layer, device embedding with resin base, and use of conductor layer and metal sheet/copper foil.

3.4.2 Device embedding by conventional process

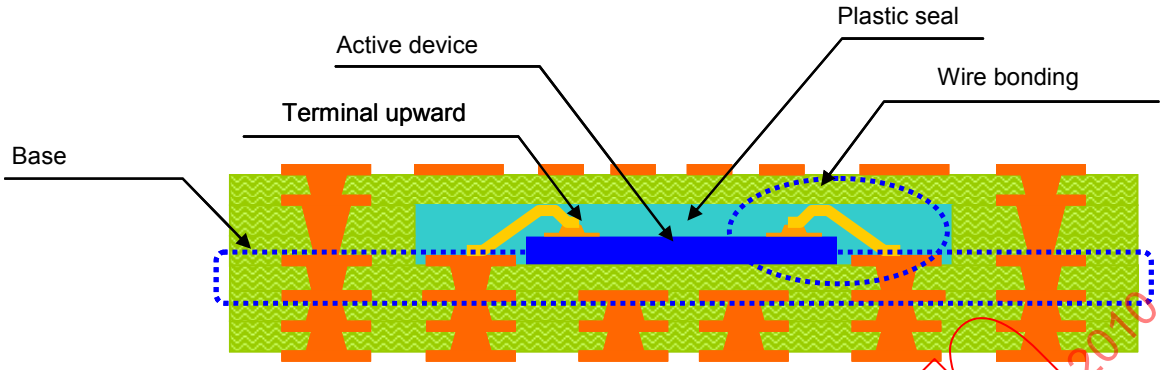


Figure 13a – Wire bonding connection and embedding of active device bear chip

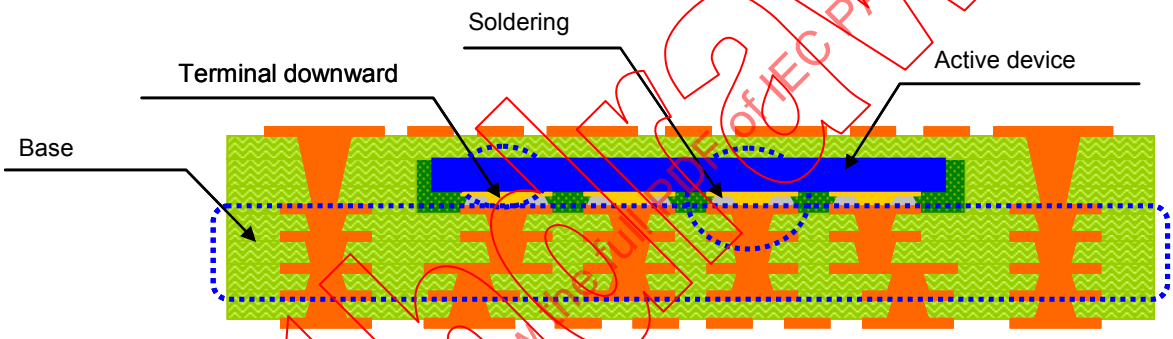


Figure 13b – Soldering connection and embedding of active device

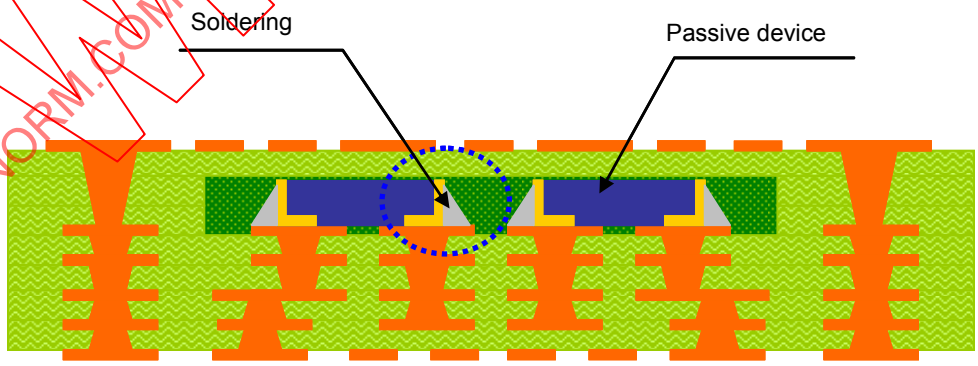


Figure 13c – Soldering connection of square type passive device

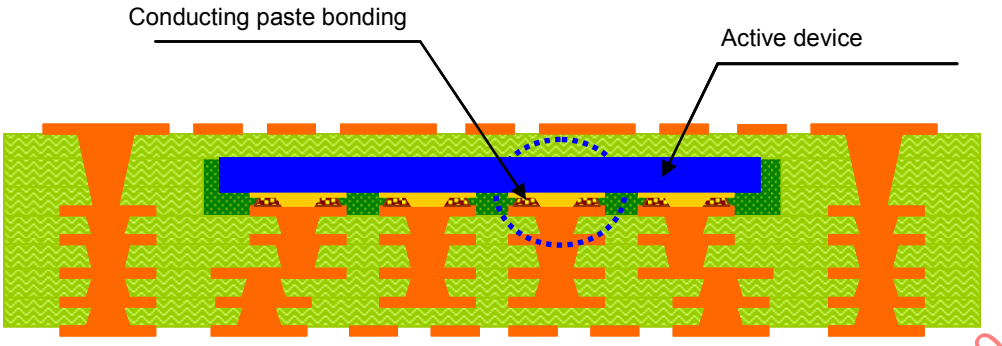


Figure 13d – Conductive resin connection and embedding of active device

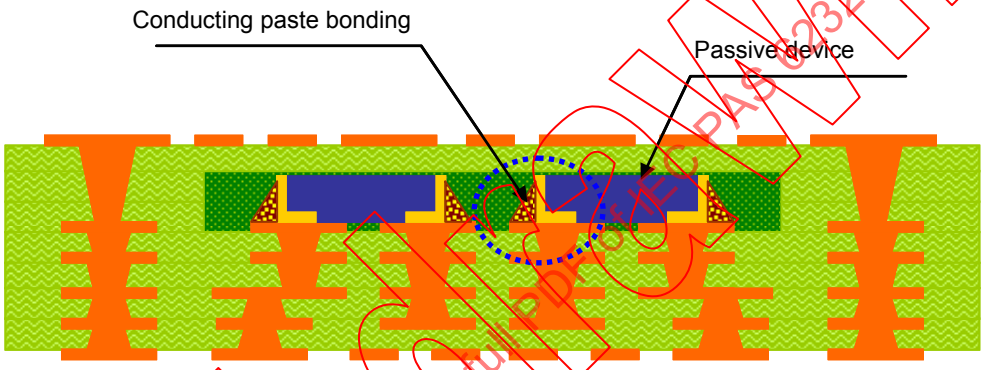


Figure 13e – Conductive resin connection and embedding of square type passive device

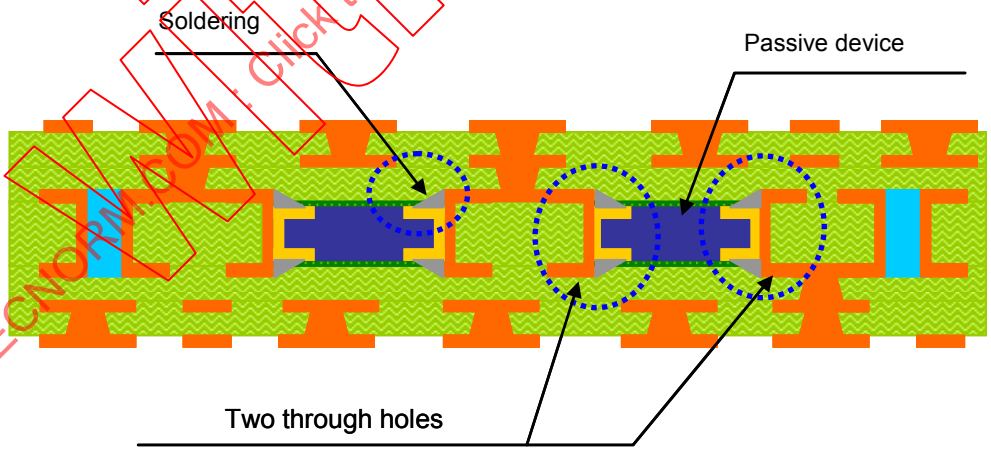


Figure 13f – Soldering connection into through hole and embedding of passive device

Figure 13 – Embedding of device by conventional methods

3.4.3 Electrical connection by vias after device embedding

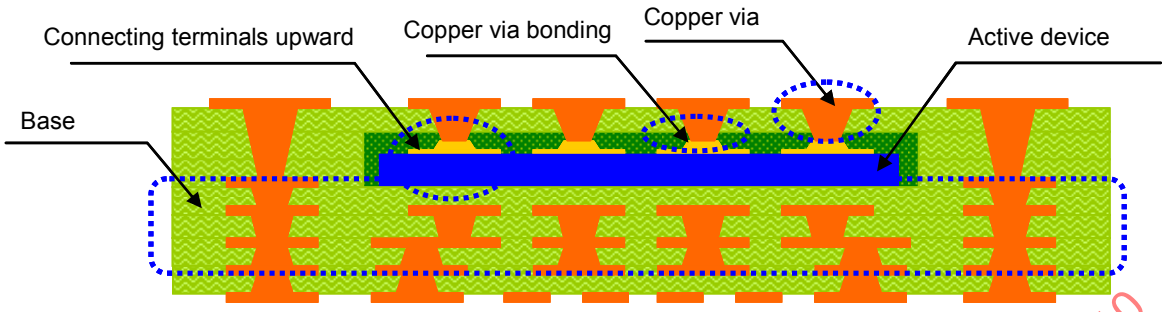


Figure 14a – Connection by Cu plating after embedding of active device

Figure 14b – Connection by Cu plating after embedding of square type passive device

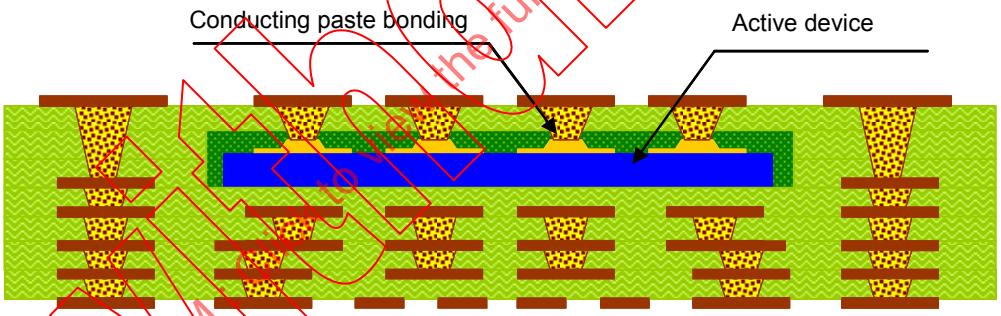


Figure 14c – Conductive paste connection after embedding of active device package

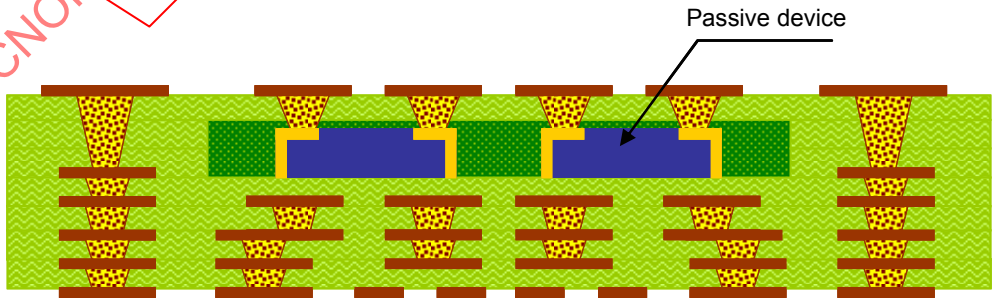


Figure 14d – Conductive paste connection after embedding of square type passive device chip

Figure 14 – Via connection after embedding

3.4.4 Embedding of various devices over multiple layers

3.4.4.1 Device embedded substrate of device embedding in multi-layers

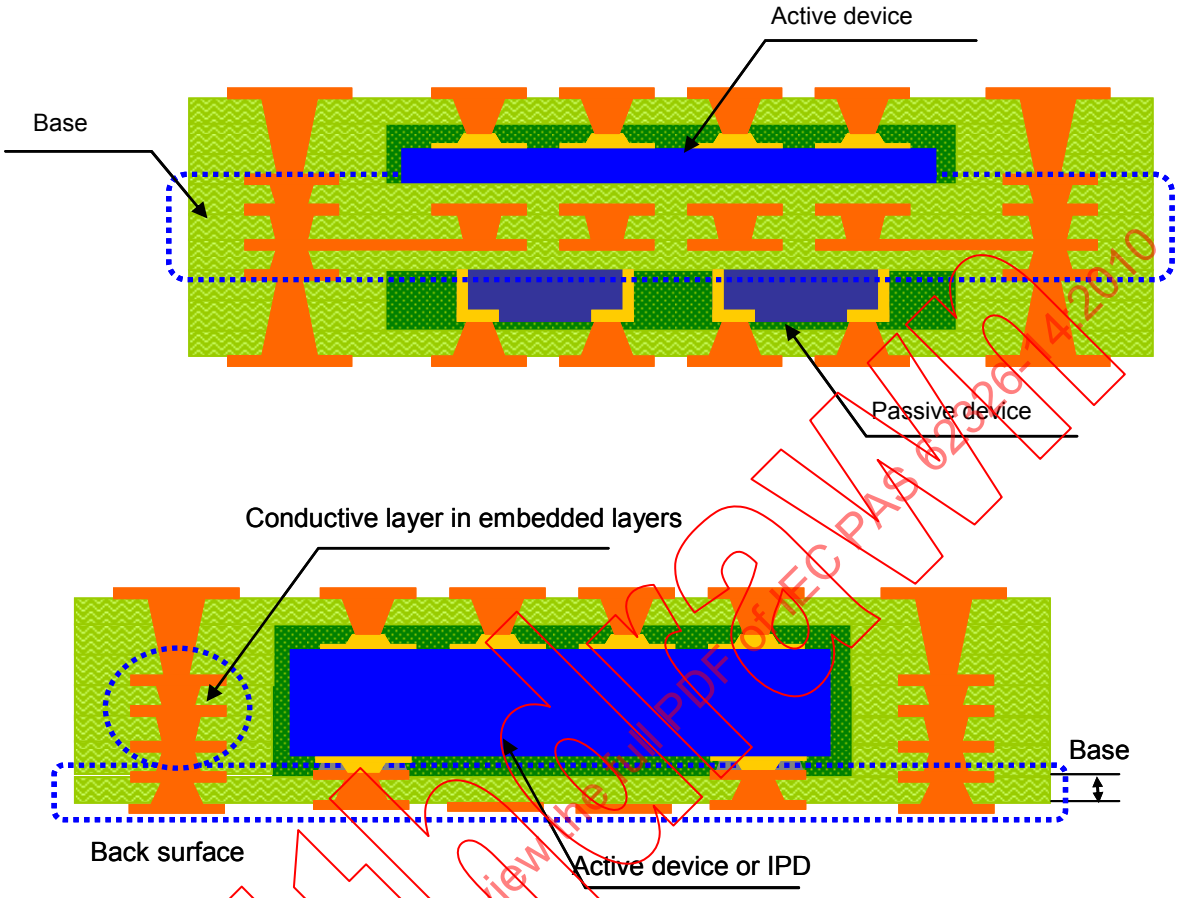


Figure 15 – Embedding of devices over multiple layers

3.4.4.2 Embedding of various devices onto resin base substrate

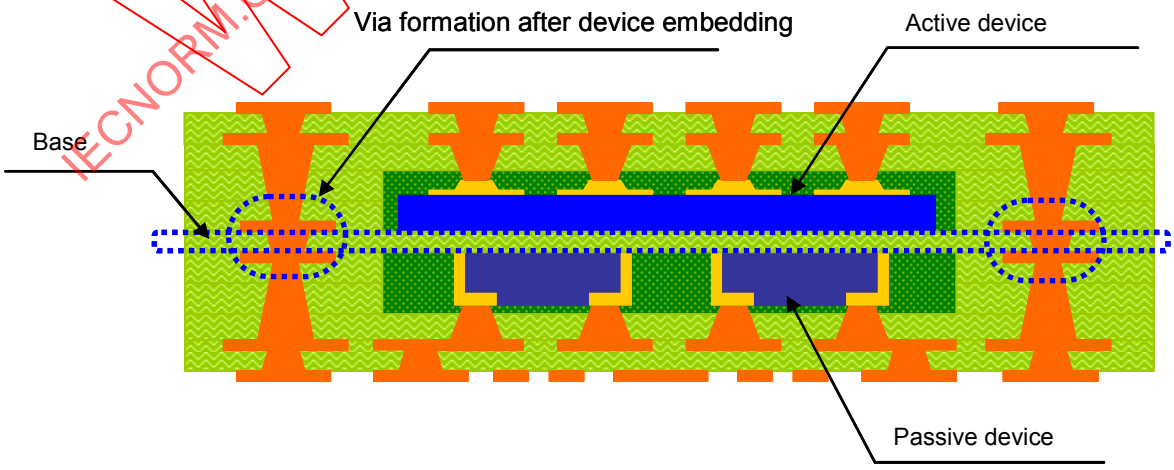


Figure 16 – Resin base substrate

3.4.4.3 Device embedding using conductor and metal sheet/copper foil base substrate

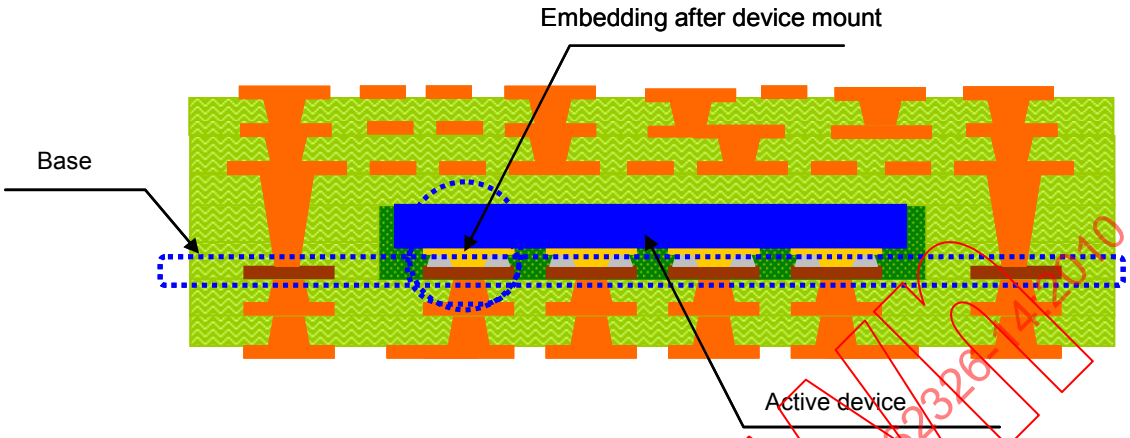


Figure 17 – Conductor and metal sheet/copper foil as the base substrate

3.4.4.4 Ceramic and resin composite device embedded substrate using passive device embedded ceramic substrates as the base

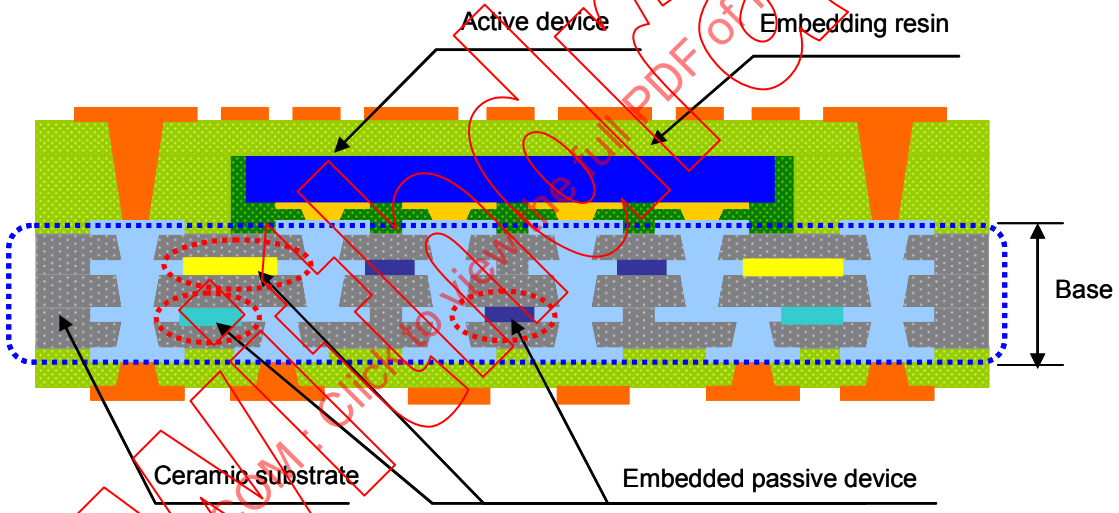


Figure 18 – Device embedded substrate using passive device embedded ceramic substrates as the base

3.4.4.5 Device embedded substrate using ceramic and LTCC substrates as the base (including ceramic and LTCC substrates which do not embed passive devices)

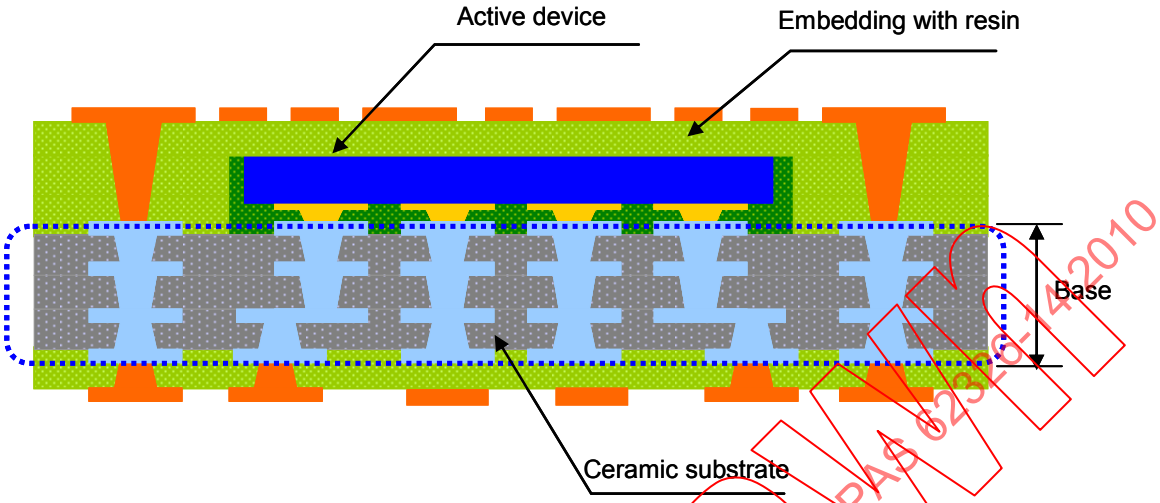


Figure 19 – Device embedded substrate using passive device embedded ceramic substrates as the base – second type

4 Test methods

4.1 General

The test methods for the un-embedded board are those for the board itself. The specifications and test methods for the embedded board are for the embedded board only and not for the embedded device. It is recommended to evaluate a TEG mounted board (test element group) to obtain assembly condition and library data for design. The TEG is less expensive than actual embedding semiconductor devices and can provide necessary technical data easily. Guarantee of reliability of a product shall be agreed between user and supplier. Embedding of device into board shall also be agreed upon between user and supplier basically based on the statement given in this document.

4.2 Structure of TEG (Test Equipment Group – Test vehicle)

A schematic diagram of TEG is shown in Figure 20 for the evaluation of the conductor pattern on the base of a board, the interconnection between the base and the test specimen and the conductor pattern on the board surface. The characteristics of the device embedded board and test equipment shall also be agreed between user and supplier.

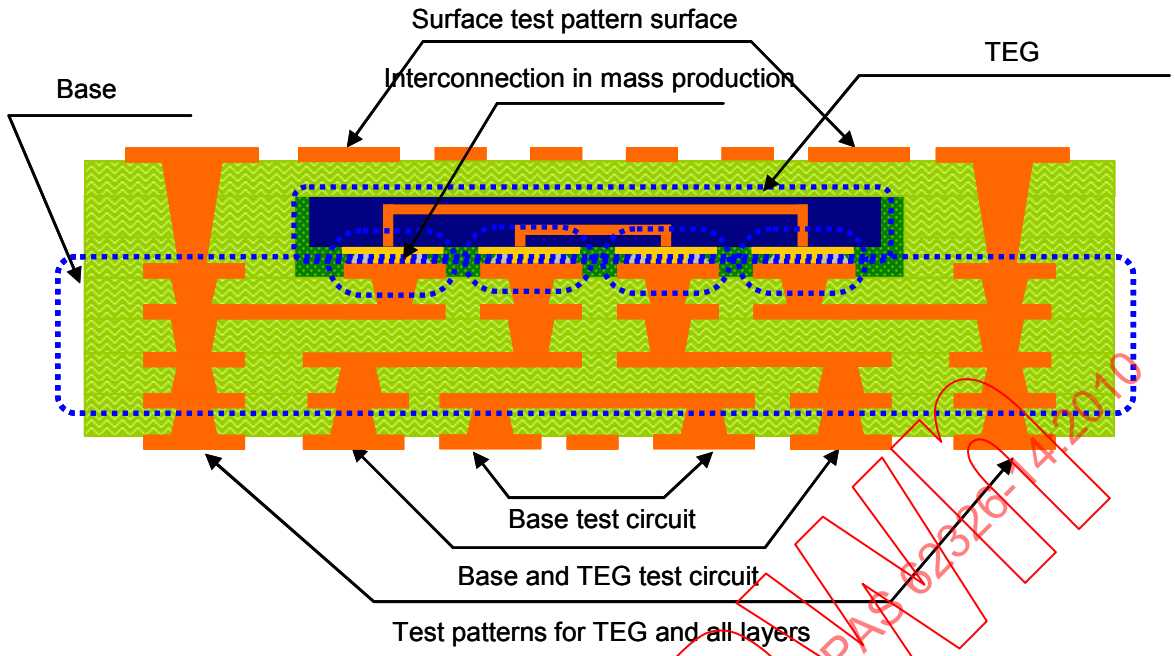


Figure 20 – Schematic diagram of test circuit

NOTE Test items, test methods, and test equipment are still under consideration in the standardization committee and there is a possibility that the description made in this document may be changed if necessary.

4.3 Test circuit

TEG, a dummy specimen of an embedding device, is embedded into board using the actual embedding condition; it is tested for the multilayer wiring patterns shown in Figure 21 similarly to the test of multilayer wiring board for interconnections between conductor pattern by means of through holes and/or vias using the Daisy chain pattern. It is recommended to use the circuit patterns made within the range of device embedding for the tests of inter-digital type capacitor, impedance, insulation and impurity migration as illustrated in Figure 22.

Size of test board, wiring specification of TEG and size as a replacement of embedding device, and wiring specification of the device embedding board shall be agreed between user and supplier.

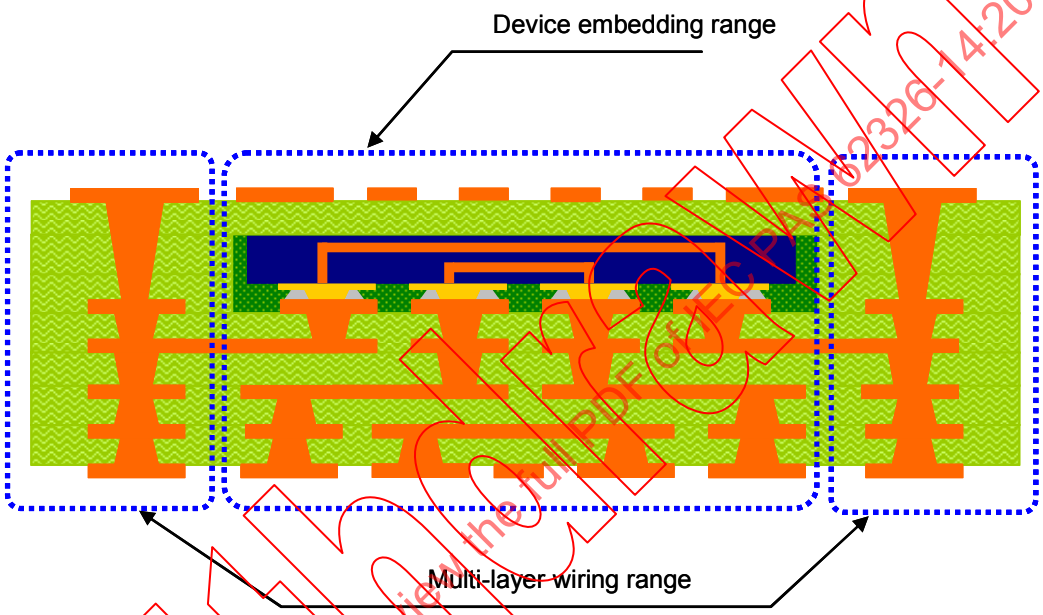


Figure 21 – Multilayer wiring patterns

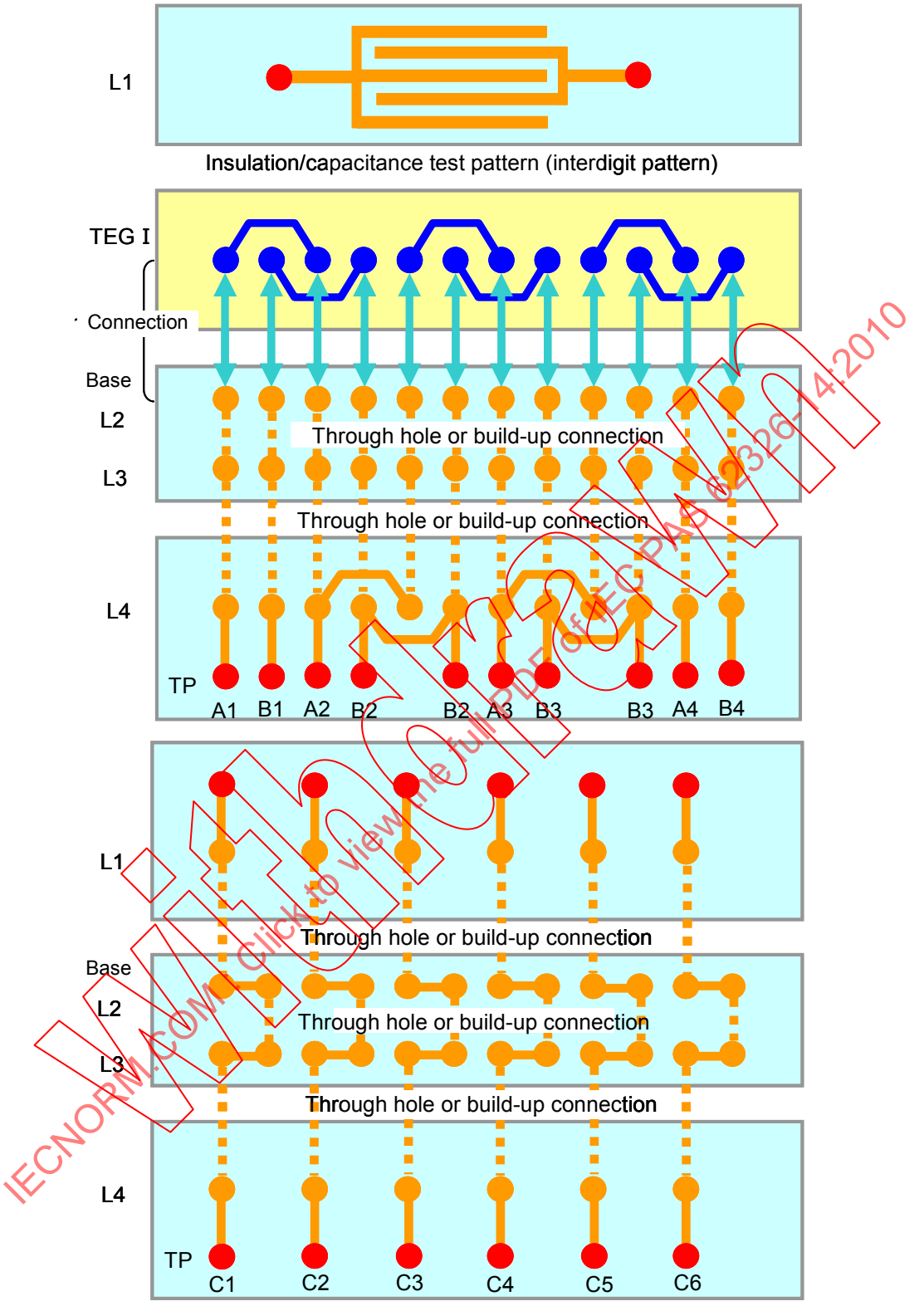


Figure 22 – Conceptual structure of test circuit, comb-type capacitor, detection pattern of impedance, insulation and migration

4.4 Test specimen (TEG) and example of test substrate

Figure 23 shows an example of specimen. It has a Daisy chain pattern in peripheral sections and interdigital capacitor, an impedance detection pattern and a bend detection pattern. Its die size is 10 mm x 10 mm and thickness is 0,15 mm. Electrode number is 316 with a pitch of 120 µm. Electrode size is 110 µm with an opening of 90 µm x 90 µm. Gold bump is used for connection. Figure 24 shows a test board. The conductor resistance (connection evaluation) test is made by the Daisy chain shown in the figure. Insulation resistance test is made using the pattern for evaluation of conductor resistance between conductors and the interdigital pattern shown in Figure 25.

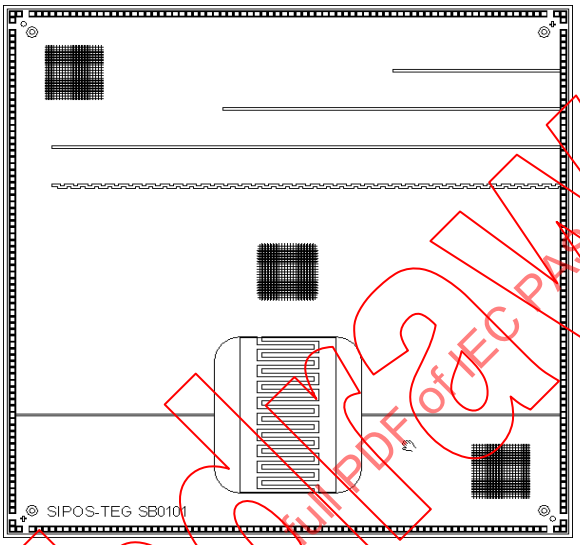


Figure 23 – Example of TEG

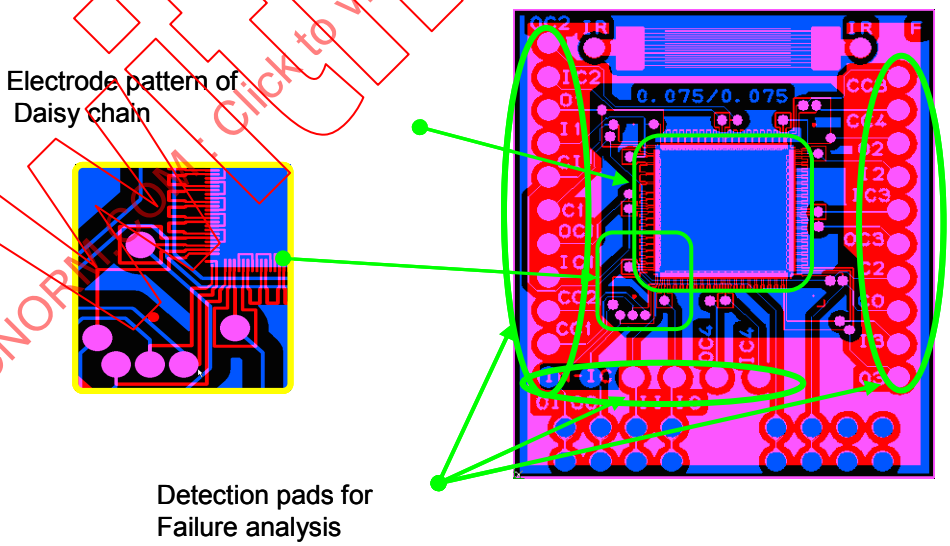


Figure 24 – Example of test circuit for connection evaluation

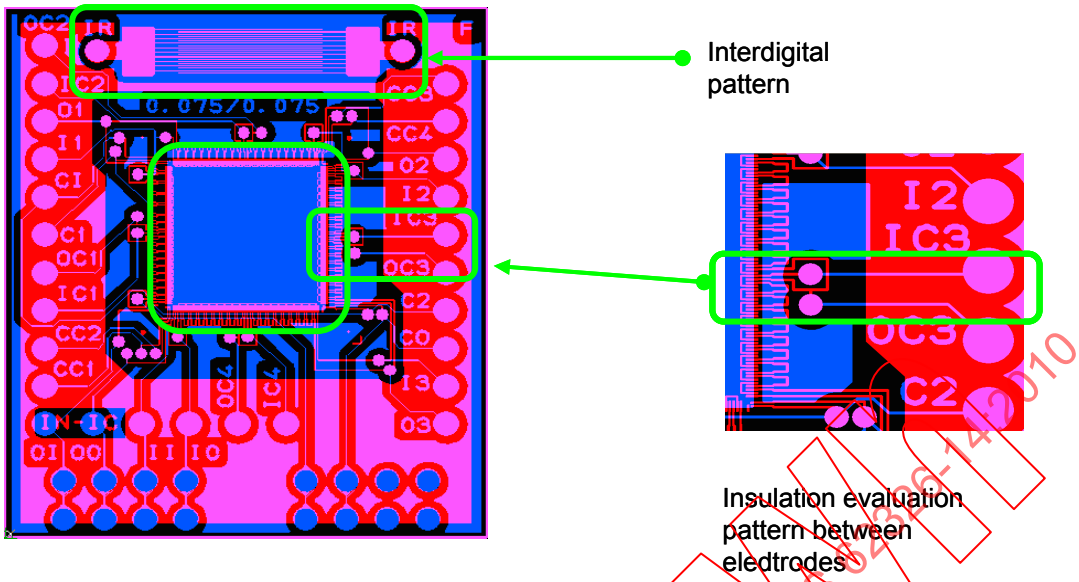


Figure 25 – Example of test circuit for insulation evaluation

5 Test items and test equipment

5.1 General

Evaluation of device embedded board is basically the same to that of electronic circuit board (printed wiring board and module substrate) but there are some new mechanical and electric test items.

Each test is performed using a specimen embedding the TEG as in actual device embedding using a Daisy chain pattern connection of the TEG and the substrate conductor pattern. It is recommended to use pads independently arranged at corners where the risk of failure is considered relatively high. Evaluation items and test methods are listed in Table 4.

5.2 Test for resistance of conductor

The test method for conduction is shown in Table 4.

Table 4 – Conduction test

Item		Specification	Test method (JIS C 5012)
Conduction (conductivity evaluation)	Inner conductor	To be agreed between user and supplier. Relations between resistance and conductor width, conductor thickness and conductor temperature is shown in Figure 26 for reference. Conductivity of Cu is taken as $\rho = 1{,}8 \times 10^{-6}$ Ω·cm.	As per 7.11 (conductor). Shape and dimension of specimen should be agreed between user and supplier. 1. Test method ・Daisy chain or resistance between specified two points. 2. Equipment ・4 terminal low resistance measurement equipment ・High/low temperature bath
	Outer conductor		As per 7.13 (inner layer connection)
	Plated through hole and via hole (copper plating or conductive paste)		Ad per 7.12 (plated through hole)
	Connection to embedded device	To be agreed between user and supplier.	Use TEG for embedding device test. Test for the connection to embedded device is under consideration.

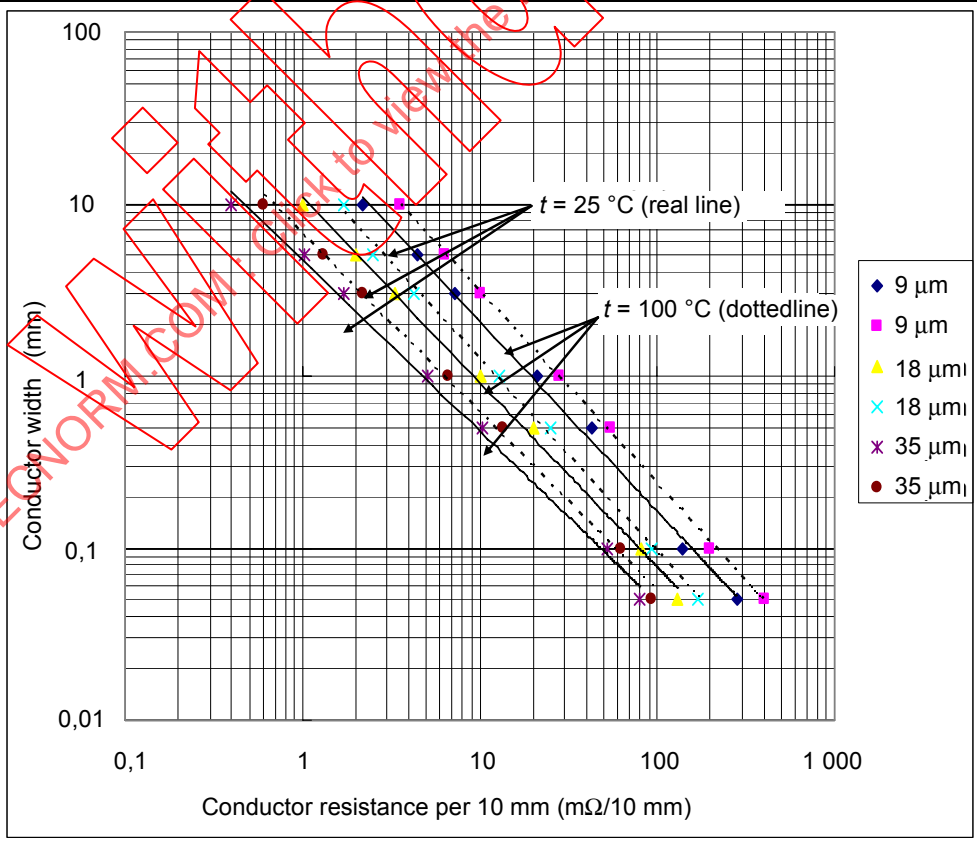


Figure 26 – Resistance per unit length of conductor pattern in relation with conductor width

5.3 Resistance to over current

The test method for resistance over current is shown in Table 5.

Table 5 – Resistance to over current and its test method

Item		Specification	Test method (JIS C 5012)
Resistance to overcurrent	Conductor	To be agreed between user and supplier	As per 7.2 (resistance to overcurrent of conductor)
	Plated through hole		As per 7.3 (resistance to overcurrent of plated through hole)
	Connection to embedded device	To be agreed between user and supplier The relation of conductor width, conductor thickness and temperature rise with current are shown in Figure 27.	Under consideration Use TEG in place of embedded device. The test for the embedded device is under consideration.

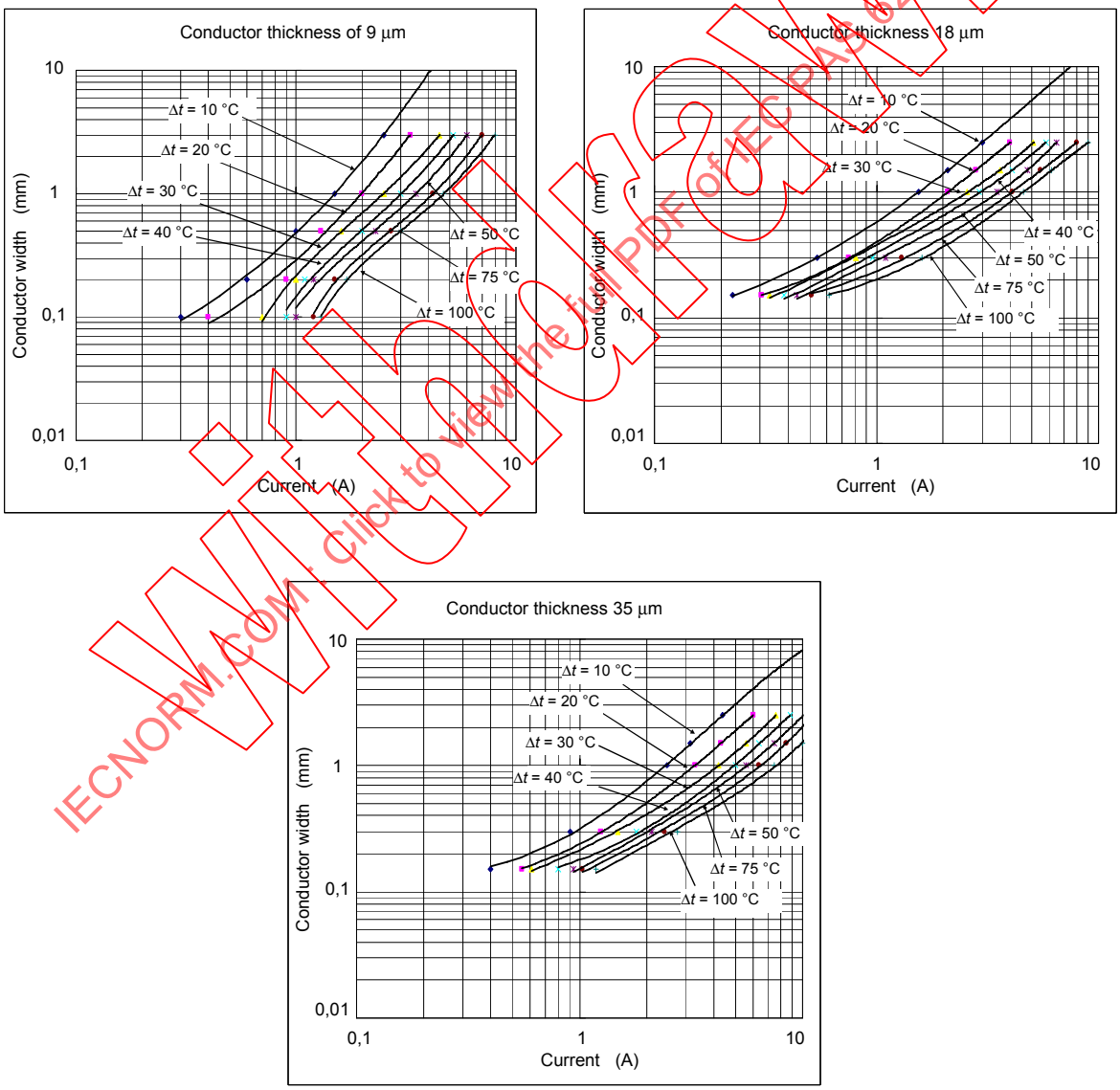


Figure 27 – The relation of conductor width, conductor thickness and temperature rise with current

5.4 Withstand voltage

The test method is shown in Table 6.

Table 6 – Withstand voltage and test method

<table>
<tr><th colspan="2">Item</th><th>Specification</th><th>Test method (JIS C 5012)</th></tr>
<tr><td rowspan="3">Withstand voltage</td><td>The same plane</td><td>There should be no mechanical damages, flush over, nor insulation damages.</td><td>As per 7.4 (surface withstand voltage)
The test voltage is chosen from the following table for both outer (with/without solder resist) and inner layers
<table>
<tr><th>Minimum conductor gap
mm</th><th>Test voltage
V</th></tr>
<tr><td>0,05≦ < 0,10</td><td>50</td></tr>
<tr><td>0,10≦ < 0,13</td><td>100</td></tr>
<tr><td>0,13≦ < 0,25</td><td>200</td></tr>
<tr><td>0,25≦ < 0,40</td><td>350</td></tr>
<tr><td>0,40≦</td><td>500</td></tr>
</table>
NOTE Solder resist is not considered as coating.</td></tr>
<tr><td>Interlayer</td><td>There should be no mechanical damages, flush over, nor insulation damages.</td><td>As per 7.5 (Interlayer withstand voltage)
The test voltage is chosen from the following table.
<table>
<tr><th>Interlayer distance
mm</th><th>Test voltage
V</th></tr>
<tr><td>0,05≦ < 0,08</td><td>250</td></tr>
<tr><td>0,08≦ < 0,20</td><td>500</td></tr>
<tr><td>0,02≦</td><td>1 000</td></tr>
</table></td></tr>
<tr><td>Connection to embedded device</td><td>To be agreed between user and supplier</td><td>Use TEG for embedding device test.
Test for the connection to embedded device is under consideration.</td></tr>
</table>

5.5 Insulation resistance

Test of the insulation resistance is made by using the electrode evaluation pattern made by combination of base and embedding board as in the case of the conductor resistance test. Test items are shown in Table 7.

Table 7 – Test methods of insulation resistance

<table>
<tr><th colspan="3">Item</th><th>Specification</th><th>Test method (JIS C 5012)</th></tr>
<tr><td rowspan="5">Insulation resistance</td><td rowspan="3">The same plane</td><td>Normal</td><td>Insulation resistance should be more than the value shown below.
<table><tr><th>Minimum conductor gap
mm</th><th>Insulation resistance
Ω</th></tr><tr><td>0,05≦ < 0,13</td><td>1×10^8</td></tr><tr><td>0,13≦</td><td>5×10^8</td></tr></table></td><td>See Annex A of this specification.
See Annex B of this specification.</td></tr>
<tr><td>Resistance to humidity (temperature-humidity cycle)
Resistance to humidity (steady state)</td><td>Insulation resistance should be more than the value shown below.
<table><tr><th>Minimum insulation thickness
mm</th><th>Insulation resistance
Ω</th></tr><tr><td>0,05≦ < 0,20</td><td>1×10^8</td></tr><tr><td>0,20≦</td><td>5×10^8</td></tr></table></td><td>Test should be made as in the case of normal condition.</td></tr>
<tr><td>Inter-layer</td><td>Normal</td><td>Insulation resistance should be more than the value shown below.
<table><tr><th>Minimum insulation thickness
mm</th><th>Insulation resistance
Ω</th></tr><tr><td>0,05≦ < 0,20</td><td>1×10^{10}</td></tr><tr><td>0,20≦</td><td>5×10^{10}</td></tr></table></td><td>See Annex C of this specification. The test voltage is given below.
<table><tr><th>Minimum insulation thickness</th><th>Test voltage
V</th></tr><tr><td>0,05≦ < 0,20</td><td>50</td></tr><tr><td>0,05≦ < 0,20</td><td>100</td></tr><tr><td>0,20≦</td><td>500</td></tr></table></td></tr>
<tr><td>Humidity (temperature-humidity cycle)
Humidity (steady state)</td><td>Insulation resistance should be more than the value shown below.
<table><tr><th>Minimum insulation thickness
mm</th><th>Insulation resistance
Ω</th></tr><tr><td>0,05≦ < 0,13</td><td>1×10^{10}</td></tr><tr><td>0,13≦</td><td>5×10^{10}</td></tr></table></td><td>Test condition is the same as in the case of steady state condition.
Test should be made after leaving the specimen at room temperature for 1 h.</td></tr>
<tr><td>Terminals of embedded device</td><td>Normal
Humidity (temperature-humidity cycle)
Humidity (steady state)</td><td>To be agreed between user and supplier.</td><td>Use TEG for embedded device.
Test for the interconnection of terminals of embedded device is under consideration.</td></tr>
</table>

5.6 Peeling strength of conductor

Test method and requirement for the peeling strength of conductor are shown in Table 8.

Table 8 – Peeling strength of conductor and test method

Item	Specification	Test method (JIS C 5012)
Peeling strength of conductor	Peeling strength of conductor should be agreed between use and supplier. Unit: kN/m Item: Glass cloth epoxy resin CCL (FR-4) (Cu foil thickness: 18 µm) Specification: 0,98 (for reference)	Test method should be agreed between user and supplier based on 8.1 (Peeling strength of conductor).

5.7 Pull-off strength of plated through hole

Test method and requirement for the pull-off strength of plated through hole are shown in Table 9.

Table 9 – Pull-off strength of plated through hole and test method

Item	Specification	Test method (JIS C 5012)
Pull-off strength of footprint	Pull-off strength of footprint should be agreed between user and supplier. NOTE Pull-off strength of Glass cloth epoxy resin CCL multilayer board should be larger than 39,2N/2mm.	As per 8.4 (pull-off strength of footprint)

5.8 Adhesivity of plated film

Adhesivity of plated film and test method are shown in Table 10.

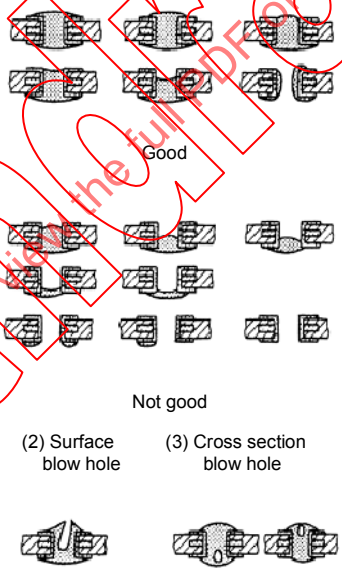
Table 10 – Adhesivity of plated film and test method

Item	Characteristics	Test method (JIS C 5012)
Adhesivity of plated film	There should not be any residue plated film on the tape beside plating overhang.	As per 8.5 (adhesivity of plated film)

5.9 Solderability

Solderability and its test method are shown in Table 11.

Table 11 – Solderability and test method

Item		Specification	Test method (JIS C 5012)
Solderability	Footprint	There should be no solder sputter on all the footprint.	As per 10.3 (Solderability test). The maximum soldering temperature is 260 °C and soldering time is 3 s max. for flow soldering, or use the temperature profile given in Annex Figure 6 for "Temperature change in reflow furnace (for reference). Use JIS C 5012, 6.2, Microsectioning when soldered junction is observed by microsectioning.
	Through hole	Solderability of device assembly holes should be clearly soldered as illustrated in the following illustration (1). There is not specification for the soldered connection of the inner layer conductor and the holes for power supply and/or ground layers which require a wide soldered area. Observable blow-holes (blow of gas contained in solder as illustrated in assembly hole (illustration 2) and the blow holes observable by microsectioning (illustration 3) should be less than 1 % of all the holes. Soldering of vias should be agreed between user and supplier. (1) Soldered shape  Good Not good (2) Surface blow hole (3) Cross section blow hole	
	Soldering of embedded device	To be agreed between user and supplier.	Soldering test of embedded device is under consideration.

5.10 Thermal shock (vapour phase cold heat cycle)

Specification and test method for thermal shock (vapour phase cold heat cycle) are shown in Table 12.

Table 12 – Characteristics and test method for thermal shock

<table>
<tr><th colspan="2">Item</th><th>Specification</th><th>Test method (JIS C 5012)</th></tr>
<tr><td rowspan="2">Thermal shock (vapour phase cold heat cycle)</td><td>Plated through hole connection

Plated via connection</td><td>Change of connection resistance after test of plated through hole, via connection, or conduction resistance of inner layer should be less than 20 % of the initial value.

No floating or peeling of conductor, through hole land or assembly pad should be observed.

There should be no delamination.

Measling and crazing should satisfy specification in 5.7.3 (defects in lamination).

Observation of specimen by microsectioning after test should satisfy specification of 6.1.2 (observation after thermal shock test).

Solder resist and marking should satisfy the values given below.

<table><tr><th>Item</th><th>Specification</th></tr><tr><td>Solder resist</td><td>No colour change, no floating, and no blister</td></tr><tr><td>Marking</td><td>Should be legible</td></tr></table></td><td>As per 9.2 (thermal shock – low and high temperature)

Specimen is a daisy chain connection of a minimum of 100 holes formed at a specified section of PWB, test coupon, or combined pattern similar to the combined test pattern (D pattern given in Annex Figure 21 or 22).

Use condition 2 in Table 4 for test temperature cycle and the number of cycles given below as the specimen thickness may affect the test result.

Cycle number<table><tr><th>Specimen thickness mm</th><th>Number of cycles</th></tr><tr><td>Less than 1,6</td><td>100</td></tr><tr><td>Above 1,6</td><td>To be agreed between user and supplier</td></tr></table>Resistance change $\triangle R/R$ (%) is obtained from the following equation:

$\triangle R/R$ (%) = (W_2 – W_1)/ W_1 x 100

where

W_1 = initial resistance

W_2 = resistance after the test</td></tr>
<tr><td>Connection to embedded device</td><td>To be agreed between user and supplier</td><td>Use TEG for embedding device test.

Test for the connection to embedded device is under consideration.</td></tr>
</table>

5.11 Thermal shock (high temperature)

Specification and test method for thermal shock are shown in Table 13.

Table 13 – Specification and test method for thermal shock

<table>
<tr><th colspan="2">Item</th><th>Specification</th><th>Test method (JIS C 5012)</th></tr>
<tr><td>Thermal shock (high temperature)</td><td>Plate through hole connection

Plated via connection</td><td>Change of connection resistance after test of plated through hole, via connection, or conduction resistance of inner layer should be less than 20 % of the initial value.

No floating or peeling of conductor, through hole land or assembly pad should be observed.

There should be no delamination.

Measling and crazing should satisfy specification in 5.7.3 (defects in lamination).

Observation of specimen by microsectioning after test should satisfy specification of 6.1.2 (observation after thermal shock test).

Solder resist and marking should satisfy the values given below.

<table><tr><th colspan="2">Item</th><th>Specification</th></tr><tr><td></td><td>Solder resist</td><td>No colour change, no floating, and no blister</td></tr><tr><td></td><td>Marking</td><td>Should be legible</td></tr></table></td><td>As per 9.3 (thermal shock – high temperature).

Specimen is formed at a specified section of PWB, test coupon, or combined pattern similar to the combined test pattern (D pattern given in Annex Figure 21 or 22).

Use test temperature cycle and the number of cycles given below as the specimen thickness may affect the test result.

Number of cycles
<table><tr><th>Specimen thickness
mm</th><th>Number of cycles</th></tr><tr><td>1,6</td><td>10</td></tr><tr><td>1,6≦ < 2,4</td><td>5</td></tr><tr><td>2,4≦</td><td>To be agreed between user and supplier</td></tr></table></td></tr>
<tr><td></td><td>Connection to embedded device</td><td>To be agreed between user and supplier</td><td>Use TEG for embedding device test.

Test for the connection to embedded device is under consideration.</td></tr>
</table>

5.12 Flammability

Flammability specification and test method are shown in Table 14.

Table 14 – Flammability specification and test method

Item		Specification	Test method (JIS C 5012)
Flammability	Insulation layer Solder resist Marking	Flammability should conform the requirement of flammability grade.	In conformity to UL 94.
	Embedded device	Flammability of embedding device should conform that of the device itself.	

5.13 Bow and twist

Specification and test method for bow and twist are shown in Table 15.

Table 15 – Specification and test method for bow and twist

<table>
<tr><th colspan="2">Item</th><th>Specification</th><th>Test method (JIS C 5012)</th></tr>
<tr><td rowspan="2">Bow and twist</td><td>Completed device embedded board (applicable to board thickness of over 0,8 mm)</td><td>Bow and twist should satisfy the following values.
For board thickness of less than 0,8 mm, bow and twist should be agreed between user and supplier.
<table>
<tr><th rowspan="2">Item</th><th colspan="2">Length of longer side （L）</th></tr>
<tr><th>100 mm</th><th>100 mm ≦</th></tr>
<tr><td>Bend</td><td>0,8 mm</td><td>For length exceeding 100 mm, bend should be less than the value given below
0,8 mm +
(L - 100) × 0,007</td></tr>
<tr><td>Twist</td><td>1,0 mm</td><td>For length exceeding 100 mm, twist should be less than the value given below
1,0 mm +
(L - 100) × 0,01</td></tr>
</table></td><td>As per 6.3.9 (flatness)</td></tr>
<tr><td>Connection to embedded device</td><td>To be agreed between user and supplier</td><td>Use TEG for embedding device test.
Test for the connection to embedded device is under consideration.</td></tr>
</table>

5.14 Migration

Specification and test method for migration are given in Table 16.

Table 16 – Specification and test method for migration

<table>
<tr><th colspan="2">Item</th><th>Specification</th><th>Test method (JIS C 5012)</th></tr>
<tr><td rowspan="2">Migration</td><td>Between conductor pattern</td><td>Migration should satisfy the resistance given below
<table><tr><th>Item</th><th>Specification</th></tr><tr><td>Migration</td><td>$1 \times 10^8\ \Omega \leqq$</td></tr></table>Measurement should be made after leaving the specimen for 1 h at room temperature.</td><td>Standard test condition is given here for reference.
Specimen
Comb pattern made on board with the minimum conductor gap on the board used.
Temperature/relative humidity
40°C/90%, 60°C/90% or 85°C/85%
Standard applied voltage
D C 5 V, 10 V, 15 V, 25 V
Time: 250 h, 500 h, 1 000 h</td></tr>
<tr><td>Between embedded device terminals and conductor pattern</td><td>To be agreed between user and supplier</td><td>Use TEG for embedding device test.
Test for the connection to embedded device is under consideration.</td></tr>
</table>

The other tests for mechanical stress given below are under consideration:

a) vibration (steady state, shock)
b) vibration at high temperature (steady state, shock)
c) drop test
d) bend
e) torsion
f) Tg (as is, in operation)
g)Tg (vibration, resonance, shock)

6 Indication, packaging and storage

6.1 Indication relative to the product should be agreed between user and supplier; however, the following subjects should be included.

a) Product name or product number

b) Name of manufacturer or its mark

c) Date of production

6.2 Packaging of the product should be agreed between user and supplier; however, the following subjects should be included.

a) Product name or product number

b) Number of product in a package

c) Date of production

d) Name of manufacturer or its mark

6.3 Package and storage

6.3.1 Packaging: The packaging should be made not to damage product and to avoid the effect of moisture.

6.3.2 Storage: The product should be stored where the effect of moisture can be avoided.

7 Design guide

7.1 General

The design guide of device embedded substrate is essentially the same as the design guide of various electronics circuit boards. The design guide stated here for device embedded substrate is basically the thorough understanding of circuit design, structure design, board design, board manufacturing, jisso (assembly processes) and tests of products. In this design guide are specified the names of constructions and structures of device embedded substrates, structures and restrictions imposed to device embedded bases, conditions of device embedding, and fabrication conditions of electronics circuit boards using device embedded substrates. Details of manufacturing conditions and reliability assurance of products are to be agreed between supplier and user.

7.2 Structure of device embedded substrate

7.2.1 General

The name of each part of a device embedded substrate is specified in this section to assist the engineers in avoiding technical misunderstanding in relevant sectors of the industry.

7.2.2 Specification of the front and back surfaces of a device embedded substrate

The definition of the front and back surfaces of a device embedded substrate basically depends on the number of devices mounted on the surface of the substrate as shown in Figure 28. The surface with more components mounted on one face than on the other is defined as the front surface. In the case of mounting a substrate on a printed wiring board (mother board), the surface connection of the substrate to the wiring board is defined as the back surface even in a case with a larger number of input/output terminals (pads) (see Figure 29). In this case the front and back surfaces are agreed between user and supplier, the agreement is the surface definition of priority different from the definition stated here.

a) Complete device embedded substrate structure

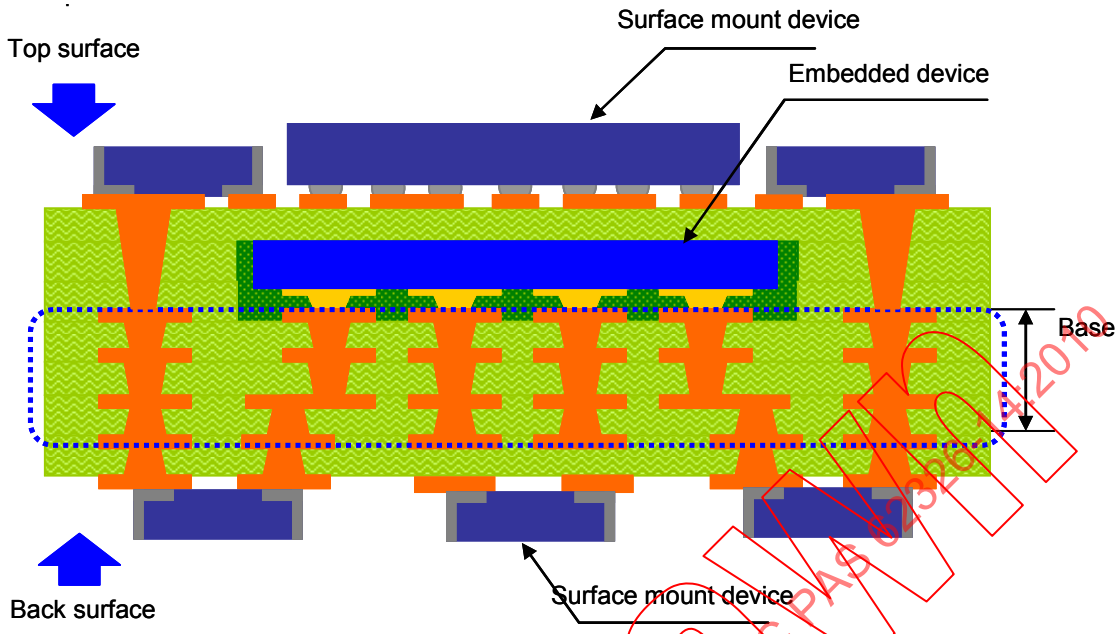


Figure 28 – Definition of front and back surfaces of a device embedded substrate

b) Device embedded substrate mounted on PWB (mother board)

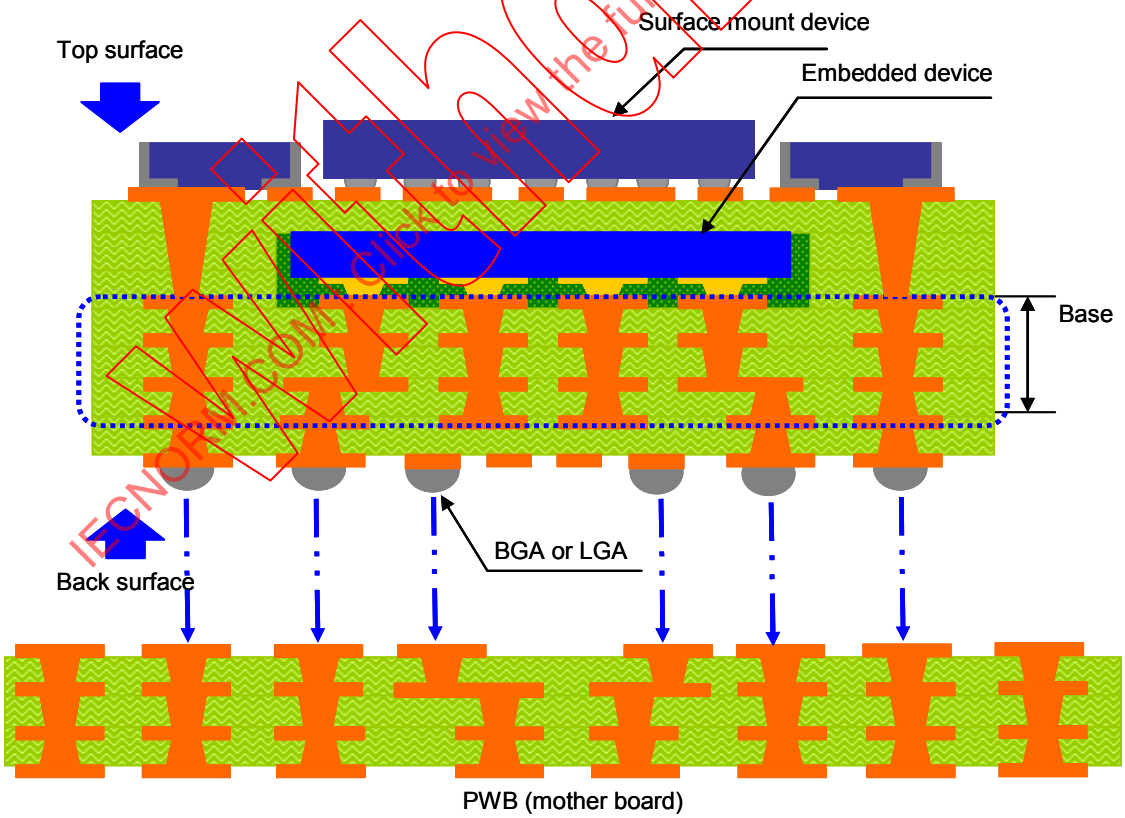


Figure 29 – Definition of front and back surfaces of a device embedded substrate – substrate mounted on a mother board

7.2.3 Definition of layers of a device embedded substrate

Layers of a multi-layer device embedded substrate is defined as the layer containing a conductive layer as one layer and defined as L1, L2, ~ L5, L6 (in the case of 6 layers) from the front surface of the substrate (see Figure 30).

In the case where the number of layers of the terminals of the embedded devices and the number of conductor layers are not the same as is the case in the via connection structure, virtual layers are specified to clarify the structure of a device embedded substrate, conductor pattern design, and the positions of embedded devices in substrate manufacturing and assembly processes.

Supplementary names for layers are added in the virtual layers to the layers as an exception to which to die bond or to mount the device to the layer. The front layer faces upward. The surface is upward (U) when terminals face upward and, downward when terminals face downward (D). Two orders of numbers are assigned to express the cases where multiple devices and/or connection terminals exist on the same single layer. The left side number expresses the connecting layer and the right side number expresses the layer number of the embedded devices. In the case of multiple layers, the number is assigned as 1 and 2 from the upper side and 1 and 2 from bottom for down side supplementary layers (see Figures 32 and 33).

EXAMPLES： Die bonding or mounting layer＝L2
Direction of connection terminals (L1 is upward)＝U
Connection layer (left side)＝1
Number of devices in a layer=2
Number of embedded devices (first layer of the same position) ＝1 （may be omitted for only 1）
(second layer of the same position)＝2 （may be omitted for only 1）
EXAMPLES: x x x x L2-U11 (upper side), x x x x L2-U12 (Lower side)

NOTE x x x x is the device number or the device mark.

a) Names of layers in pad connection

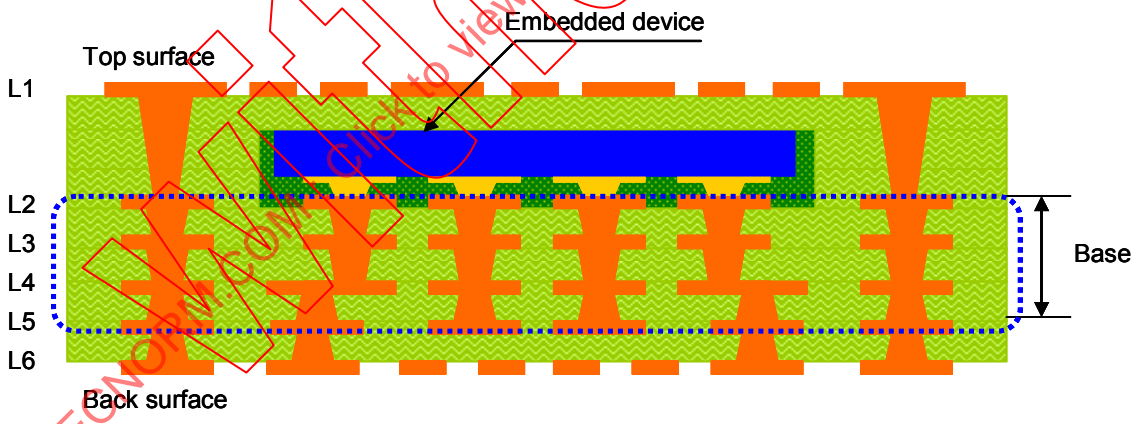


Figure 30 – Definition of layers of a pad-connection substrate

b) Remarks on positioning of terminals

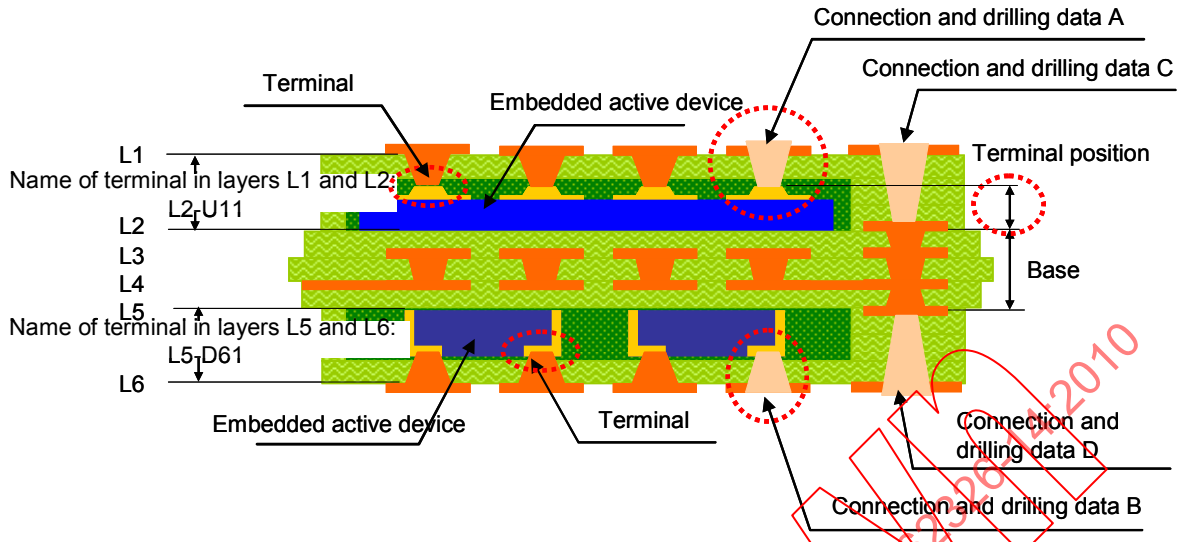


Figure 31 – Illustration of virtual layers

Note added in proof

The virtual layers are necessary to identify the interconnection layers (position) in substrate design for the case the position(s) of interconnection terminals of embedded devices is different from the position of a conductor layer when the position of a conductor layer is used as the reference of positions in an embedded substrate. In a production process, there may be no conductor layer at the terminal position(s). Basic number of layers may be 6 but virtual layer(s) may be required to identify the terminal positions. A virtual layer may be handled as a virtual conductor layer in pattern design and specify the interconnection position. Interconnection data and hole drilling data, A and B, are specified for the terminal connections of an embedded device and interconnection data and hole drilling data, C and D, are specified to the connections to L2 and L5 layers (in the case of this example). The virtual layer may be omitted when the position of terminals of an embedding device and that of a conductor layer is the same as in the case of via connection.

c) Names of layers in via connections (terminals in between layers)

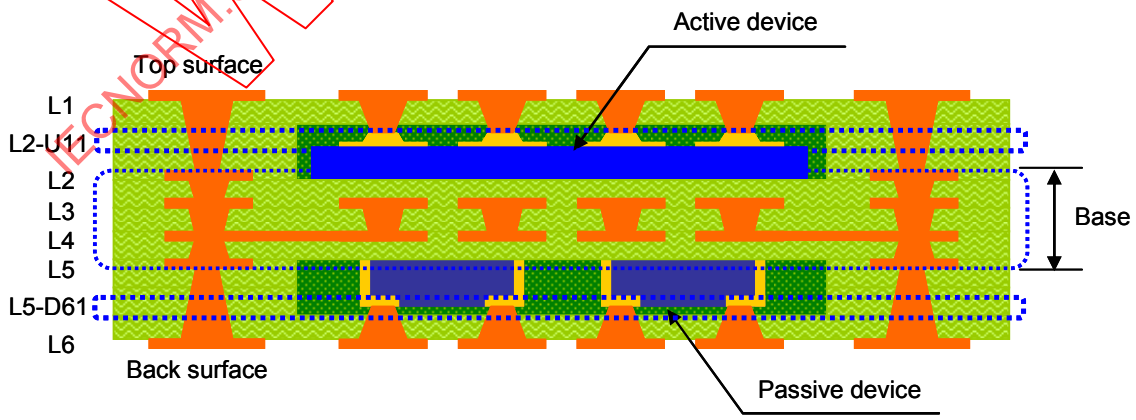


Figure 32 – Layer names in the via interconnection (I)

x x x x - L2-U11 L2: Device is embedded in L2 (2nd layer).

U: Terminals are connected upward.
11: Connections of single embedded device at L1

x x x x - L5-D61 L5: Device is embedded in L5 (5th layer).
D: Terminals are connected downward.
61: Connection of single embedded device at L6

d) Names of layers in via connection (devices are stacked in 2 or more layers)

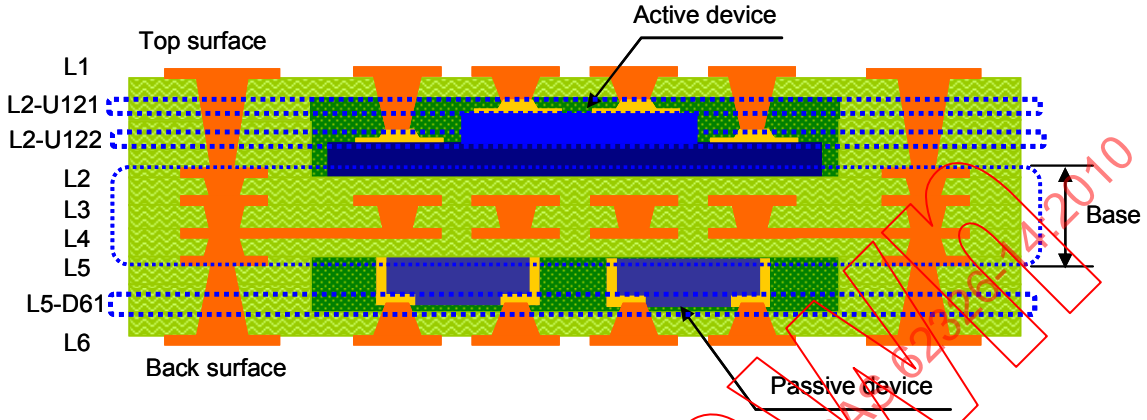


Figure 33 – Layer names in the via interconnection (II)

x x x x - L2-U121 L2: Device is embedded in L2 (2nd layer)
U: Terminals are connected upward.
121: Connections of two embedded devices at L1

x x x x – L2-U122 L2: Device is embedded in L2 (2nd layer).
U: Terminals are connected upward.
122: Connection of two embedded devices at L1

e) Names of layers in via connection (devices are embedded in more than 2 layers)

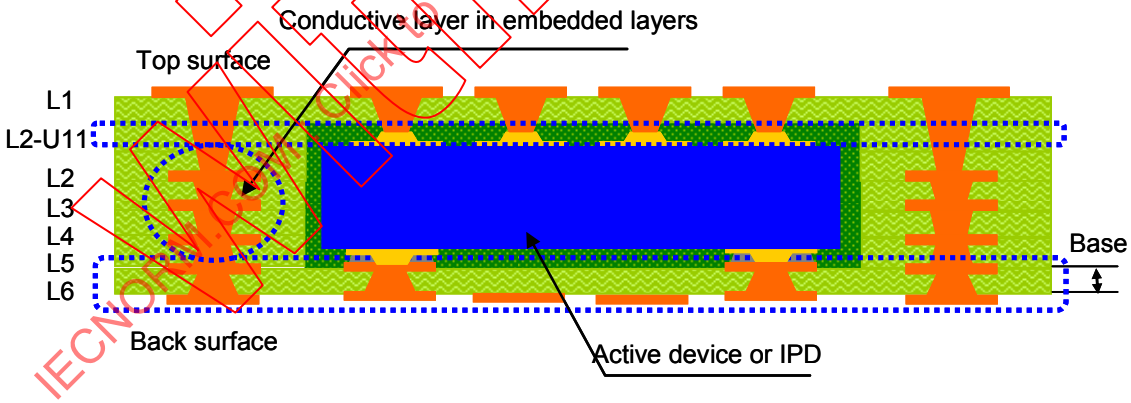


Figure 34 – Layer names in via connection (III)

Table 17 shows examples of layer names shown in Figures 31 to 34.

Table 17 – Layer names of device embedding substrate

Exam-ple	Embedding device				Embedding device and interconnection					
	Device	Hyphen	Terminal No./name	Hyphen	Embed-ding	Hyphen	Terminal direction	Connec-ting layer	No. of devices in a layer	
									Num-ber	Layer
Figure 31	Active device	-	A12	-	L2	-	U	1	1	Omit
	Passive device	-	1	-	L5	-	D	6	1	Omit
Figure 32	Active device	-	A13	-	L2	-	U	1	1	Omit
	Passive device	-	2	-	L5	-	D	6	1	Omit
Figure 33	Active device	-	A13	-	L2	-	U	1	2	1
	IPD	-	4	-	L2	-	U	1	2	2
	Capacitor	-	+	-	L5	-	D	6	1	Omit
Figure 34	IPD, etc.	-	12	-	L2	-	U	1	1	Omit
		-	B1	-	L6		D	6	1	Omit

NOTE Device information is necessary in embedding substrate design.

Example of device information indication: the device is indicated as 'Active device-A12-L2-U11' in the case of Figure 31.

7.2.4 Definitions of insulation layer thickness, conductor spacing and distance between electrode and conductor spacing (hereafter called “electrode”) at a terminal

The insulation layer thickness and the distance between each conductive layer are defined in reference to the position of each layer.

1) The insulation layer thickness is defined as the layer separating the conductor layers. The thickness is not the thickness of each layer to be laminated but the thickness of the actual insulation layer of the substrate.
2) The conductor distance is defined as the distance between the conductors formed on one layer.
3) The distance between the electrode and the conductor is the thickness of the insulator in between the terminals of the embedding device and the conductor layer to be connected.
4) The following terms are used to indicate each distance.

(1) Insulation layer thickness	DG1 (Dielectric gap)
(2) Distance between conductor layers	LG1 (Layer gap)
(3) Distance between terminal and conductor	EG11 (Device embedding gap)

The number used in the indication is the number of layers. The left number in (3) is for the conductor layer and the number on the right shows the step, first, second, etc., of the multi-device embedding into the substrate. See 7.2.3 for the definition of steps (layers). Figures 35 and 36 show the definition of layers of a device embedded substrate for cases of pad and via connections. Additional remarks are added to Figures 37 and 38 for the dielectric gap, layer gap and device embedding gap.

a) Insulation layer thickness, conductor separation and terminal/conductor distance in pad connection

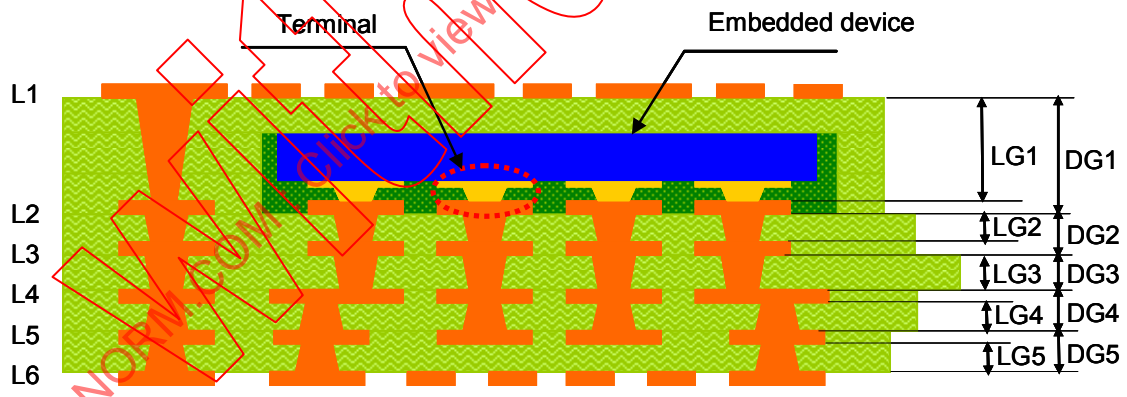


Figure 35 – Definitions of dielectric gap and layer gap in the pad connection method

b) Insulation layer thickness, conductor separation and terminal/conductor distance in via connection

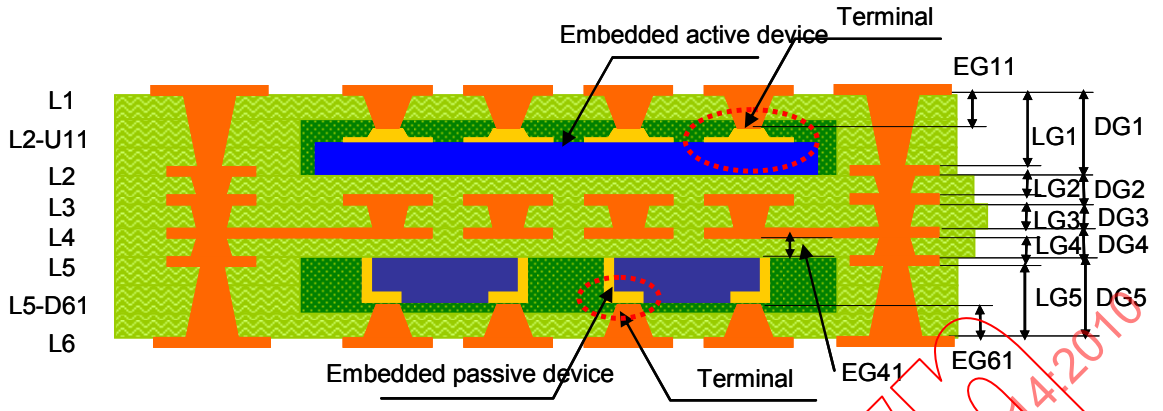


Figure 36 – Definitions of dielectric gap and layer gap in the via connection method

c) Additional remark on insulation layer thickness

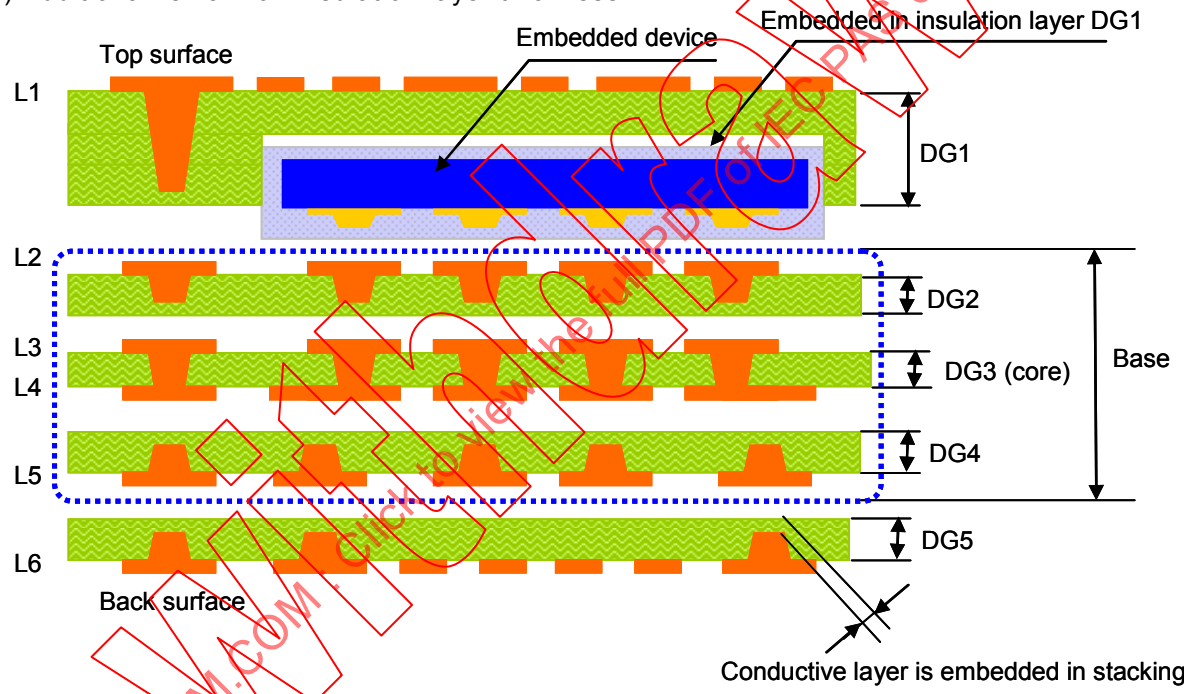


Figure 37 – Additional illustration of dielectric gap

d) Remarks on conductor separation and terminal/conductor distance

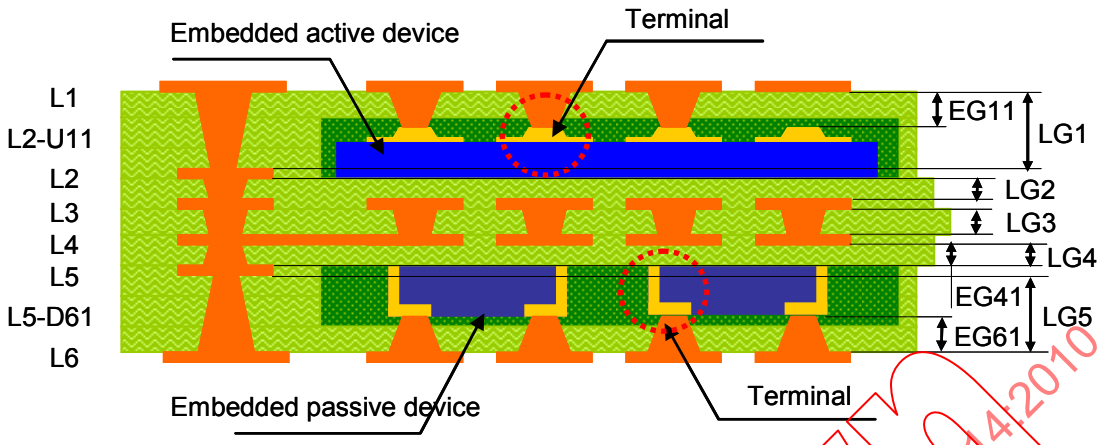


Figure 38 – Additional illustration of layer gap

7.3 Conditions for base

Base board and assembly condition are given in Table 18.

Table 18 – Requirements to device assembly to base substrate of device embedded boards

Item		Condition	Remarks
Base	Base material	Organic: FR-4, FR-5, BT Resin, polyimide, PPE, PTFE Inorganic: ceramics, LTCC	Copper foil carrier, metal heat fin for heat radiation, film type carrier, silicon interposer., ceramics interposer
	Board structure	Single sided, double sided、 Multilayer, Build-up multilayer, Single-sided flexible, double-sided flexible, Multilayer flexible, Ceramics, LTCC electronic circuit substrate Passive device embedded ceramics	
	Number of layers	1 layer, 2 layers, ~ arbitrary number of layers	
	Copper foil	5 µm, 9 µm, 12 µm, 18 µm, 35 µm, 70 µm	
	Insulator	> 10 µm	
	Maximum size	610 mm × 510 mm	Variable based on the capability of die Bonder and/or chip mounter
	Minimum size	340 mm × 250 mm	
Embedded layer	Insulation material	Prepreg such as FR-4, FR-5, BT Resin, polyimide, PPE, PTFE (B stage type) Resin such as FR-4、FR-5、BT resin, polyimide, etc. Sealing resin used for semiconductor packages Others	A cut-off may be required for a thick embedding device
	Number of layers	1 layer, 2 layers, ~ arbitrary number of layers	
	Copper foil	5 µm, 9 µm, 12 µm, 18 µm, 35 µm, 70 µm	
	Board size	Depends on the base size	
Condition	Die bonder	Maximum : 330 mm × 250 mm × 2,5 mm Minimum : 50 mm × 50 mm × 0,5 mm	A carrier may be necessary if the thickness is less than 0,3 mm
	Mounter	Maximum : 510 mm × 460 mm × 4,0 mm Minimum : 50 mm × 50 mm × 0,3 mm	
	Fiducial mark	Fiducial mark shall be in accordance to customers process capability	
	Position accuracy	To be agreed by customer based materials and process capability	
Condition for sheet components	Die bonder	Maximum : 25 mm × 25 mm × 0,5 mm Minimum : 0,25 mm × 0,25 mm × 0,1 mm	
	Mounter	Maximum : 24 mm × 24 mm × 6,5 mm Minimum : 0,4 mm × 0,2 mm × 0,12 mm	
	Thermal resistance	Withstand for 120 min at 180 °C	
	Resistance to pressure	3 MPa ~4 MPa	
	Resistance to chemical solvent	To be agreed by customer based materials and process capability	

NOTE The above assembly requirements are for reference to the Standard drafting committee for device embedding substrate. Detailed requirements are to be agreed between user and supplier.

7.4 Conditions for embedding devices

Work panel size, panel thickness and embedding condition are shown in Table 19 when automatic device embedding equipment is used.

Table 19 – Embedding requirement

Assembly		Device	Shape		Direction (to embedded terminals)	Panel size mm		Thickness mm		Fiducial mark
						Max.	Min.	Max.	Min.	
Pad bonding	Die bonding	Bare die	WB		Up	267×90	90×15	0,9	0,1	—
			TAB		Up	—	—	—	—	—
	Mounting	Bare die	FC	US	Down	330×250	50×50	2,5	0,5	＊1
				C4 *4 (note 1)	Down	330×250 510×460	50×50 50×50	2,5 4,0	0,5 0,3	＊1 ＊2
				GBS	Down	330×250	50×50	2,5	0,5	＊1
				ESC、ES C5	Down					
				ACF(P)	Down					
				NCF(P)	Down					
				Others	Down	—	—	—	—	—
	Mounting	WLP	Reflow Resin bonding		Down	510×460	50×50	4,0	0,3	＊2
		Package	Reflow Resin bonding		Down					
		Rectan-gular chip	Reflow Resin bonding		Down					
		Rod	Reflow Resin bonding		—					
		Module MEMS	Reflow		Down					
Via bonding	Die bonding	Bare die	Copper plating Conductive paste		Up	310×215	50×30	3,0	0,1	＊3
		WLP Package	Copper plating Conductive paste		Up					
	Mounting	Rectan-gular chip	Copper plating Conductive paste		Up	510×460	50×50	4,0	0,3	＊2
		Module MEMS	Copper plating Conductive paste		Up					

Size and shape of fiducial mark

Size = ＊1 : 0,25 ～ 0,8 mm, ＊2 : 0,5 mm ～ 1,6 mm, ＊3 : 0,2 ～ 1,6 mm、

Shape = circle, cross, square

NOTE 1 *4 (C4): on upper layer for terminal pitch ≧0,3 mm, on lower layer for terminal pitch ＜0,3 mm.

NOTE 2 The above assembly requirements are for reference. Detailed requirements are to be agreed between user and supplier.

Table 20 shows the embedding methods of semiconductor devices and Table 21 for electronic devices.

Table 20 – Mounting methods of semiconductor devices

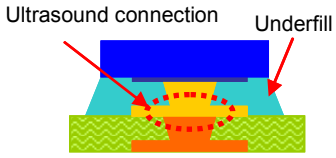
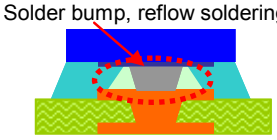
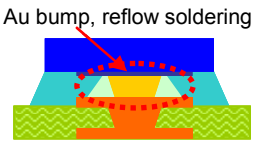
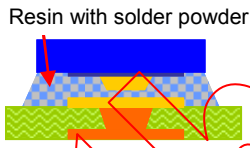
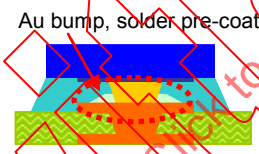
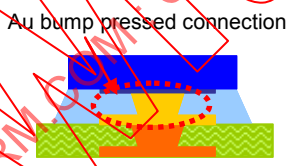
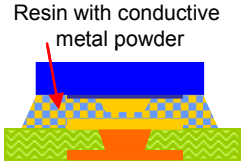
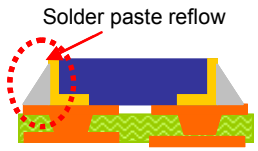
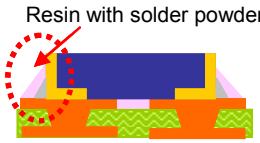
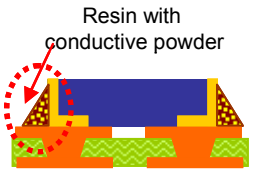
Method	Schematic diagram	Short name	Name	Explanation
Metal bonding		US	Ultra Sonic Bonding	Ultrasonic energy is applied between semiconductor terminal (bump) and board electrode to metal bond and then underfill thermosetting resin for mechanical reinforcement. Gold is often used for the bumps and connecting pads of the board.
		C4	Controlled Collapse Chip Connection	Reflow solder bumps LSI with high temperature solder and underfill resin after cleaning the joints. Solder pre-coat, Au plating, OSP are used.
		GBS	Gold Bump Soldering	LSI with Au bumps are pressed to board with solder pre-coated pads and heated to bond the junctions, then underfill to mechanical reinforcement
		ESC5	Epoxy Encapsulated Solder Connection 5th	Use solder powder mixed thermosetting adhesive and press and heat to bond the device to board. Au plating or OSP are used for the pads of board.
		ESC	Epoxy Encapsulated Solder Connection	Thermosetting resin is used between LSI bumps and solder pre-coated boards pads. Press and heat to establish electrical interconnection.
Compression bonding		NCF (P)	Non Conductive Film (Paste)	Thermosetting resin is used between LSI Au bumps and boards pads. Press and heat to establish electrical interconnection. Au plating is usually used for pads on board.
		ACF (P)	Anisotropic Conductive Film (Paste)	Thermosetting resin mixed with conductive powder is applied to the connecting electrodes and then press and heat to obtain electrical connection. Au plating is usually used for pads on board.

Table 21 – Mounting method of devices

Method	Schematic diagram	Short name	Name	Explanation
Reflow		—	Soldering	Bonding by reflow soldering. It is necessary to clean flux used in reflow soldering.
Resin		—	Solder-resin Bonding	Use solder powder mixed adhesive and reflow to bond the device to board.
		—	Conductive adhesive bonding	Use conductive thermosetting adhesive and harden the resin after mounting a device on a board to attain electrical conduction